National Semiconductor

March 1996

DM74ALS652/74ALS652-1
Octal TRI-STATE® Bus Transceiver and Register

General Description

This device incorporates an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high level logic drive provide this device with the capability of being connected directly to and driving the bus lines in a bus organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'ALS652-1 version features the same performance as the standard versions, with the addition of increased current drive capability to meet the current requirements of various bus architectures. For all ALS-1 products, the recommended maximum I_{OL} is increased to 48 mA.

The registers in the 'ALS652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

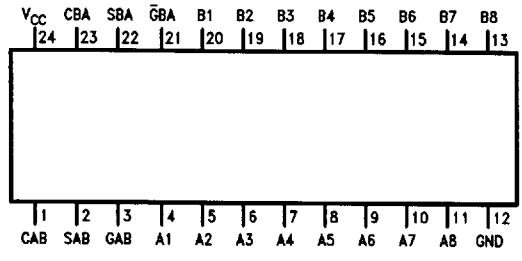
The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable (GAB and $\overline{G}$BA) control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

- Maximum I_{OL} increased to 48 mA for 'ALS652-1 product
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Independent registers and enables for A and B buses
- Multiplexed real-time and stored data

Connection Diagram



TL/F/9174–1

Order Number DM74ALS652NT, 74ALS652-1NT, DM74ALS652WM or 74ALS652-1WM
See NS Package Number M24B or N24C

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	44.5°C/W
M Package	80.5°C/W

Note: This product meets application requirements of 500 temperature cycles from −65°C to +150°C.

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74ALS652/74ALS652-1			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current	ALS652			24	mA
		ALS652-1			48	
f_{CLK}	Clock Frequency		0		40	MHz
t_W	Pulse Duration, Clocks Low or High		12.5			ns
t_{SU}	Data Setup Time, A before CAB or B before CBA		10 ↑			ns
t_H	Data Hold Time, A after CAB or B after CBA		0 ↑			ns
T_A	Free Air Operating Temperature		0		70	°C

↑ = with reference to the low to high transition of the respective clock.

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		
			I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
			I_{OL} = 48 mA		0.35	0.5	
I_I	Input Current at Max Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100	μA
			Control Inputs, V_I = 7V			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V, (Note 1)				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)	Control Inputs			−200	μA
			I/O Ports			−200	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		47	76	mA
			Outputs Low		55	88	
			Outputs Disabled		55	88	

Note 1: For I/O ports the TRI-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

Switching Characteristics over recommended operating free air temperature range (Notes 1, 2)

Symbol	Parameter	Conditions	From (Input) To (Output)	DM74ALS652/ 74ALS652-1		Units
				Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, $R_1 = R_2$ = 500Ω, T_A = Min to Max	CBA or CAB to A or B	10	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CBA or CAB to A or B	5	17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B to B or A	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	3	12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	12	35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	6	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	5	20	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$BA to A	3	17	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$BA to A	5	18	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$BA to A	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$BA to A	2	16	ns
t_{PZH}	Output Enable Time to High Level Output		GAB to B	6	22	ns
t_{PZL}	Output Enable Time to Low Level Output		GAB to B	6	18	ns
t_{PHZ}	Output Disable Time from High Level Output		GAB to B	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		GAB to B	2	16	ns

Note 1: See Section 5 for test waveforms and output load.
Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Function Table

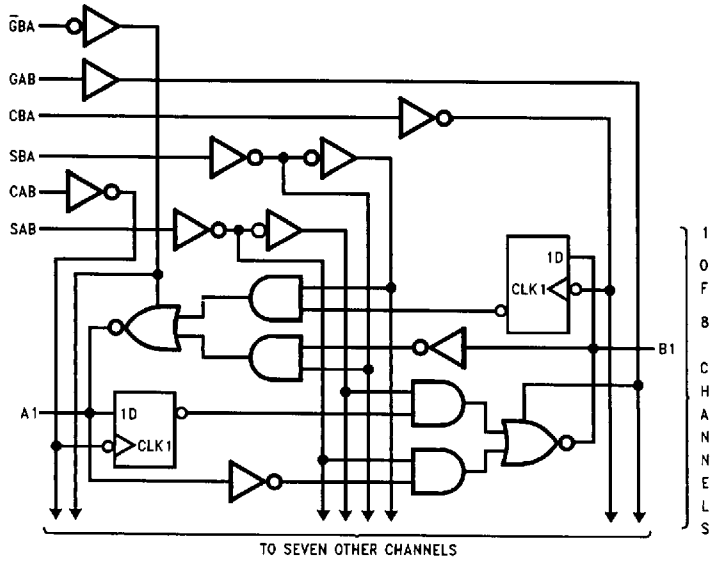
Inputs						Data I/O (Note 3)		Operation or Function
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
X	H	↑	H/L	X	X	Input	Not Specified	Store A, Hold B
L	X	H/L	↑	X	X	Not Specified	Input	Store B, Hold A
L	H	↑	↑	X	X	Input	Input	Store A and B Data
L	H	H/L	H/L	X	X	Input	Input	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H/L	X	H	Output	Input	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	↑	↑	X	X	Input	Output	Stored A Data to B Bus
H	H	↑	↑	X (Note 4)	X	Input	Output	Store A in both Registers
L	L	↑	↑	X	X (Note 4)	Output	Input	Store B in both Registers

Note 3: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Note 4: Select control = L; clocks can occur simultaneously
Select control = H; clocks must be staggered in order to load both registers.

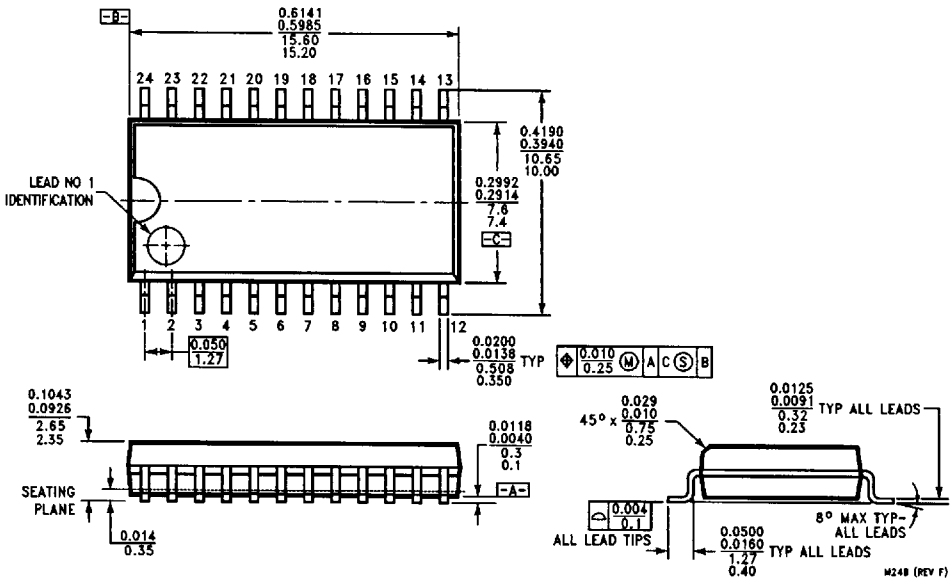
H = High Logic Level, L = Low Logic Level, X = Don't Care (Either Low or High Logic Levels, including transitions), H/L = Either Low or High Logic Level excluding transitions, ↑ = Positive-going edge of pulse.

Logic Diagram



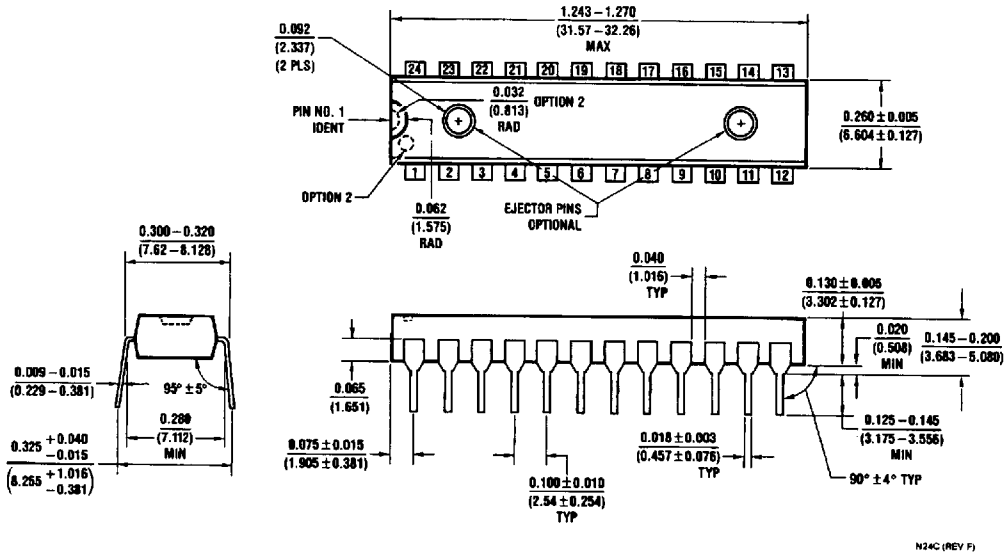
TL/F/9174–2

Physical Dimensions inches (millimeters)



S.O. Package (WM)
Order Number DM74ALS652WM or 74ALS652-1WM
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (NT)
Order Number DM74ALS652NT or 74ALS652-1NT
NS Package Number N24C

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408