National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC402A-X-RH REV 0A0

Original Creation Date: 05/16/00
Last Update Date: 05/31/00
Last Major Revision Date:

LOW-GAIN OP AMP WITH FAST 14-BIT SETTLING: ALSO AVAILABLE GUARANTEED TO 300K RAD(Si) TESTED TO MIL-STD-883, METHOD 1019.5

General Description

The CLC402 is an operational amplifier designed for low-gain applications ($\pm$ 1 to $\pm$ 8), requiring fast, accurate settling and superior DC accuracy. Settling to 0.0025% in 25ns (32ns guaranteed over temperature), the CLC402 is ideal as the input amplifier in high accuracy (up to 14-bits) A/D systems. Unlike most other high-speed op amps, the CLC402 is free of thermally induced tails in the settling response.

The CLC402 is an upgrade to, and pin compatible with, the industry standard CLC400. Constructed using a unique, proprietary design and an advanced complementary bipolar process, it offers performance far beyond ordinary monolithic op amps. In addition, unlike many other high-speed op amps, the CLC402 offers both high performance and stability without the need for compensation circuitry - even at a gain of + 1.

Supporting the CLC402's excellent pulse performance are improved DC characteristics. The CLC402's input offset voltage is typically 0.5mV and is guaranteed to be less than 1.6mV at +25C. The input offset voltage drift is typically only 3uV/C.

Industry Part Number

CLC402A

NS Part Numbers

CLC402AJ-QML
CLC402AJFQML

Prime Die

UB1303B

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 0.0025% settling in 25ns (32ns max)
- 0.5mV input offset voltage, 3uV/C drift
- ±1 to ±8 closed-loop gain range
- Low power, 150mW
- 0.01%/0.05 degrees differential gain/phase

CONTROLLING DOCUMENT:

CLC402AJ-QML	5962-9203301MPA
CLC402AJFQML	5962F9203301MPA

Applications

- High-accuracy A/D systems (12-14 bits)
- High-accuracy D/A converters
- High-speed communications
- IF processors
- Video distribution

(Absolute Maximum Ratings)

(Note 1)

Supply voltage (Vcc)	±7 V dc
Output current (Io)	±70 mA
Maximum Power dissipation (Pd) (Note 2)	305mW
Storage temperature range	-65 C ≤ Ta ≤ +150 C
Lead temperature (soldering, 10 seconds)	+300C
Junction temperature (Tj)	175C
Thermal Resistance	
(ThetaJA) Junction-to-ambient	
Ceramic DIP (Still Air)	TBD
(500 LFPM)	TBD
(ThetaJC) Junction-to-case	
Ceramic DIP	TBD
Package Weight (Typical)	
Ceramic DIP	TBD
ESD Tolerance	
ESD Rating (Note 3)	2000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) /ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply voltage (Vcc)	±5 V dc
Gain Range	±1 to ±10
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 4)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5 V dc, Av = +2, Rf = 250 Ohms, Rg = 250 Ohms, -55C ≤ Ta ≤ +125C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input bias current, noninverting				-25	25	uA	1
					-35	35	uA	2
					-45	45	uA	3
DIBN	Input bias current, average temperature coefficient, noninverting		1		-100	100	nA/C	2
			1		-250	250	nA/C	3
Ibi	Input bias current, inverting				-30	30	uA	1
					-40	40	uA	2
					-50	50	uA	3
DIBI	Input bias current, average temperature coefficient, inverting		1		-100	100	nA/C	2
			1		-250	250	nA/C	3
Vio	Input offset voltage				-1.6	1.6	mV	1
					-2.8	2.8	mV	2
					-2.6	2.6	mV	3
DVIO	Input offset voltage, average temperature coefficient		1		-12	12	uV/C	2, 3
Icc	Supply current no load					20	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	-Vcc = -4.5 V to -5.0 V +Vcc = +4.5V to +5.0 V	2		60		dB	1, 2
			2		55		dB	3
+Io	Output current		1		45		mA	1, 2
			1		25		mA	3
-Io	Output current		1			-45	mA	1, 2
			1			-25	mA	3
+Vo	Output voltage swing	Rl = 100 Ohms	1		2.8		V	4, 5
			1		2.3		V	6
-Vo	Output voltage swing	Rl = 100 Ohms	1			-2.8	V	4, 5
			1			-2.3	V	6

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 4) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5 V dc, Av = +2, Rf = 250 Ohms, Rg = 250 Ohms, -55C ≤ Ta ≤ +125C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rin	Noninverting input resistance		1		85		K Ohms	1, 2
			1		50		K Ohms	3
Cin	Noninverting input capacitance		1			5.5	pF	4, 5, 6
Ro	Output impedance		1			0.1	Ohms	1, 2, 3
CMRR	Common mode rejection ratio	Vcm = ±1.0 V	1		60		dB	4, 5
			1		55		dB	6

Electrical Characteristics

AC PARAMETERS: (SEE NOTE 4)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5 V dc, Av = +2, Rf = 250 Ohms, Rg = 250 Ohms, -55C ≤ Ta ≤ +125C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small signal bandwidth	-3 dB bandwidth Vout < 0.5 Vpp			130		MHz	4
			2		120		MHz	5, 6
LSBW	Large Signal bandwidth	-3 dB bandwidth Vout < 5 Vpp	1		50		MHz	4, 5, 6
GFPL	Gain flatness peaking	0.1 to 25 MHz, Vout < 0.5 Vpp				0.3	dB	4
			2			0.4	dB	5, 6
GFPH	Gain flatness rolloff	>25 MHz, Vout < 0.5 Vpp				0.5	dB	4
			2			0.7	dB	5, 6
GFR	Gain flatness rolloff	0.1 MHz to 50 MHz, Vout < 0.5 Vpp				1	dB	4
			2			1	dB	5, 6
LPD	Linear phase deviation	0.1 MHz to 50 MHz, Vout < 0.5 Vpp	1			1.0	Deg	4
			1			1.2	Deg	5, 6
HD2	2nd harmonic distortion	2 Vpp at 20 MHz				-43	dBc	4
			2			-43	dBc	5
			2			-38	dBc	6
HD3	3rd harmonic distortion	2 Vpp at 20 MHz				-53	dBc	4
			2			-50	dBc	5
			2			-53	dBc	6
Trs	Rise and fall time	0.5 V step, Cl < 10 pF measured between 10% and 90% points	1			2.7	nS	9
			1			2.9	nS	10, 11
Trl	Rise and fall time	5 V step, Cl < 10 pF measured between 10% and 90% points	1			8.0	nS	9, 10, 11
Tsh	Settling time	2 V step at 0.0025% of the final value, Cl < 10 pF	1			32	nS	9, 10, 11
Tsp	Settling time	2 V step at 0.01% of the final value, Cl < 10 pF	1			25	nS	9, 10, 11
Ts	Settling time	2 V step at 0.01% of the final value, Cl < 10 pF	1			15	nS	9, 10, 11
Os	Overshoot	0.5 V step, Cl < 10 pF	1			10	%	9, 10, 11
Sr	Slew rate	Vout = 4V step, measured at ±1V, Cl < 10pF	1		500		V/uS	4, 5, 6
SNF	Equivalent input noise, total noise floor	> 1MHz	1			155	dBm (1Hz)	4, 5, 6

Electrical Characteristics

AC PARAMETERS: (SEE NOTE 4) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5 V dc, Av = +2, Rf = 250 Ohms, Rg = 250 Ohms, -55C ≤ Ta ≤ +125C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
INV	Equivalent input noise, total integrated noise	100MHz to 150MHz	1			49	uV	4, 5, 6

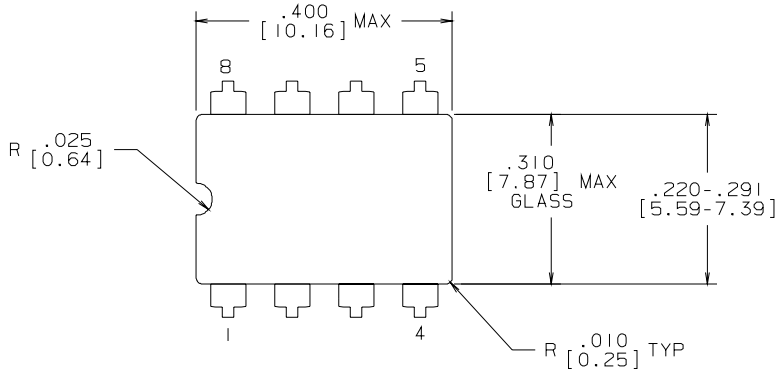
Note 1: Guaranteed, if not tested.
Note 2: This parameter is group A sample tested only and is excluded from final electrical testing, but is guaranteed to the limits specified.
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
Note 4: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5

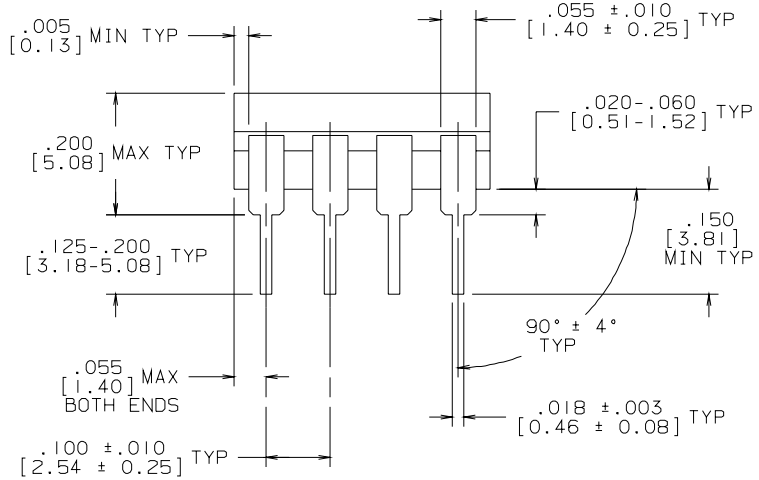
Graphics and Diagrams

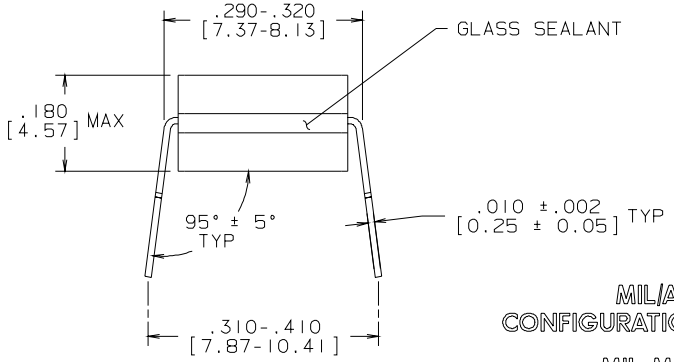
GRAPHICS#	DESCRIPTION
07081HRA4	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000420A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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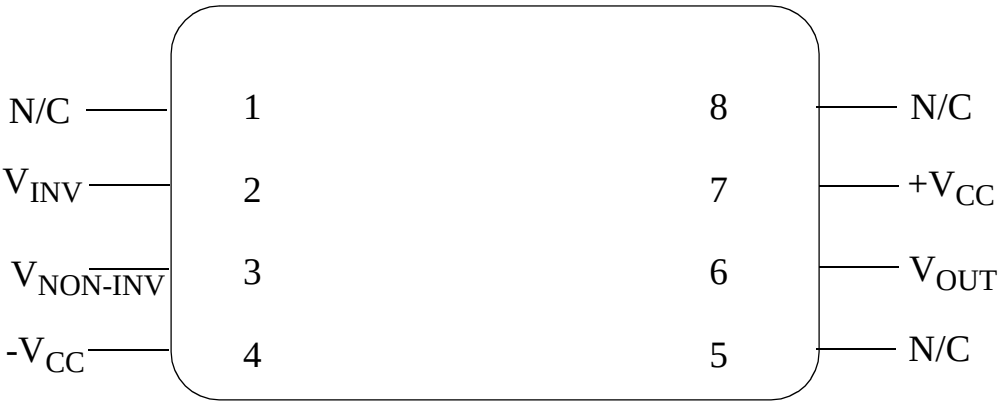
CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC402J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000420A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003719	05/31/00	Rose Malone	Initial MDS Release: MNCLC402A-X-RH, Rev. 0A0. Added Rad Hard Devices. Replaces MDS: MNCLC402A, Rev. 0A0.