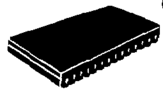
MCM6229BA

Product Preview

256K x 4 Bit Static Random Access Memory

J PACKAGE
300 MIL SOJ
CASE 810B–03



WJ PACKAGE
400 MIL SOJ
CASE 810–03

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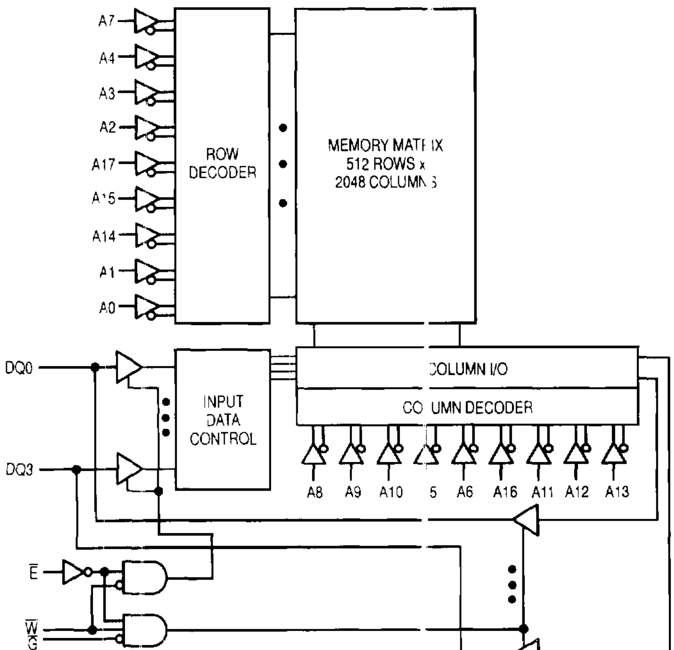
The MCM6229BA is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high–performance silicon–gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6229BA is equipped with both chip enable (Ē) and output enable (G̅) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs to high impedance.

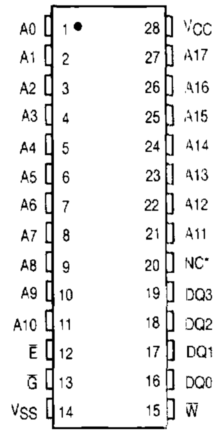
The MCM6229BA is available in 300 mil and 400 mil, 28–lead surface–mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Low Power Operation: 120/115/110/105/100 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Inputs
W̅	Write Enable
G̅	Output Enable
Ē	Chip Enable
DQ0 – DQ3	Data Inputs/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC*	No Connection

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	μA
AC Active Supply Current (I_{out} = 0 mA, all inputs = V_{IL} or V_{IH}, V_{IL} = 0, V_{IH} ≥ 3 V, cycle time ≥ t_{AVAV} min, V_{CC} = max)	MCM6229BA–15: t_{AVAV} = 15 ns MCM6229BA–17: t_{AVAV} = 17 ns MCM6229BA–20: t_{AVAV} = 20 ns MCM6229BA–25: t_{AVAV} = 25 ns MCM6229BA–35: t_{AVAV} = 35 ns	I_{CCA}	— — — — —	135 120 115 110 100	mA
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	MCM6229BA–15: t_{AVAV} = 15 ns MCM6229BA–17: t_{AVAV} = 17 ns MCM6229BA–20: t_{AVAV} = 20 ns MCM6229BA–25: t_{AVAV} = 25 ns MCM6229BA–35: t_{AVAV} = 35 ns	I_{SB1}	— — — — —	45 40 35 30 25	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

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CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs except Clocks & DQs $\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . 2 ns
Input Timing Measurement Reference Level . . . . 1.5 V
Output Timing Measurement Reference Level . . . . 1.5 V
Output Load . . . . See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6229BA–15		6229BA–17		6229BA–20		6229BA–25		6229BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6 ,7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

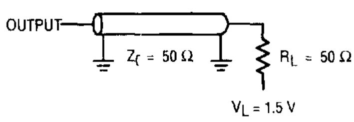


Figure 1A

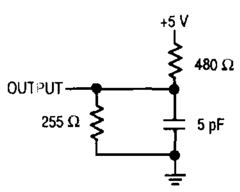
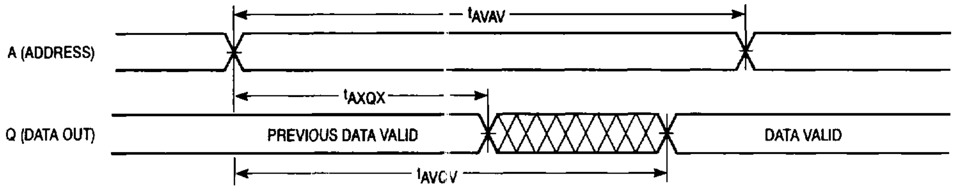


Figure 1B

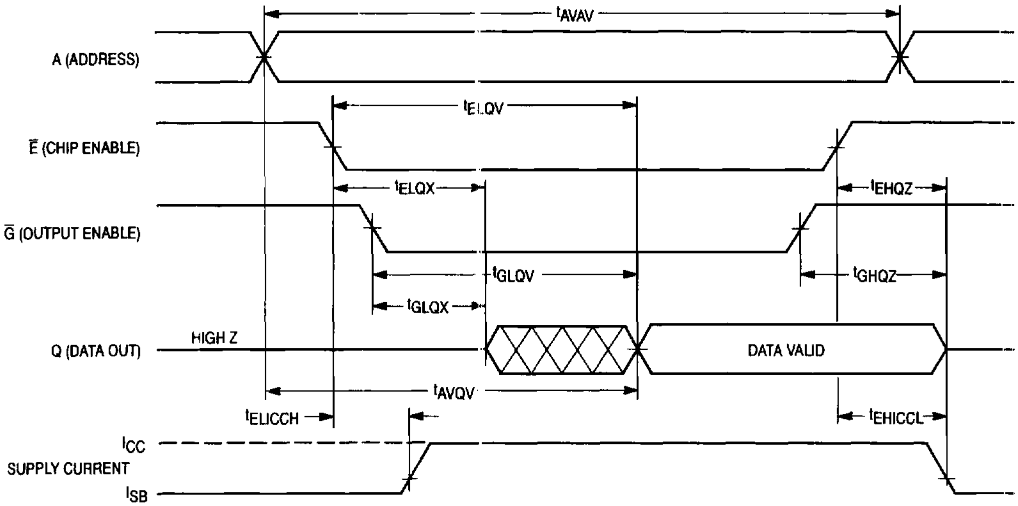
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)



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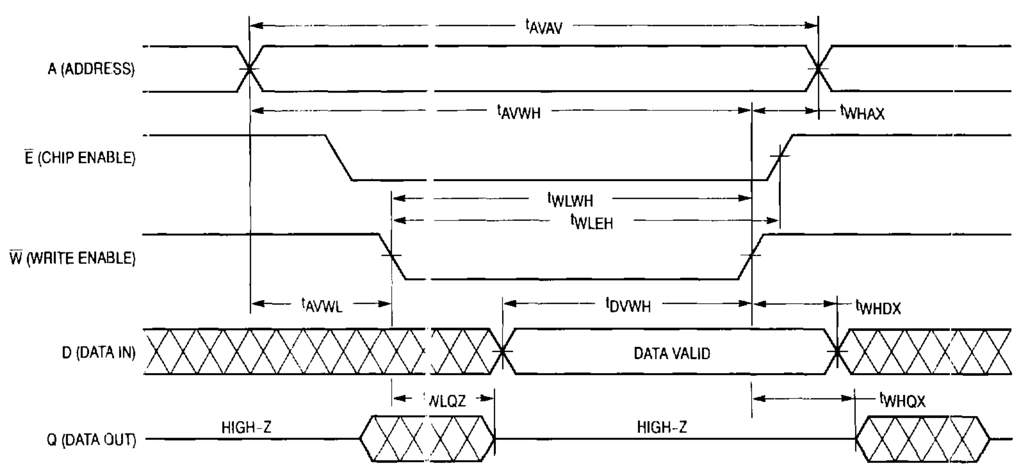
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229BA–15		6229BA–17		6229BA–20		6229BA–25		6229BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	7	—	8	—	9	—	10	—	11	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady–state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, and 3)

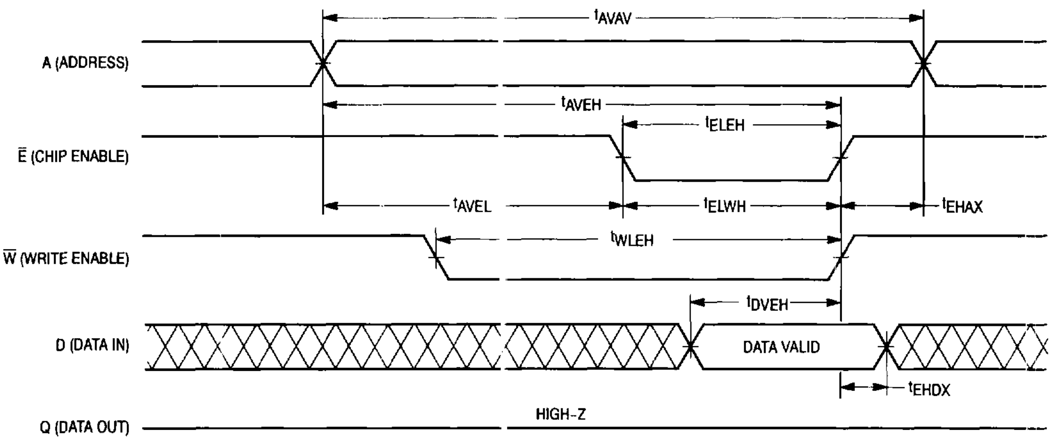


WRITE CYCLE 2 (Ē Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	6229BA–15		6229BA–17		6229BA–20		6229BA–25		6229BA–35		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	12	—	14	—	15	—	17	—	20	—	ns	5, 6
Write Pulse Width	t_{WLEH}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	8	—	9	—	9	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of Ē low and W̄ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If Ḡ goes low coincident with or after W̄ goes low, the output will remain in a high–impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If Ē goes low coincident with or after W̄ goes low, the output will remain in a high–impedance state.
6. If Ē goes high coincident with or before W̄ goes high, the output will remain in a high–impedance state.

WRITE CYCLE 2 (Ē Controlled See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6229BA XX XX X

- Motorola Memory Prefix — MCM
- Part Number — 6229BA
- Package (J = 300 mil SOJ, WJ = 400 mil SOJ)
- Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Shipping Method (R = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6229BAJ15 MCM6229BAJ15R MCM6229BAWJ15 MCM6229BAWJ15R
MCM6229BAJ17 MCM6229BAJ17R MCM6229BAWJ17 MCM6229BAWJ17R
MCM6229BAJ20 MCM6229BAJ20R MCM6229BAWJ20 MCM6229BAWJ20R
MCM6229BAJ25 MCM6229BAJ25R MCM6229BAWJ25 MCM6229BAWJ25R
MCM6229BAJ35 MCM6229BAJ35R MCM6229BAWJ35 MCM6229BAWJ35R