TC74HC564AP/AF
TC74HC574AP/AF/AFW

Octal D-Type Flip-Flop with 3-State Output
TC74HC564A Inverting
TC74HC574A Non-Inverting

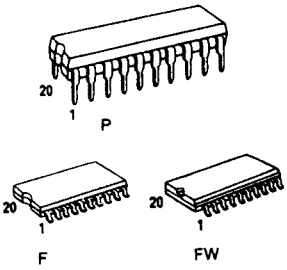
The TC74HC564A and HC574A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type Flip-Flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

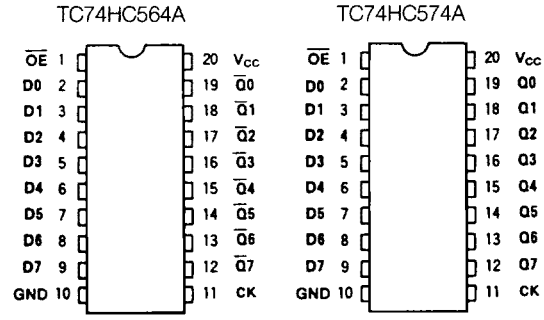
The TC74HC564A has inverting outputs, and the TC74HC574A has non-inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Features

- High Speed: f_{MAX} = 62MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ 28% V_{CC} (Min)
- Output Drive Capability: 15 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 6mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS564/574



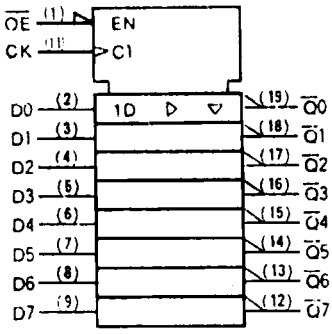
Pin Assignment

Truth Table

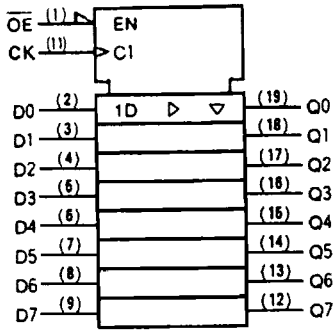
Inputs			Outputs	
$\overline{OE}$	CK	D	Q(574A)	$\overline{Q}$(564A)
H	X	X	Z	Z
L	↑	X	Qn	$\overline{Qn}$
L	↓	L	L	H
L	↓	H	H	L

X: Don't Care
Z: High Impedance
Q_n($\overline{Q}_n$): No Change

TC74HC564A

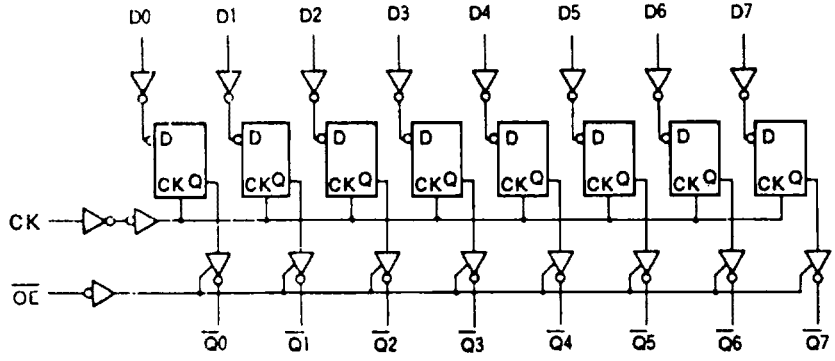


TC74HC574A

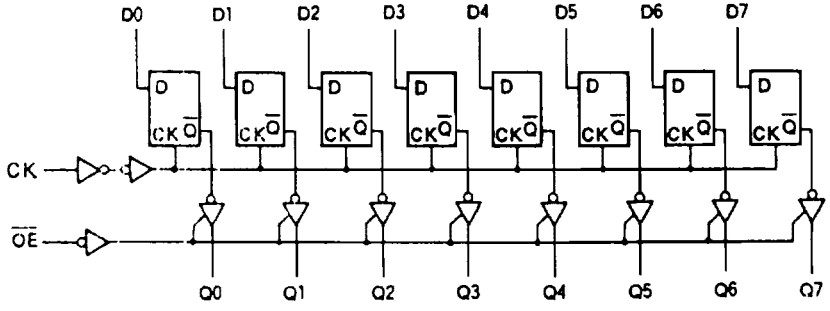


IEC Logic Symbol

TC74HC564A



TC74HC574A



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -6 mA I_{OH} = -7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 6 mA I_{OL} = 7.8mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	–	–	±0.5	–	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		–	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	–	2.0	–	75	95	ns
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Setup Time (Dn)	t_s	–	2.0	–	75	95	
			4.5	–	15	19	
			6.0	–	13	16	
Minimum Removal Time (Dn)	t_h	–	2.0	–	0	0	
			4.5	–	0	0	
			6.0	–	0	0	
Clock Frequency	f	–	2.0	–	6	5	MHz
			4.5	–	31	24	
			6.0	–	36	28	

AC Electrical Characteristics ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
			CL	V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	50	2.0	–	25	60	–	75	ns
				4.5	–	7	12	–	15	
				6.0	–	6	10	–	13	
Propagation Delay Time (CK-Q, $\overline{Q}$)	t_{pLH}	–	50	2.0	–	70	150	–	190	
				4.5	–	20	30	–	38	
				6.0	–	15	26	–	33	
	t_{pHL}		150	2.0	–	88	190	–	240	
				4.5	–	25	38	–	48	
				6.0	–	19	33	–	41	
Output Enable Time	t_{pZL}	$R_L = 1k\Omega$	50	2.0	–	48	125	–	155	
				4.5	–	15	25	–	31	
				6.0	–	12	21	–	26	
	t_{pZH}		150	2.0	–	60	165	–	205	
				4.5	–	20	33	–	41	
				6.0	–	16	28	–	35	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	–	34	125	–	155	
				4.5	–	17	25	–	31	
				6.0	–	15	21	–	26	
Maximum Clock Frequency	f_{MAX}	–	50	2.0	6	17	–	5	–	
				4.5	31	50	–	24	–	
				6.0	36	59	–	28	–	
Input Capacitance	C_{IN}	–			–	5	10	–	10	pF
Output Capacitance	C_{OUT}	–			–	10	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)	–			–	54	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/8(\text{per bit})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 39 + 15 \bullet n$$