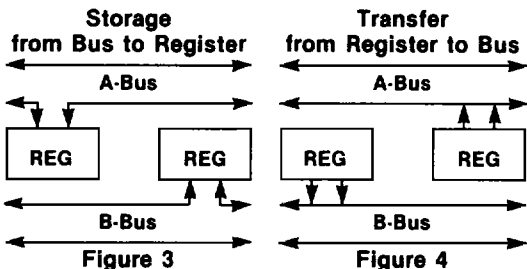
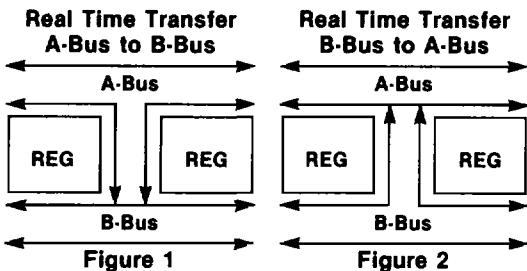


54AC/74AC646

Octal Transceiver/Register With 3-State Outputs

Description

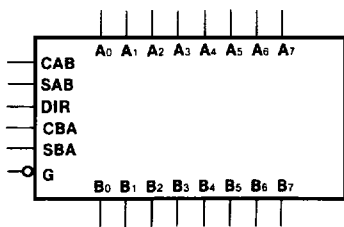
The 'AC646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.



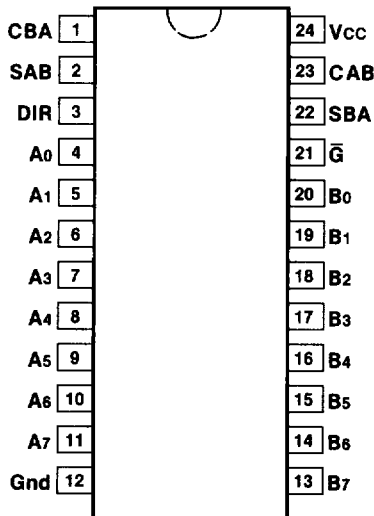
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA

Ordering Code: See Section 6

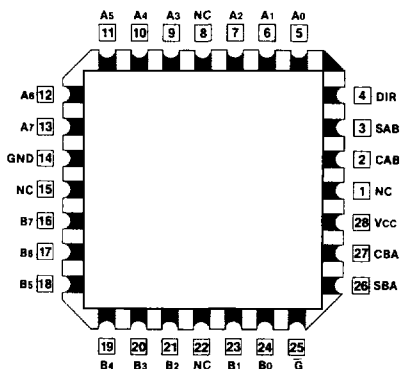
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

- A0 - A7 Data Register Inputs
- B0 - B7 Data Register A Outputs
- CAB, CBA Data Register B Inputs
- SAB, SBA Data Register B Outputs
- DIR, \bar{G} Clock Pulse Inputs
- Output Enable Inputs

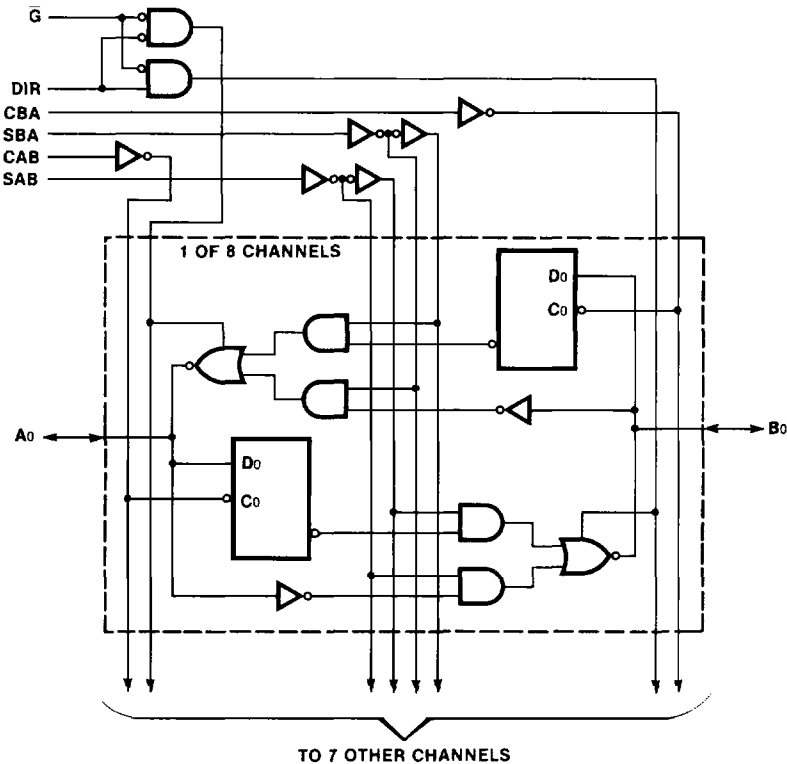
Function Table

Inputs						Data I/O*		Operation or Function
\bar{G}	DIR	CAB	CBA	SAB	SBA	A0 - A7	B0 - B7	
H	X	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data
H	X	\downarrow	\downarrow	X	X			
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus
L	L	X	X	X	H			
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus
L	H	H or L	X	H	X			

*The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 \downarrow = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC646

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C

AC Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	10.5 7.5	16.5 12.0	1.0 1.0	21.0 14.5	1.0 1.0	18.5 13.0	ns	3-6
t _{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	9.5 6.5	14.5 10.5	1.0 1.0	18.0 12.5	1.0 1.0	16.0 11.5	ns	3-6
t _{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	7.5 5.0	12.0 8.0	1.0 1.0	15.0 10.0	1.0 1.0	13.5 9.0	ns	3-5
t _{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	7.5 5.0	12.5 9.0	1.0 1.0	15.5 11.0	1.0 1.0	13.5 9.5	ns	3-5
t _{PLH}	Propagation Delay SBA or SAB to A _n or B _n (w/ A _n or B _n HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.0 1.0	15.5 11.0	ns	3-6
t _{PHL}	Propagation Delay SBA or SAB to A _n or B _n (w/ A _n or B _n HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.0 1.0	15.0 11.0	ns	3-6
t _{PZH}	Enable Time G̅ to A _n or B _n	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.5	1.0 1.0	14.0 10.0	1.0 1.0	12.5 9.0	ns	3-7
t _{PZL}	Enable Time G̅ to A _n or B _n	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	15.5 11.0	1.0 1.0	14.0 10.0	ns	3-8
t _{PHZ}	Disable Time G̅ to A _n or B _n	3.3 5.0	1.0 1.0	8.0 6.5	12.5 10.0	1.0 1.0	14.5 12.0	1.0 1.0	13.5 11.0	ns	3-7
t _{PLZ}	Disable Time G̅ to A _n or B _n	3.3 5.0	1.0 1.0	7.5 6.0	12.0 9.5	1.0 1.0	15.0 11.5	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table 1 data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPZH	Enable Time DIR to An or Bn	3.3	1.0	6.5	11.0	1.0	13.5	1.0	12.0	ns	3-7
		5.0	1.0	5.0	7.5	1.0	9.5	1.0	8.5		
tPZL	Enable Time DIR to An or Bn	3.3	1.0	7.0	11.5	1.0	14.5	1.0	13.0	ns	3-8
		5.0	1.0	5.0	8.0	1.0	10.0	1.0	9.0		
tPHZ	Disable Time DIR to An or Bn	3.3	1.0	7.5	11.5	1.0	13.5	1.0	12.5	ns	3-7
		5.0	1.0	5.5	9.5	1.0	10.5	1.0	10.0		
tPLZ	Disable Time DIR to An or Bn	3.3	1.0	7.5	12.0	1.0	15.0	1.0	13.5	ns	3-8
		5.0	1.0	5.5	9.5	1.0	10.5	1.0	10.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
ts	Set-up Time, HIGH or LOW Bus to Clock	3.3	2.0	5.0	6.0		5.5		ns	3-9
		5.0	1.5	4.0	4.5		4.5			
th	Hold time, HIGH or LOW Bus to Clock	3.3	-1.5	0	0.5		0		ns	3-9
		5.0	-0.5	0.5	1.0		1.0			
tw	Clock Pulse Width HIGH or LOW	3.3	2.0	3.5	5.0		4.5		ns	3-6
		5.0	2.0	3.5	5.0		3.5			

*Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table 1 data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CIO	Input/Output Capacitance	15.0	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance	60.0	pF	Vcc = 5.5 V