National Semiconductor

ADVANCE INFORMATION

F100331
Low Power Triple D Flip-Flop

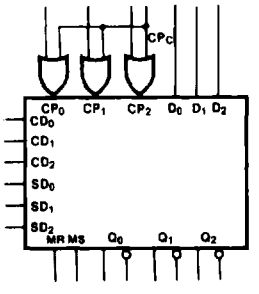
General Description

The F100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the F100131
- 2000V ESD protection
- Pin/function compatible with F100131
- Voltage compensated operating range = −4.2V to −5.7V

Logic Symbol



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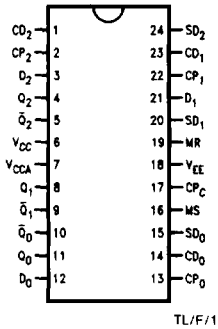
Pin Names	Description
CP_0–CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0–D_2	Data Inputs
CD_0–CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



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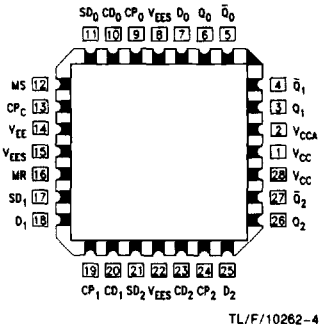
28-Pin PCC



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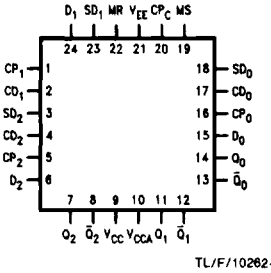
24-Pin Quad Cerpak



TL/F/10262-3