

# P4C163/P4C163L ULTRA HIGH SPEED 8K x 9 STATIC CMOS RAMS (SCRAMS)

T-46-23-12

## ★ FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 17/20/25/30/35 ns (Commercial)
  - 20/25/30/35/45 ns (Military)
- Low Power Operation (Commercial/Military)
  - 745 mW Active - 17 (Commercial)
  - 690/800 mW Active - 20, 25, 30, 35, 45
  - 125/140 mW Standby (TTL Input)
  - 1.1 mW Standby (CMOS Input) P4C163L
- Output Enable and Dual Chip Enable Control Functions
- Single 5V±10% Power Supply
- Data Retention with 2.0V Supply, 10 µA Typical Current
- Common I/O
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE II Technology™
- Standard Pinout (JEDEC Approved)
  - 28-Pin 300 mil DIP, SOJ
  - 28-Pin 350 x 550 mil LCC



## ★ DESCRIPTION

The P4C163 and P4C163L are 73,728-bit ultra high-speed static RAMs organized as 8K x 9. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V±10% tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is 10 µA from a 2.0V supply.

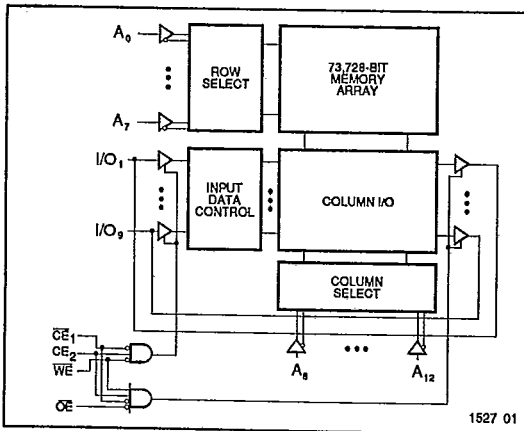
Access times as fast as 15 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption in both active and standby modes. The P4C163 and P4C163L are members of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies.

The P4C163 and P4C163L are manufactured with PACE II Technology™ which is Performance Advanced CMOS Engineering to use 0.7 micron effective channel lengths giving 400 picosecond loaded\* internal gate delays. PACE II Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, this technology features latch-up protection and single-event-upset protection, and is supported by a Class 1 facility for volume production.

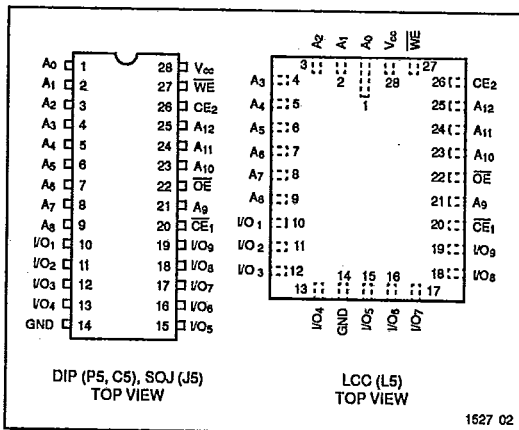
The P4C163 and P4C163L are available in 28-pin 300 mil DIP and SOJ and 28-pin 350 x 550 mil LCC packages providing excellent board level densities.

\*For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply.

## ★ FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATIONS



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★ MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Pin with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub>	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>A</sub>	Operating Temperature	-55 to +125	°C

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Symbol	Parameter	Value	Unit
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade <sup>(2)</sup>	Ambient Temperature	GND	V <sub>CC</sub>
Military	-55 to +125°C	0V	5.0V ± 10%

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Grade <sup>(2)</sup>	Ambient Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

Symbol	Parameter	Test Conditions	P4C163		P4C163L		Unit	
			Min	Max	Min	Max		
V <sub>IH</sub>	Input High Voltage		2.2	V <sub>CC</sub> +0.5	2.2	V <sub>CC</sub> +0.5	V	
V <sub>IL</sub>	Input Low Voltage		-0.5 <sup>(3)</sup>	0.8	-0.5 <sup>(3)</sup>	0.8	V	
V <sub>HG</sub>	CMOS Input High Voltage		V <sub>CC</sub> -0.2	V <sub>CC</sub> +0.5	V <sub>CC</sub> -0.2	V <sub>CC</sub> +0.5	V	
V <sub>LC</sub>	CMOS Input Low Voltage		-0.5 <sup>(3)</sup>	0.2	-0.5 <sup>(3)</sup>	0.2	V	
V <sub>CD</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA		-1.2		-1.2	V	
V <sub>OL</sub>	Output Low Voltage (TTL Load)	I <sub>OL</sub> = +10 mA, V <sub>CC</sub> = Min. I <sub>OL</sub> = +8 mA, V <sub>CC</sub> = Min.		0.5 0.4		0.5 0.4	V	
V <sub>OLC</sub>	Output Low Voltage (CMOS Load)	I <sub>OLC</sub> = +100 μA, V <sub>CC</sub> = Min.		0.2		0.2	V	
V <sub>OH</sub>	Output High Voltage (TTL Load)	I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.	2.4		2.4		V	
V <sub>OHc</sub>	Output High Voltage (CMOS Load)	I <sub>OHc</sub> = -100 μA, V <sub>CC</sub> = Min.	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max. V <sub>IN</sub> = GND to V <sub>CC</sub>	Mil. Com'l.	-10 -5	+10 +5	-5 -2	+5 +2	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CE} = V_{IH}$ V <sub>OUT</sub> = GND to V <sub>CC</sub>	Mil. Com'l.	-10 -5	+10 +5	-5 -2	+5 +2	μA

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CAPACITANCES<sup>(4)</sup>

(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	pF

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Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V<sub>IL</sub> and I<sub>IL</sub> not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20 ns.
- This parameter is sampled and not 100% tested.

**POWER DISSIPATION CHARACTERISTICS**

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Over recommended operating temperature and supply voltage<sup>(2)</sup>

Symbol	Parameter	Test Conditions	P4C163		P4C163L		Unit
			Min	Max	Min	Max	
$I_{CC}$	Dynamic Operating Current - 17	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 135	— —	n/a n/a	mA
$I_{CC}$	Dynamic Operating Current - 20, 25	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 145 125	— —	145 125	mA
$I_{CC}$	Dynamic Operating Current - 30, 35, 45	$V_{CC} = \text{Max.}, f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 100 85	— —	100 85	mA
$I_{SB}$	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}, V_{CC} = \text{Max.},$ $f = \text{Max.},$ Outputs Open	Mil. Com'l.	— 25 23	— —	25 23	mA
$I_{SB1}$	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1 \geq V_{HC}$ or $CE_2 \leq V_{LC}, V_{CC} = \text{Max.},$ $f = 0,$ Outputs Open, $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	Mil. Com'l.	— 20 18	— —	1 0.2	mA

n/a = Not Applicable

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**DATA RETENTION CHARACTERISTICS (P4C163L Only)**

Symbol	Parameter	Test Condition	Min	Typ.* $V_{CC} =$		Max $V_{CC} =$		Unit
				2.0V	3.0V	2.0V	3.0V	
$V_{DR}$	$V_{CC}$ for Data Retention		2.0					V
$I_{CCDR}$	Data Retention Current	Mil. Com'l.		10 10	15 15	200 60	300 90	$\mu\text{A}$ $\mu\text{A}$
$t_{CDR}$	Chip Deselect to Data Retention Time	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$	0					ns
$t_R^\dagger$	Operation Recovery Time	or $V_{IN} \leq 0.2V$	$t_{RC}^\S$					ns

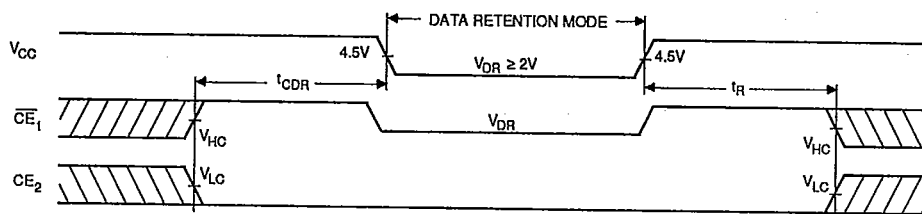
\* $T_A = +25^\circ\text{C}$

$t_{RC}$  = Read Cycle Time

$^\dagger$ This parameter is guaranteed but not tested.

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**DATA RETENTION WAVEFORM**



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AC ELECTRICAL CHARACTERISTICS—READ CYCLE

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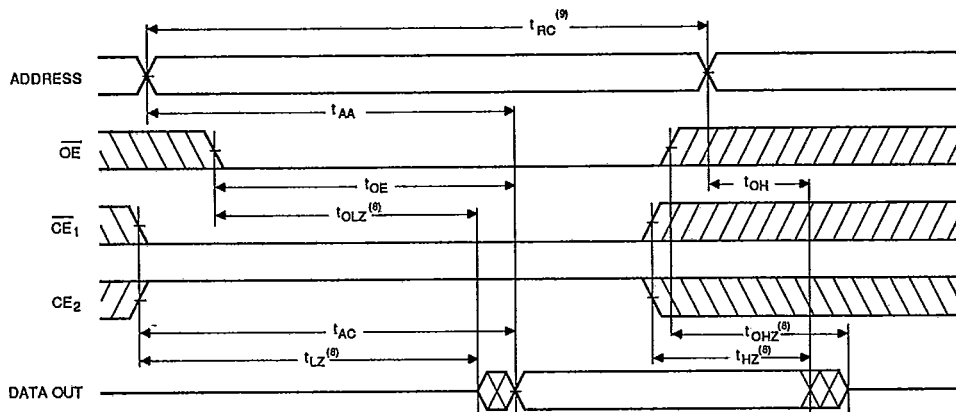
( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

Symbol	Parameter	-17*		-20		-25		-30		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{RC}$	Read Cycle Time	17		20		25		30		35		45		ns
$t_{AA}$	Address Access Time		17		20		25		30		35		45	ns
$t_{AC}$	Chip Enable Access Time		17		20		25		30		35		45	ns
$t_{OH}$	Output Hold from Address Change	2		2		3		3		3		3		ns
$t_{LZ}$	Chip Enable to Output in Low Z	2		2		3		3		3		3		ns
$t_{HZ}$	Chip Disable to Output in High Z		8		8		10		13		15		20	ns
$t_{OE}$	Output Enable Low to Data Valid		10		10		13		15		18		20	ns
$t_{OLZ}$	Output Enable Low to Low Z	2		2		3		3		3		3		ns
$t_{OHZ}$	Output Enable High to High Z		9		9		12		14		15		20	ns
$t_{PU}$	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
$t_{PD}$	Chip Disable to Power Down Time		17		20		20		20		20		25	ns

\* $V_{CC} = 5V \pm 5\%$  for -17

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READ CYCLE NO. 1 ( $\overline{OE}$  CONTROLLED)<sup>(6)</sup>



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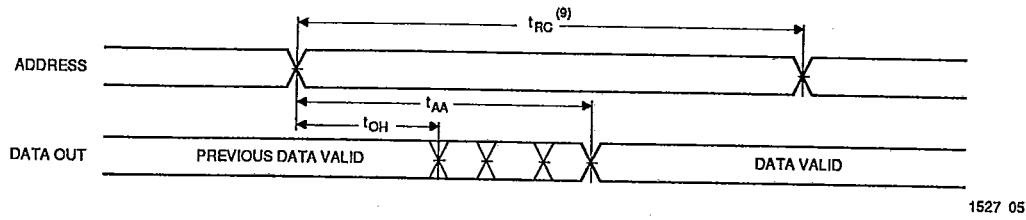
Notes:

- 5.  $\overline{WE}$  is high for READ cycle.
- 6.  $\overline{CE}_1$  is low,  $\overline{CE}_2$  is high and  $\overline{OE}$  is low for READ cycle.
- 7. ADDRESS must be valid prior to, or coincident with  $\overline{CE}_1$  transition low and  $\overline{CE}_2$  transition high.

- 8. Transition is measured  $\pm 200$  mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.

READ CYCLE NO. 2 (ADDRESS CONTROLLED) <sup>(5,9)</sup>

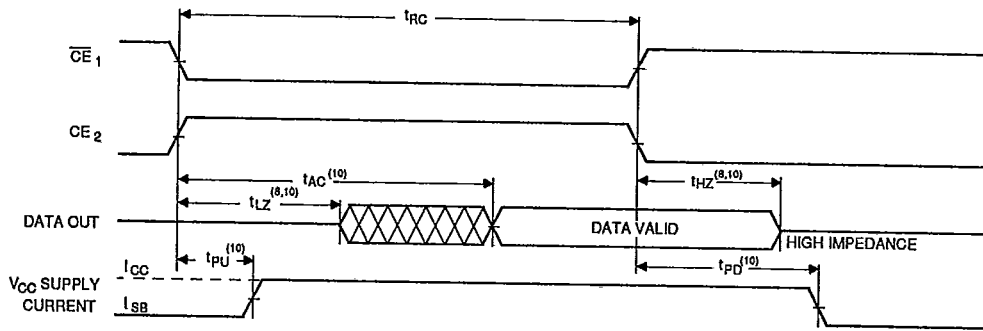
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READ CYCLE NO. 3 ( $\overline{CE}_1$ ,  $CE_2$  CONTROLLED) <sup>(5,7,10)</sup>

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Notes:

9. READ Cycle Time is measured from the last valid address to the first transitioning address.

10. Transitions caused by a chip enable control have similar delays irrespective of whether  $\overline{CE}_1$  or  $CE_2$  causes them.

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AC CHARACTERISTICS—WRITE CYCLE

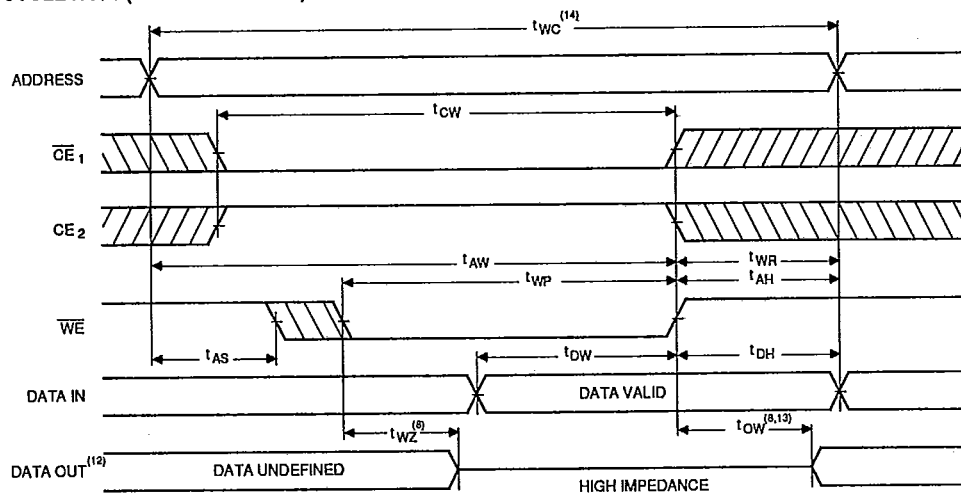
( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

Symbol	Parameter	-17*		-20		-25		-30		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{WC}$	Write Cycle Time	17		20		25		30		35		45		ns
$t_{CW}$	Chip Enable Time to End of Write	13		15		18		22		25		33		ns
$t_{AW}$	Address Valid to End of Write	13		15		18		22		25		33		ns
$t_{AS}$	Address Set-up Time	0		0		0		0		0		0		ns
$t_{WP}$	Write Pulse Width	13		15		18		20		20		25		ns
$t_{AH}$	Address Hold Time	0		0		0		0		0		0		ns
$t_{WR}$	Write Recovery Time	0		0		0		0		0		0		ns
$t_{DW}$	Data Valid to End of Write	10		11		13		15		15		20		ns
$t_{DH}$	Data Hold Time	0		0		0		0		0		0		ns
$t_{WZ}$	Write Enable to Output in High Z		7		8		10		12		14		18	ns
$t_{OW}$	Output Active from End of Write	3		3		3		5		5		5		ns

\* $V_{CC} = 5V \pm 5\%$  for -17

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WRITE CYCLE NO. 1 (WE CONTROLLED)<sup>(11)</sup>



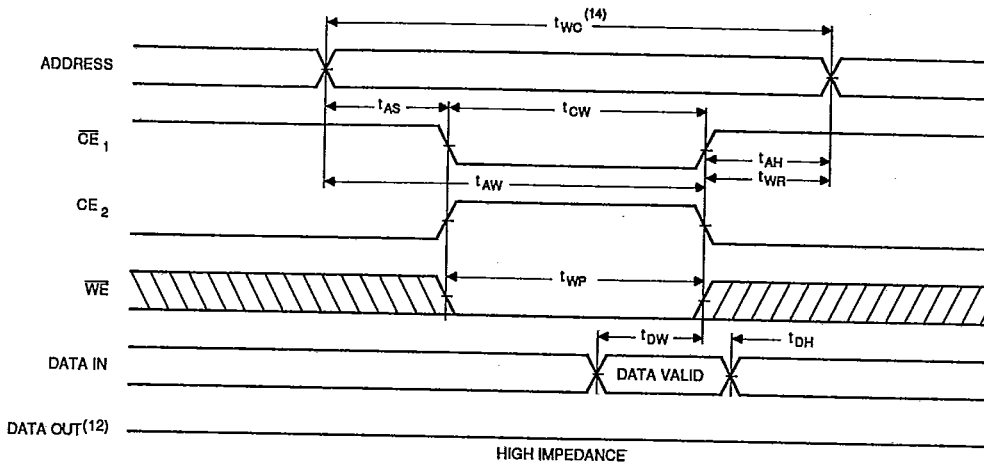
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Notes:

- 11.  $\overline{CE}_1$  and  $\overline{WE}$  must be low, and  $CE_2$  high for WRITE cycle.
- 12.  $\overline{OE}$  is low for this WRITE cycle to show  $t_{WZ}$  and  $t_{OW}$ .
- 13. If  $\overline{CE}_1$  goes high, or  $CE_2$  goes low, simultaneously with  $\overline{WE}$  high, the output remains in a low impedance state

- 14. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CE CONTROLLED) (11)



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AC TEST CONDITIONS

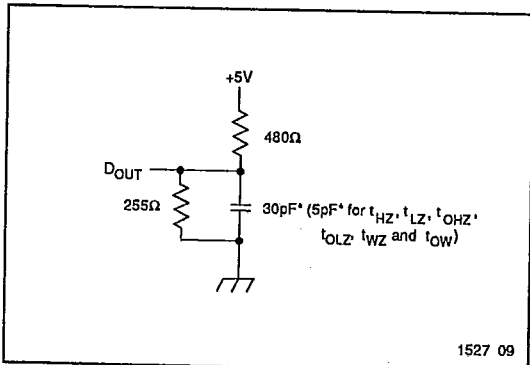
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

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TRUTH TABLE

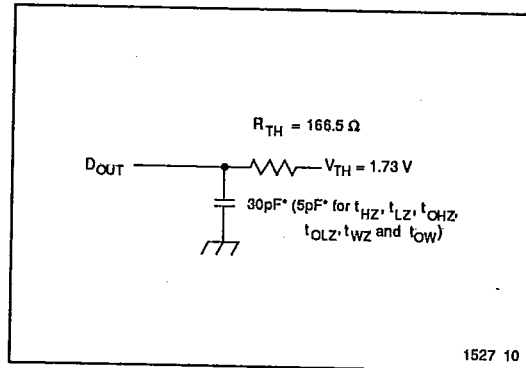
Mode	CE <sub>1</sub>	CE <sub>2</sub>	OE	WE	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D <sub>OUT</sub> Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D <sub>OUT</sub>	Active
Write	L	H	X	L	High Z	Active

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Figure 1. Output Load



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Figure 2. Thevenin Equivalent

\* Including scope and test fixture.

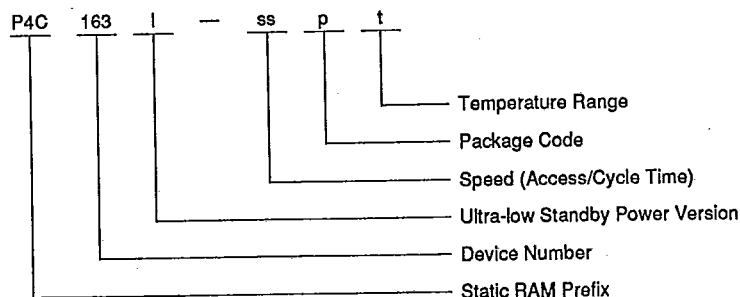
Note:

Due to the ultra-high speed of the P4C163/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V<sub>cc</sub> and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between V<sub>cc</sub> and ground. To

avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D<sub>out</sub> to match 166Ω (Thevenin Resistance).

**ORDERING INFORMATION**

The following part numbering scheme is used for



- L = Ultra-low standby power designator L, if needed.
- ss = Speed (access/cycle time in ns), e.g., 17, 20
- p = Package code, i.e., P, J, C, L.
- t = Temperature range, i.e., C, M, MB.

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**PACKAGE SUFFIX**

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
J	Plastic SOJ, 300 mil wide standard
C	Sidebrazed DIP, 300 mil wide standard
L	Leadless Chip Carrier (ceramic)

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**TEMPERATURE RANGE SUFFIX**

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C – +70°C.
M	Military Temperature Range, –55°C – +125°C.
MB	Mil. Temp. with MIL-STD-883C Class B compliance

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**SELECTION GUIDE**

The P4C163/L is available in the following temperature, speed and package options. The P4C163L is only available with access times of 20 ns and slower for commercial temperatures; 25 ns and slower for military temperatures.

Temp. Range	Package	Speed					
		17	20	25	30	35	45
Com'l	Plastic DIP	-17PC	-20PC	-25PC	-30PC	-35PC	N/A
	Plastic SOJ	-17JC	-20JC	-25JC	-30JC	-35JC	N/A
	Sidebrazed DIP	-17CC	-20CC	-25CC	-30CC	-35CC	N/A
	LCC	-17LC	-20LC	-25LC	-30LC	-35LC	N/A
Mil. Temp.	Sidebrazed DIP	N/A	-20CM	-25CM	-30CM	-35CM	-45CM
	LCC	N/A	-20LM	-25LM	-30LM	-35LM	-45LM
Military Proc'd*	Sidebrazed DIP	N/A	-20CMB	-25CMB	-30CMB	-35CMB	-45CMB
	LCC	N/A	-20LMB	-25LMB	-30LMB	-35LMB	-45LMB

\* Military temperature range with MIL-STD-883 Revision C, Class B processing.  
N/A = Not available

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TECHDOC 1527