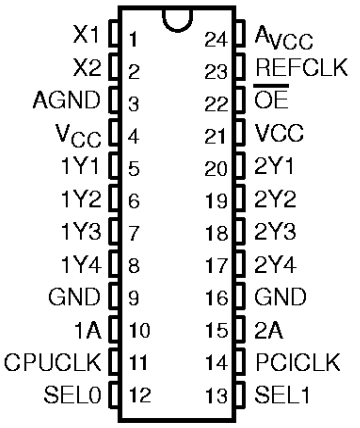
- **Generates Programmable CPU Clock Output (50 MHz, 60 MHz, or 66 MHz)**
- **Generates 33-MHz Clock for Asynchronous PCI**
- **One 14.318-MHz Reference Clock Output**
- **All Output Clock Frequencies Derived From a Single 14.31818-MHz Crystal Input**
- **LVTTL-Compatible Inputs and Outputs**
- **Internal Loop Filters for Phase-Lock Loops Eliminate the Need for External Components**
- **Operates at 3.3-V V_{CC}**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC913 is a high-performance clock generator with integrated dual 1-to-4 buffers, which simplifies clock system design for PC motherboards. The CDC913 consists of a crystal oscillator, two phase-locked loops (PLL), and two 1-to-4 buffers. The CDC913 generates all frequencies using a single 14.318-MHz crystal.

The CPUCLK output is programmable to one of three frequencies (50 MHz, 60 MHz, or 66 MHz) via the SEL0 and SEL1 inputs. PCICLK outputs a 33-MHz clock, independent of the CPUCLK frequency. REFCLK provides a buffered copy of the 14.318-MHz reference. The oscillator and PLLs in the CDC913 are bypassed when in the TEST mode, i.e., SEL1 = SEL0 = H. When in the TEST mode, a test clock can be driven over the X1 input and buffered out from the PCICLK, CPUCLK, and REFCLK outputs.

Outputs 1Yn and 2Yn are 3-state outputs and are enabled via $\overline{OE}$. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled.

Since the CDC913 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at the X1 input, and following any changes to the SELn inputs.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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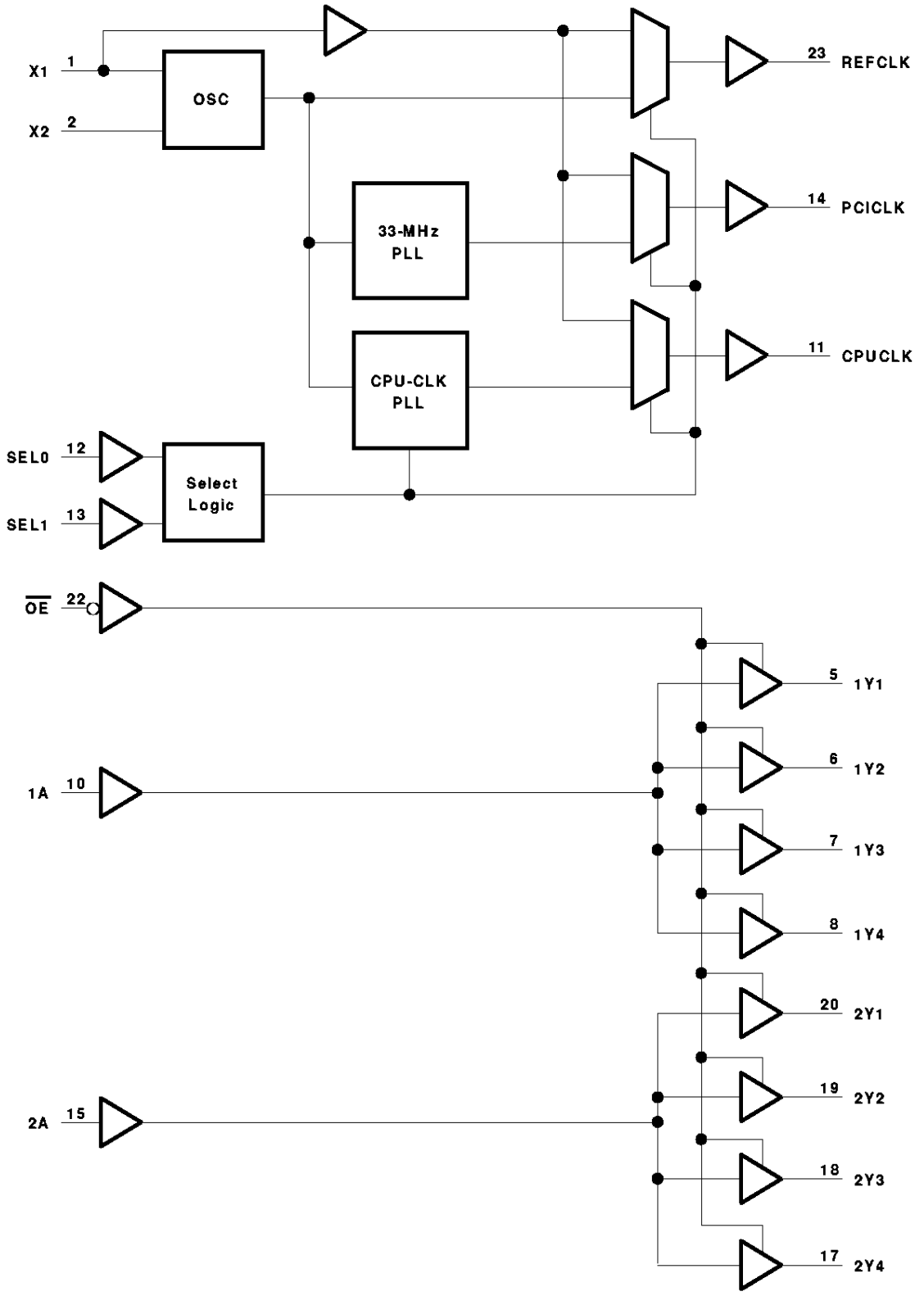
Function Tables

SEL0	SEL1	X1	CPUCLK	PCICLK	REFCLK
L	L	14.318 MHz	50 MHz	33 MHz	14.318 MHz
H	L	14.318 MHz	60 MHz	33 MHz	14.318 MHz
L	H	14.318 MHz	66 MHz	33 MHz	14.318 MHz
H	H	TCLK†	TCLK†	TCLK†	TCLK†

† Test clock (TCLK) is driven over X1 when the CDC913 is in the TEST mode; i.e., SEL1 = SEL0 = H.

$\overline{OE}$	1A	2A	1Yn	2Yn
H	X	X	Hi-Z	Hi-Z
L	L	L	L	L
L	L	H	L	H
L	H	L	H	L
L	H	H	H	H

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 2 × I_{OHmax}
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . . 0.65 W
DW package . . . . . 1.7 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.135	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
I_{OH}	High-level output current	REFCLK		–12	mA
		PCICLK		–6	
		CPUCLK		–6	
		1Yn		–12	
		2Yn		–12	
I_{OL}	Low-level output current	REFCLK		12	mA
		PCICLK		6	
		CPUCLK		6	
		1Yn		12	
		2Yn		12	
T_A	Operating free-air temperature		0	70	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			MIN	TYP†	MAX	UNIT
				MIN	TYP†	MAX				
V_{IK}	V_{CC} = 3.135 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 3.135 V	I_{OH} = –12 mA	REFCLK	2.5			2.4			V
		I_{OH} = –6 mA	PCICLK	2.5			2.4			
		I_{OH} = –6 mA	CPUCLK	2.5			2.4			
		I_{OH} = –12 mA	1Yn	2.5			2.4			
		I_{OH} = –12 mA	2Yn	2.5			2.4			
V_{OL}	V_{CC} = 3.135 V	I_{OL} = 12 mA	REFCLK			0.4			0.5	V
		I_{OL} = 6 mA	PCICLK			0.4			0.5	
		I_{OL} = 6 mA	CPUCLK			0.4			0.5	
		I_{OL} = 12 mA	1Yn			0.4			0.5	
		I_{OL} = 12 mA	2Yn			0.4			0.5	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1			±1	µA
I_{OZ}	V_{CC} = 3.6 V,	V_O = 3 V or 0				±1			±1	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high						1	mA
			Outputs low						1	
			Outputs disabled						1	
C_i	V_I = 3.135 V or 0							6		pF
C_o	V_I = 3.135 V or 0							6		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
Stabilization time‡	After SEL1, SEL0		5	ms
	After power up		5	

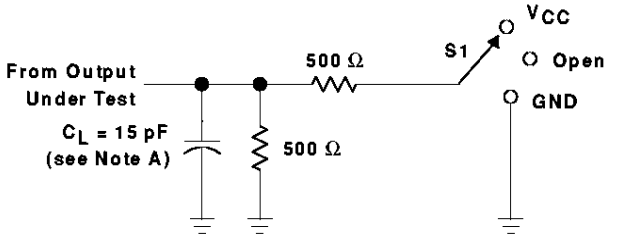
‡ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at X1. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

switching characteristics (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V_{CC} = 3.3 V, T_A = 25°C			V_{CC} = 3.135 V to 3.6 V, T_A = 0°C to 70°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	1A	1Yn		1.5		3.5	1.2	3.8	ns
	2A	2Yn		1.5		3.5	1.2	3.8	
t_{PHL}	1A	1Yn		1.5		3.5	1.2	3.8	ns
	2A	2Yn		1.5		3.5	1.2	3.8	
t_{PZH}	$\overline{OE}$	1Yn		2.5		7	2	7.5	ns
		2Yn		2.5		7	2	7.5	
t_{PZL}	$\overline{OE}$	1Yn		2.5		7	2	7.5	ns
		2Yn		2.5		7	2	7.5	
t_{PHZ}	$\overline{OE}$	1Yn		2.5		7	2	7.5	ns
		2Yn		2.5		7	2	7.5	
t_{PLZ}	$\overline{OE}$	1Yn		2.5		7	2	7.5	ns
		2Yn		2.5		7	2	7.5	
$t_{sk(o)}$		1Yn				350		350	ps
		2Yn				350		350	
		Any Y				500		500	
$t_{sk(p)}$		1Yn and 2Yn				1		1	ns
$Jitter_{(pk-pk)}$†		CPUCLK						±250	ps
		PCICLK						±350	
$t_{c(period)}$†		PCICLK					30		ns
		CPUCLK	SEL0 = L, SEL1 = L				20		
			SEL0 = H, SEL1 = L				16.7		
			SEL0 = L, SEL1 = H				15		
Duty cycle†		CPUCLK					45%	55%	
		PCICLK					45%	55%	
t_r‡								2	ns
t_f‡								2	ns

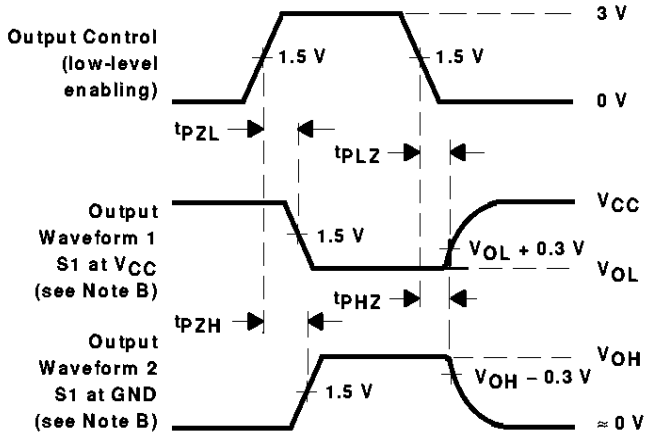
† Specifications are applicable only after the PLL stabilization time has elapsed.
‡ Rise and fall times are characterized using the load circuits shown in Figure 1.

PARAMETER MEASUREMENT INFORMATION

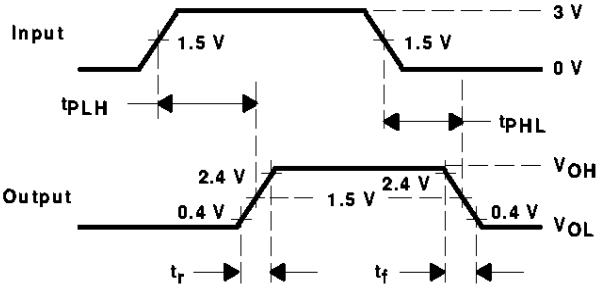


TEST	S1
t_{PLH} /t_{PHL}	Open
t_{PLZ} /t_{PZL}	2X V_{CC}
t_{PHZ} /t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS

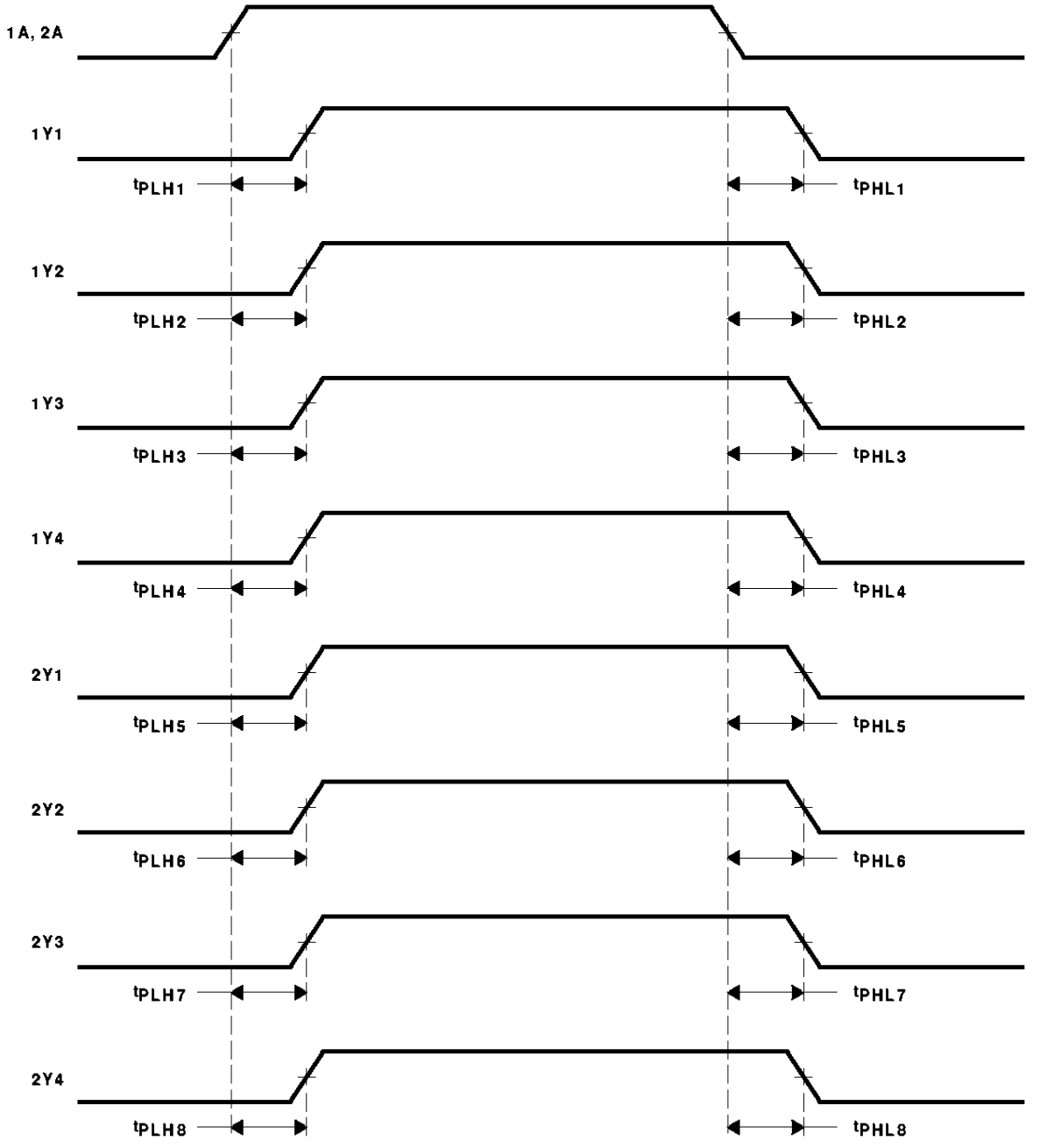


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8).
The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 8).
Pulse skew, tsk(p), is calculated as the greater of | tPLHn – tPLHn | (n = 1, 2, . . . , 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(p)}$

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