2.5V Drive Nch MOSFET

2SK3018UB

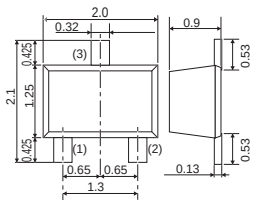
● Structure
Silicon N-channel MOSFET

● Features
1) Low on-resistance.
2) Low voltage drive(2.5V drive).

● Application
Switching

● Dimensions (Unit : mm)

UMT3F

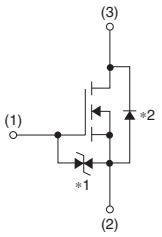


Abbreviated symbol : KN

● Packaging specifications

Type	Package	Taping
	Code	TCL
	Basic ordering unit (pieces)	3000
2SK3018UB		O

● Inner circuit



(1) Gate
(2) Source
(3) Drain

*1 ESD PROTECTION DIODE
*2 BODY DIODE

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±100	mA
	Pulsed	I_{DP} *1	±400	mA
Power dissipation		P_D *2	200	mW
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Each terminal mounted on a recommended land.

● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-a)*	625	°C / W

* Each terminal mounted on a recommended land.

● **Electrical characteristics** (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±1	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	I_D=10μA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	0.8	-	1.5	V	V_{DS}=3V, I_D=100μA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	5	8	Ω	I_D=10mA, V_{GS}=4V
		-	7	13		I_D=1mA, V_{GS}=2.5V
Forward transfer admittance	$\|Y_{fs}\|$*	20	-	-	mS	V_{DS}=3V, I_D=10mA
Input capacitance	C_{iss}	-	13	-	pF	V_{DS}=5V
Output capacitance	C_{oss}	-	9	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	4	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	15	-	ns	V_{DD}≒5V, I_D=10mA
Rise time	t_r *	-	35	-	ns	V_{GS}=5V
Turn-off delay time	$t_{d(off)}$*	-	80	-	ns	R_L=500Ω
Fall time	t_f *	-	80	-	ns	R_G=10Ω

*Pulsed

● Electrical characteristic curves

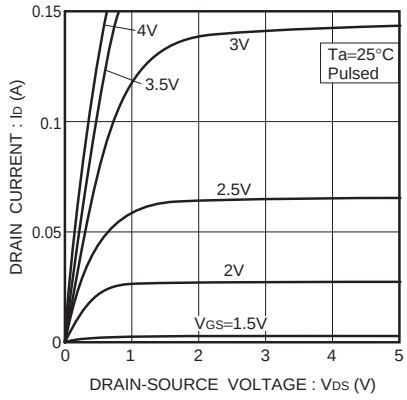


Fig.1 Typical output characteristics

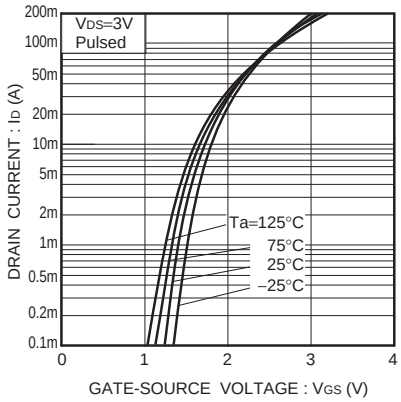


Fig.2 Typical transfer characteristics

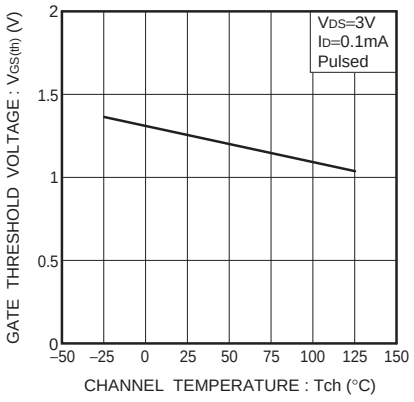


Fig.3 Gate threshold voltage vs. channel temperature

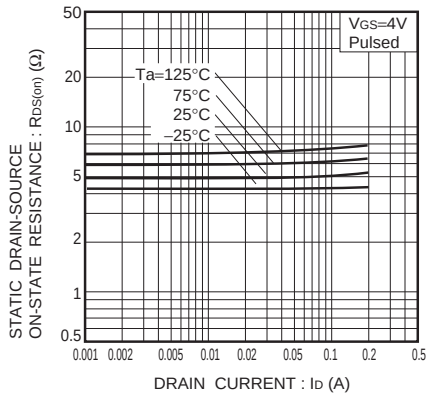


Fig.4 Static drain-source on-state resistance vs. drain current (I)

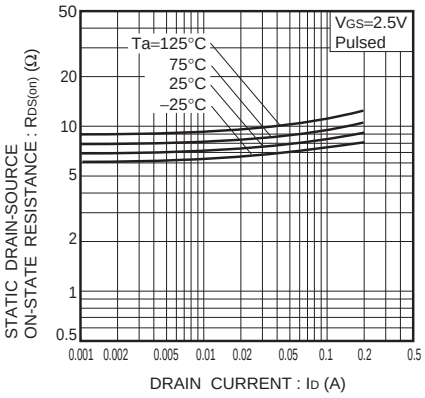


Fig.5 Static drain-source on-state resistance vs. drain current (II)

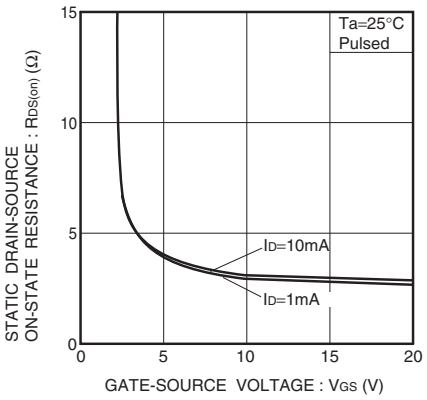


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

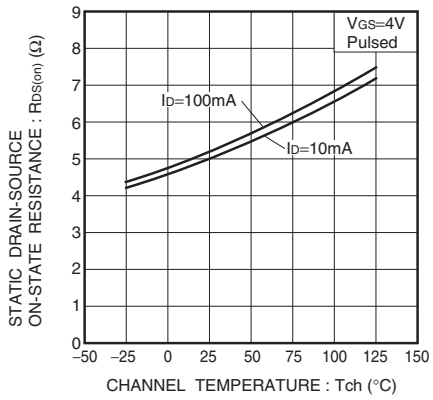


Fig.7 Static drain-source on-state resistance vs. channel temperature

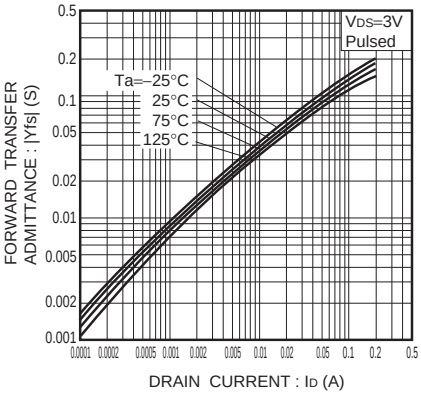


Fig.8 Forward transfer admittance vs. drain current

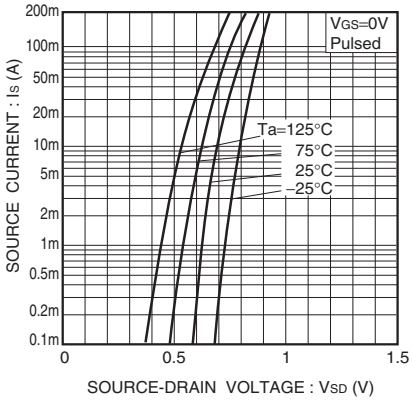


Fig.9 Reverse drain current vs. source-drain voltage (I)

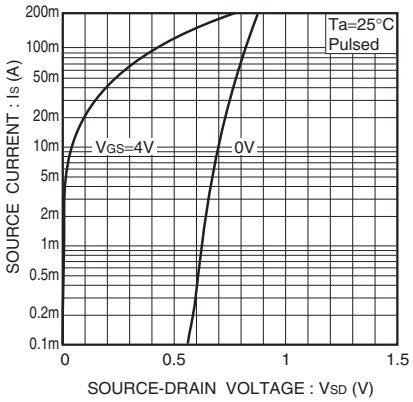


Fig.10 Reverse drain current vs. source-drain voltage (II)

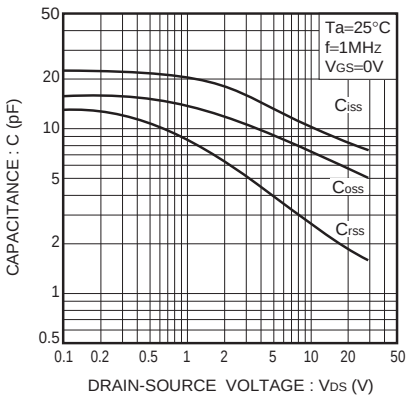


Fig.11 Typical capacitance vs. drain-source voltage

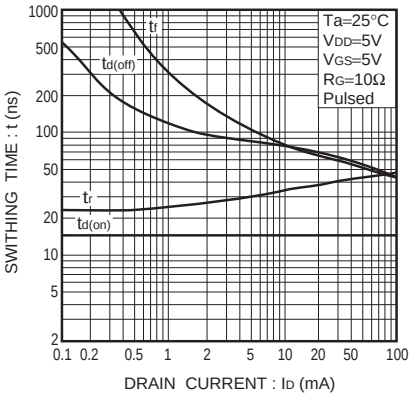


Fig.12 Switching characteristics

● Measurement circuits

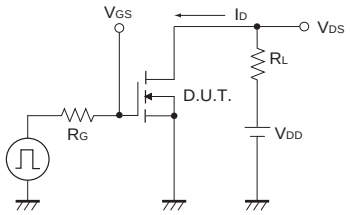


Fig.1-1 Switching Time Measurement Circuit

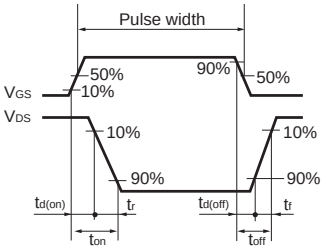


Fig.1-2 Switching Waveforms

● Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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