High Speed LDO Regulator with Inrush Current Prevention

FEATURES

- Operating Voltage Range 1.7 V – 5.5 V
- Output Voltage Range from 1.2 V to 3.6 V with 0.05 V increments
- Output Voltage Accuracy ±1%
- Output Current up to 200 mA
- Dropout Voltage 240 mV @ 200 mA
- Low Power Consumption at 45 µA typical
- Standby Current less than 0.1 µA typical
- Ripple Rejection 75 dB at 1 kHz
- Load Capacitor Auto Discharge
- Current Limit and Short Circuit Protection
- Low ESR Ceramic Capacitor compatible
- Operating Ambient Temperature - 40 + 85^{0}C
- Packages : SOT-25, SSOT-24, and USP-4
- EU RoHS Compliant, Pb Free

APPLICATIONS

- Mobile phones
- Cameras, VCRs
- Various portable equipment
- Reference voltage source

DESCRIPTION

The IXD1233 is a 200 mA highly precise, high speed, low dropout voltage regulator with 75 dB @ 1 kHz ripple rejection. They consist of a voltage reference, an error amplifier, a current limiter with inrush current prevention, a phase compensation circuit, and a driver transistor.

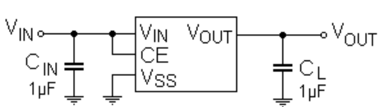
Output voltage is selectable in 0.05V increments within a range of 1.2 V ~ 3.6 V with ± 1% accuracy.

The IXD1233 regulators are compatible with low ESR ceramic capacitors, and due to excellent transient response, they maintain stability even during significant load fluctuations. The current limiter's foldback circuit also operates as short circuit protection.

The chip enable (CE) function allows for disabling the IC, greatly reducing power consumption and simultaneously discharging the load capacitor to prevent load malfunction.

This regulator is available in SOT-25, SSOT-24, and USP-4 packages.

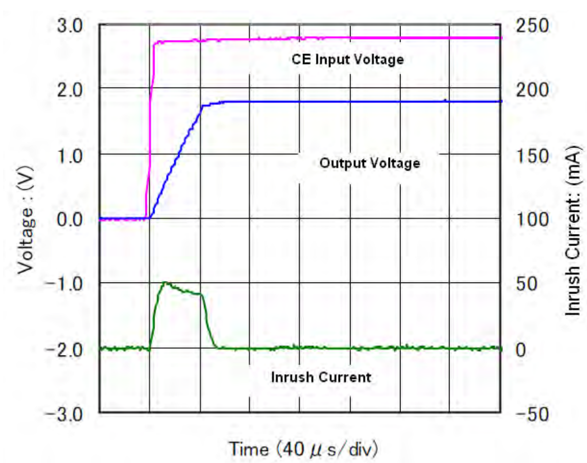
TYPICAL APPLICATION CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTIC

Inrush Current Limit

C_{IN} = C_L = 1.0 µF (ceramic), V_{IN} = 2.8 V, V_{OUT} = 1.8 V, V_{CE} = 0 V → 2.8 V, tr = 5 µs, Ta = 25^{0}C



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	– 0.3 ~ +6.0	V
Output Current		I_{OUT}	275[1)]	mA
Output Voltage		V_{OUT}	– 0.3 ~ V_{IN} + 0.3 or +6.0 V[2)]	V
CE Input Voltage		V_{CE}	– 0.3 ~ +6.0	V
Power Dissipation[2)]	SOT-25	P_D	600 (PCB mounted)	mW
	SSOT-24		500 (PCB mounted)	
	USP-4		1000 (PCB mounted)	
Operating Temperature Range		T_{OPR}	– 40 ~ + 85	^{0}C
Storage Temperature Range		T_{STG}	– 55 ~ +125	^{0}C

All voltages are in respect to V_{SS}

1) $I_{OUT} \le Pd/(V_{IN}-V_{OUT})$
2) The lowest value between V_{IN} + 0.3 and 6.0 V
3) This is a reference data taken by using the test board. Please refer to page 18 to 20 for details

ELECTRICAL OPERATING CHARACTERISTICS

Ta = 25 ^{0}C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
Output Voltage [1)]	$V_{OUT(E)}$	$V_{OUT(T)} \ge 2$ V[3)]	$V_{OUT(T)}$x 0.99	$V_{OUT(T)}$*	$V_{OUT(T)}$x 1.01	V	①
		$V_{OUT(T)} < 2$ V[3)]	$V_{OUT(T)}$- 0.02	$V_{OUT(T)}$*	$V_{OUT(T)}$+ 0.02		
Maximum Output Current	I_{OUT_MAX}		200			mA	①
Load Regulation	ΔV_{OUT}	0.1 mA ≤ I_{OUT} ≤ 200 mA		25	45	mV	①
Dropout Voltage[2)]	V_{DIF1}	I_{OUT} = 200 mA		E-1[4)]		mV	①
Supply Current	I_{SS}	I_{OUT} = 0 mA		45	87	μA	②
Standby Current	I_{STB}	V_{CE} = 0 V		0.01	0.10	μA	②
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} * \Delta V_{IN}}$	I_{OUT} = 30 mA, $V_{OUT(T)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, if $V_{OUT(T)}$ ≥ 2 V, or 2.5 V ≤ V_{IN} ≤ 5.5 V		0.02	0.10	%/V	①
Input Voltage	V_{IN}		1.7		5.5	V	①
Output Voltage Temperature Characteristics	$\frac{\Delta V_{OUT}}{V_{OUT} * \Delta T_{OPR}}$	I_{OUT} = 30 mA - 40 ^{0}C ≤ T_{OPR} ≤ 85 ^{0}C		± 80		ppm/^{0}C	①
Power Supply Rejection Ratio	PSRR	V_{IN} = ($V_{OUT(T)}$ + 1.0 V) + 1 Vp-p_{AC};, when $V_{OUT(T)}$ < 2.5 V, V_{IN} = 3.0 V + 0.5 Vp-p_{AC}, V_{CE} = $V_{OUT(T)}$ + 1.0 V, I_{OUT} = 30 mA, f = 1 kHz		75		dB	③
Current Limit	I_{LIM}			200	255	mA	①
Short Current	I_{SHORT}	V_{OUT} = V_{SS}		60		mA	①
CE "H" Level Voltage	V_{CEH}		0.9		V_{IN}	V	①
CE "L" Level Voltage	V_{CEL}				0.3	V	①
CE "H" Level Current	I_{CEH}	V_{CE} = V_{IN} = 5.5 V	2.5	6.0	9.5	μA	①
CE "L" Level Current	I_{CEL}	V_{CE} = V_{SS}	-0.1		0.1	μA	①
C_L Discharge Resistance	R_{DCH}	V_{IN} = 5.5 V, V_{CE} = 0 V, V_{OUT} = 2 V		270		Ω	①
Inrush Current	I_R	V_{IN} = 5.5 V, V_{CE} = 0 V → 5.5 V		95		mA	④

NOTE:

Unless otherwise stated, $V_{IN} = V_{CE} = V_{OUT\,(T)}$ +1.0 V. I_{OUT} = 1 mA

1) $V_{OUT\,(T)}$ is Nominal output voltage and $V_{OUT\,(E)}$ is Effective output voltage, (I.e. the output voltage when "$V_{OUT\,(T)}$ +1.0V" is provided at the V_{IN} pin, while maintaining a certain I_{OUT} value).
2) V_{DIF} = {V_{IN}-V_{OUT}}, where V_{IN1} is the input voltage when V_{OUT} = 0.98 $V_{OUT(T)}$ appears, while input voltage gradually decreases
3) Refer to the Table "Voltage Chart. Output Voltage"
4) Refer to the Table "Voltage Chart, Dropout Voltage"

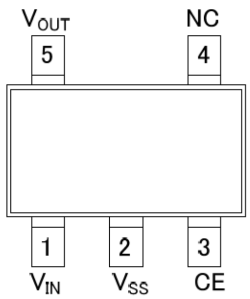
ELECTRICAL OPERATING CHARACTERISTICS (CONTINUED)

Voltage Chart

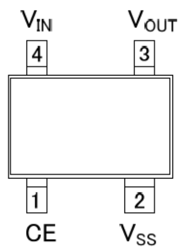
NOMINAL OUTPUT VOLTAGE	E-0		E-1	
	Output Voltage		Dropout Voltage	
	$V_{OUT(E)}$, V		V_{DIF}, V	
$V_{OUT(T)}$, V	MIN	MAX	MIN	MAX
1.20	1.1800	1.2200	680	950
1.25	1.2300	1.2700		
1.30	1.2800	1.3200	640	800
1.35	1.3300	1.3700		
1.40	1.3800	1.4200	600	695
1.45	1.4300	1.4700		
1.50	1.4800	1.5200		
1.55	1.5300	1.5700		
1.60	1.5800	1.6200	510	630
1.65	1.6300	1.6700		
1.70	1.6800	1.7200		
1.75	1.7300	1.7700		
1.80	1.7800	1.8200	400	600
1.85	1.8300	1.8700		
1.90	1.8800	1.9200		
1.95	1.9300	1.9700		
2.00	1.9800	2.0200	375	520
2.05	2.0295	2.0705		
2.10	2.0790	2.1210		
2.15	2.1285	2.1715		
2.20	2.1780	2.2220		
2.25	2.2275	2.2725		
2.30	2.2770	2.3230		
2.35	2.3265	2.3735		
2.40	2.3760	2.4240		
2.45	2.4255	2.4745		

NOMINAL OUTPUT VOLTAGE	E-0		E-1	
	Output Voltage		Dropout Voltage	
	$V_{OUT(E)}$, V		V_{DIF}, V	
$V_{OUT(T)}$, V	MIN	MAX	MIN	MAX
2.50	2.4750	2.5250	310	420
2.55	2.5245	2.5755		
2.60	2.5740	2.6260		
2.65	2.6235	2.6765		
2.70	2.6730	2.7270		
2.75	2.7225	2.7775		
2.80	2.7720	2.8280		
2.85	2.8215	2.8785		
2.90	2.8710	2.9290		
2.95	2.9205	2.9795		
3.00	2.9700	3.0300	240	380
3.05	3.0195	3.0805		
3.10	3.0690	3.1310		
3.15	3.1185	3.1815		
3.20	3.1680	3.2320		
3.25	3.2175	3.2825		
3.30	3.2670	3.3330		
3.35	3.3165	3.3835		
3.40	3.3660	3.4340		
3.45	3.4155	3.4845		
3.50	3.4650	3.5350		
3.55	3.5145	3.5855		
3.60	3.5640	3.6360		

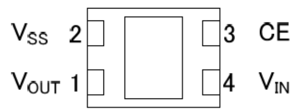
PIN CONFIGURATION



SOT-25 (TOP VIEW)



SSOT-24 (TOP VIEW)



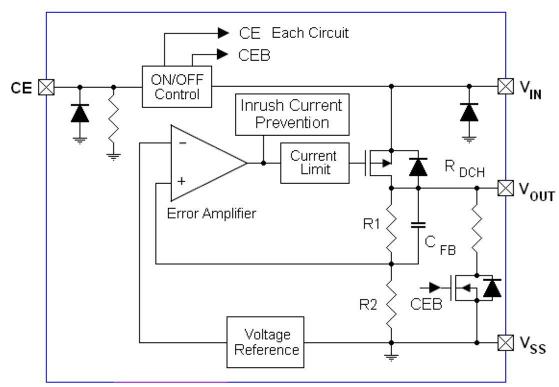
USP-4 (BOTTOM VIEW)

*The dissipation pad for the USP-3 package should be solder-plated in recommended mounting pattern and metal masking to enhance mounting strength and heat release.
If the pad needs to be connected to other pins, it should be connected to the V_{SS} (No.2) pin.

PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTIONS
SOT-25	SSOT-24	USP-4		
1	4	4	V_{IN}	Power Input
2	2	2	V_{SS}	Ground
3	1	3	CE	ON/OFF Control LOW or OPEN – Standby mode, HIGH - Active
4	-	-	NC	No Connection
5	3	1	V_{OUT}	Output Voltage

BLOCK DIAGRAM



IXD1233H

Diodes inside the circuits are ESD protection diodes and parasitic diodes.

BASIC OPERATION

The Error Amplifier of the IXD1233 series monitors output voltage divided by internal resistors R1 & R2 and compares it with the internal Reference Voltage (see Block Diagram above). The output signal from the error amplifier drives the gate of the P-channel MOSFET, which is connected to the V_{OUT} pin and operates as a series voltage regulator.

The Current Limit and Short Protection circuits monitor the level of the output current. The CE pin enables shutdown of internal circuitry to minimize power consumption.

Low ESR Capacitors

An internal phase compensation circuit guarantees stable IXD1233 operation even if output capacitors with low ESR are used. However, connect the output capacitor C_L as close to the V_{OUT} and the V_{SS} pins as possible to prevent effectiveness of the phase compensation from degrading. The C_L capacitance value should be at least 1µF. In case the capacitor depends on the bias and temperature, ensure that actual capacitance is maintained at operating voltage and temperature range. In addition, an input capacitor $C_{IN} \geq 0.1\mu F$ between the V_{IN} and V_{SS} pins should be used to ensure stable input power.

Current Limiter, Short-Circuit Protection

The IXD1233 series includes a combination of a fixed current limiter circuit & a foldback circuit, which aid the operations of the current limiter and circuit protection. When the load current reaches the current limit level, the fixed current limiter circuit activates and output voltage drops. Because of this drop, the foldback circuit activates too, and output voltage drops further decreasing output current. When the output pin is shorted, a current of about 60 mA flows.

CE Pin

The CE pin allows shutdown internal circuitry to minimize power consumption. In shutdown mode, output at the V_{OUT} pin is pulled down to the V_{SS} level via R_{DCH} resistor and N-channel switch.

Note that the IXD1233 CE input is active HIGH with pull down resistor. IC will be in shutdown mode, if CE pin is open.

C_L High-speed Discharge Function

The N-channel transistor located between V_{OUT} and V_{SS} pins quickly discharge the output capacitor (C_L), when the CE pin does low. The discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance R_{DCH} = 270 Ω (TYP.) and the output capacitance (C_L).

Time constant $\tau = C_L \times R_{DCH}$ determines the output voltage after discharge as

$$V = V_{OUT\,(E)} \times e\text{-}t/\tau$$

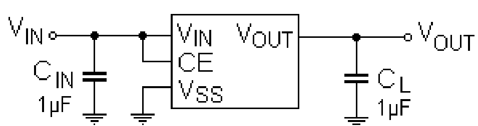
where: $V_{OUT\,(E)}$ - Output voltage, and t - Discharge time
Discharge time can be calculated also by the next formula:

$$t = \tau \times \ln (V_{OUT\,(E)}/V)$$

Inrush Current Prevention

The IXD1233 has a build-in inrush current prevention circuit. When the IC starts to operate, the circuit limits inrush current at 95 mA (TYP.) to charge C_L capacitor. However, the device cannot provide output current above this value for approximately 100 µs because of function of this limiter.

TYPICAL APPLICATION CIRCUIT



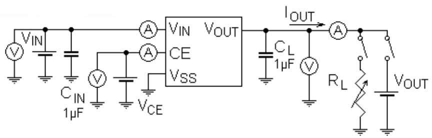
The output capacitor $C_L \geq 1$ µF should be connected between the output pin (V_{OUT}) and the V_{SS} pin for stable regulator's operation.
Ceramic capacitors with low ESR are recommended.

LAYOUT AND USE CONSIDERATIONS

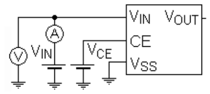
1. Mount the external component as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
2. The IC may malfunction if absolute maximum ratings are exceeded.
3. If power source of this regulator is a high impedance device with impedance of 10 Ω or more, an input capacitor $C_{IN} \geq 1$µF should be used to prevent oscillations.
4. In case of high output current, increasing the input capacitor value can stabilize operations.
5. Oscillations may occur if the input capacitor value is not enough to reduce the input impedance and the output capacitor C_L is large. In this case, operations can be stabilized by either increasing the input capacitor or reducing the output capacitor.
6. During start-up, IC provides constant current until $V_{OUT} = V_{OUT\,(T)}$.
7. Ensure that output current I_{OUT} is less than $P_D / (V_{IN} - V_{OUT})$, where P_D is a rated power dissipation value of the package shown at ABSOLUTE MAXIMUM RATING table to not exceed it.

TEST CIRCUITS

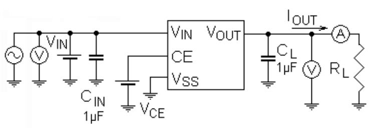
Circuit ①



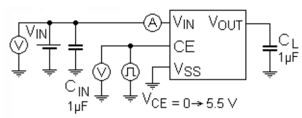
Circuit ②



Circuit ③



Circuit ④

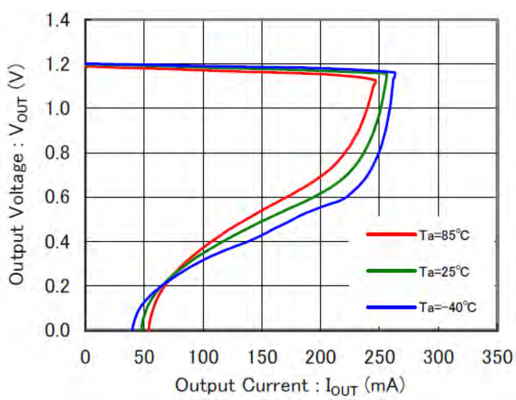


$V_{IN} = V_{OUT} + 1.0\ V_{DC} + 0.5\ Vp\text{-}p_{AC}$, if $V_{OUT} \leq 2.5$ V, $V_{IN} = 3.0\ V_{DC} + 0.5\ Vp\text{-}p_{AC}$

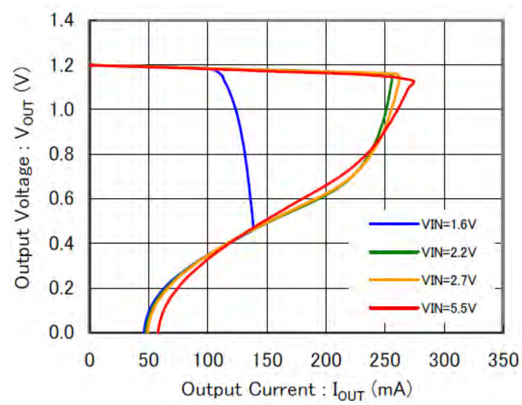
TYPICAL PERFORMANCE CHARACTERISTICS

(1) Output Voltage vs. Output Current

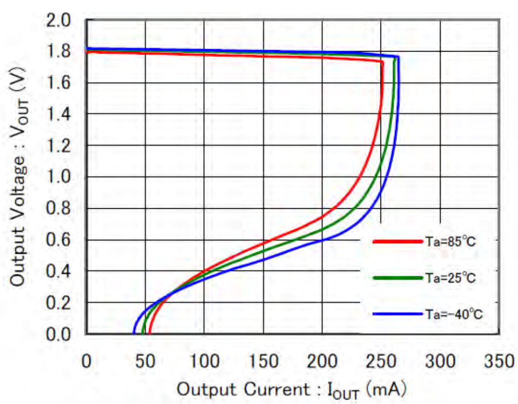
$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 2.2$ V, $V_{OUT} = 1.2$ V



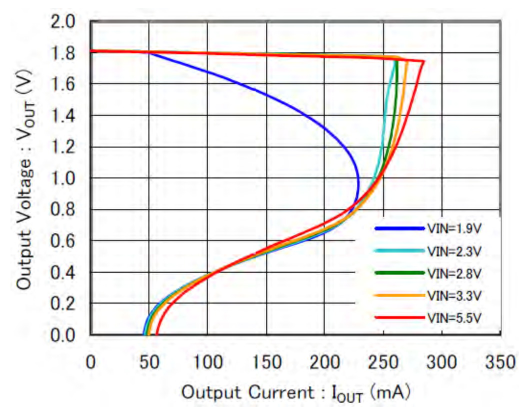
$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 2.2$ V, $V_{OUT} = 1.2$ V, Ta = 25°C



$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 2.8$ V, $V_{OUT} = 1.8$ V



$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 2.8$ V, $V_{OUT} = 1.8$ V, , Ta = 25°C

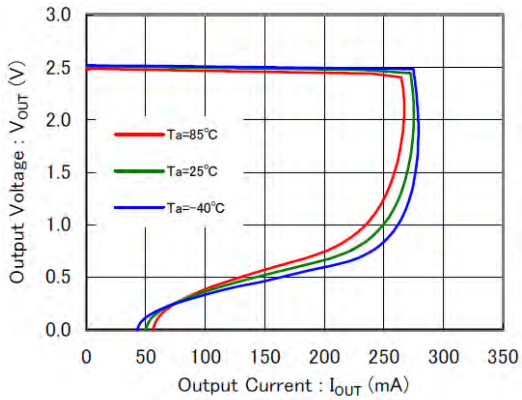


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

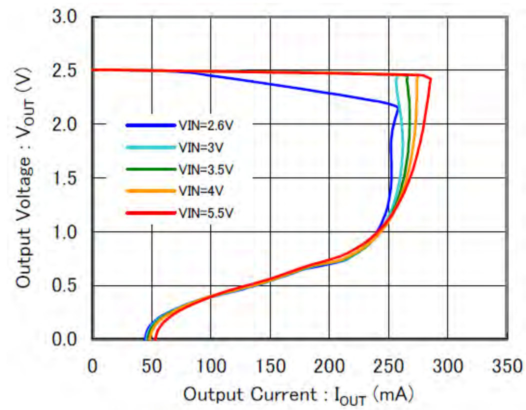
(1) Output Voltage vs Output Current (Continue)

Topr = 25 ⁰C

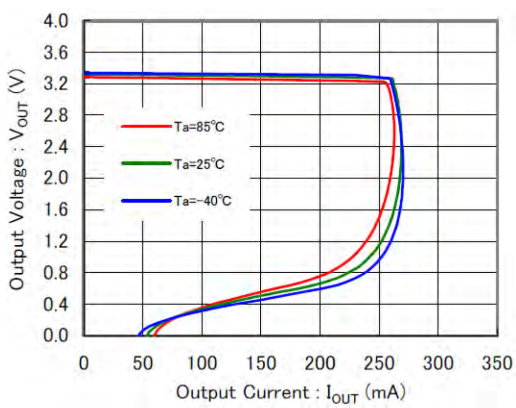
$C_{IN} = C_L$ = 1 µF (ceramic), V_{IN} = 3.5 V, V_{OUT} = 2.5 V



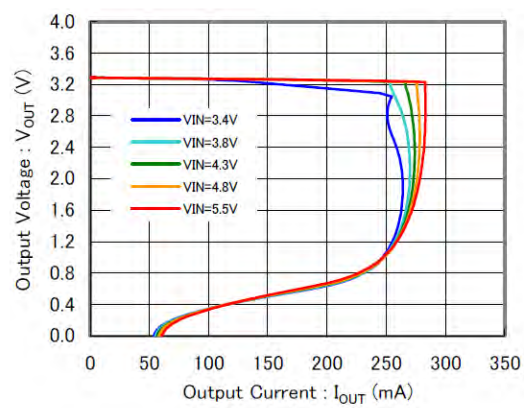
$C_{IN} = C_L$ = 1 µF (ceramic), V_{IN} = 3.5 V, V_{OUT} = 2.5 V, , Ta = 25⁰C



$C_{IN} = C_L$ = 1 µF (ceramic), V_{IN} = 4.3 V, V_{OUT} = 3.3 V

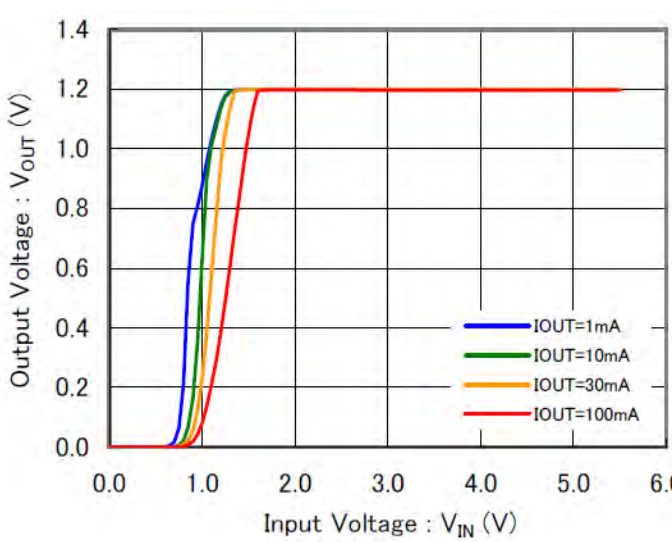


$C_{IN} = C_L$ = 1 µF (ceramic), V_{IN} = 4.3 V, V_{OUT} = 3.3 V, , Ta = 25⁰C

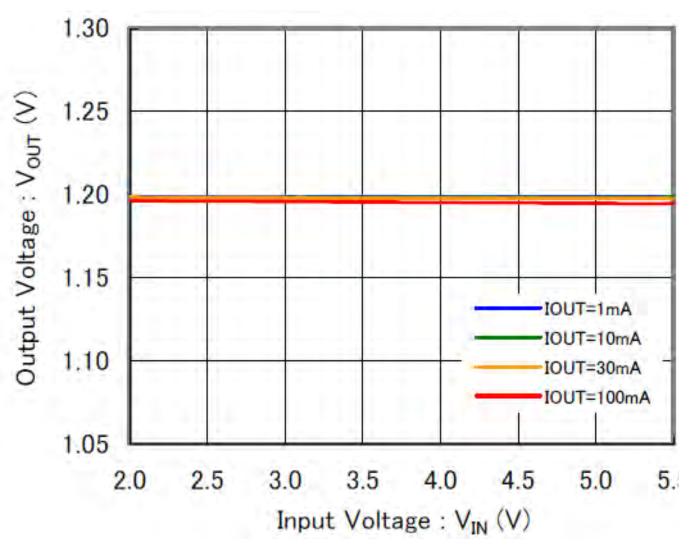


(2) Output Voltage vs. Input Voltage

$C_{IN} = C_L$ = 1 µF (ceramic), V_{OUT} = 1.2 V, Ta = 25⁰C



$C_{IN} = C_L$ = 1 µF (ceramic), V_{OUT} = 1.2 V, Ta = 25⁰C

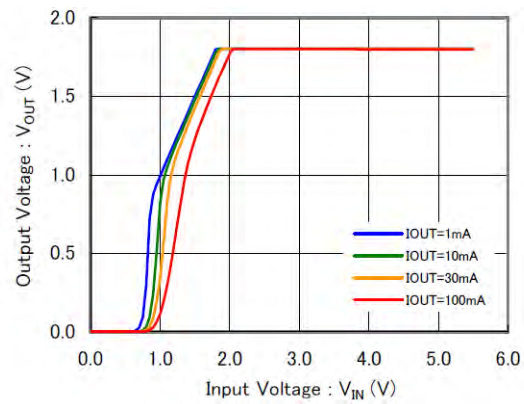


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

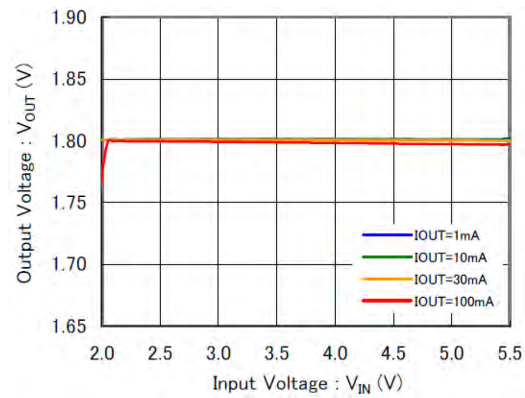
(2) Output Voltage vs. Input Voltage (Continue)

Topr = 25 ⁰C

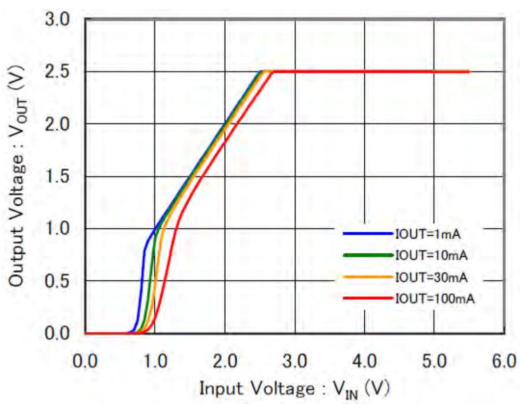
$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 2.8 V, V_{OUT} = 1.8 V



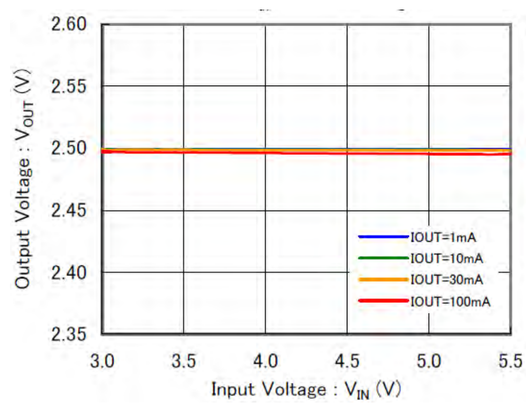
$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 2.8 V, V_{OUT} = 1.8 V, , Ta = 25⁰C



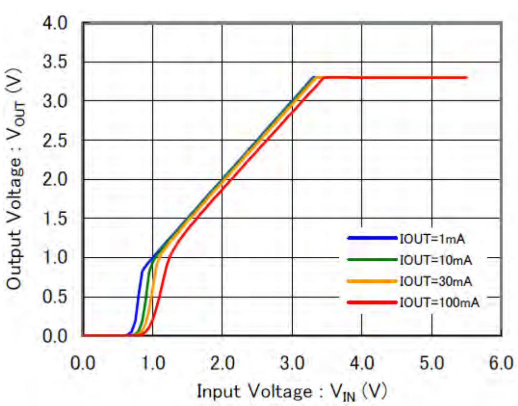
$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 3.5 V, V_{OUT} = 2.5 V



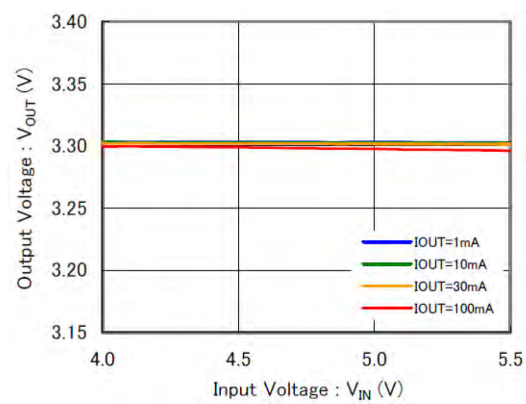
$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 3.5 V, V_{OUT} = 2.5 V, , Ta = 25⁰C



$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 4.3 V, V_{OUT} = 3.3 V



$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 4.3 V, V_{OUT} = 3.3 V, , Ta = 25⁰C

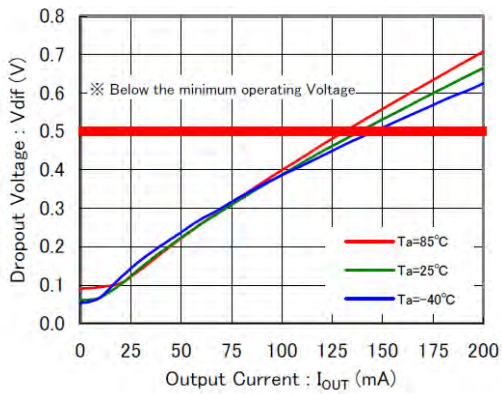


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

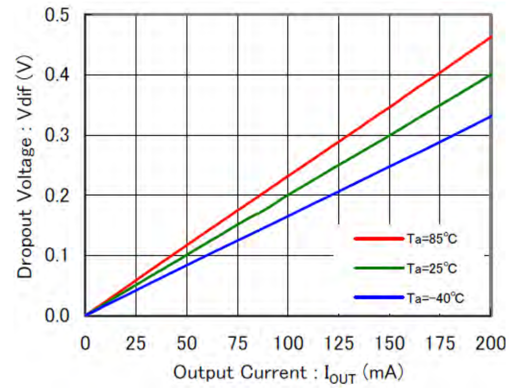
(3) Dropout Voltage vs. Output Current

Topr = 25 ^{0}C

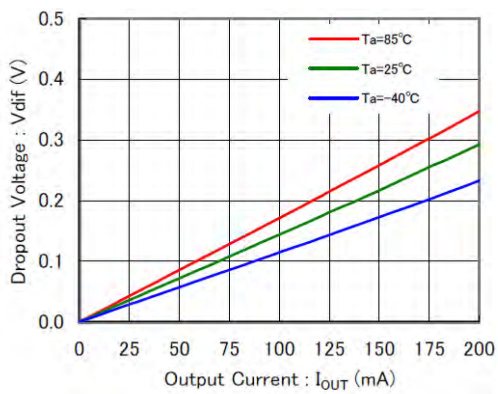
$C_{IN} = C_L = 1$ µF (ceramic), $V_{OUT} = 1.2$ V, Ta = 25^{0}C



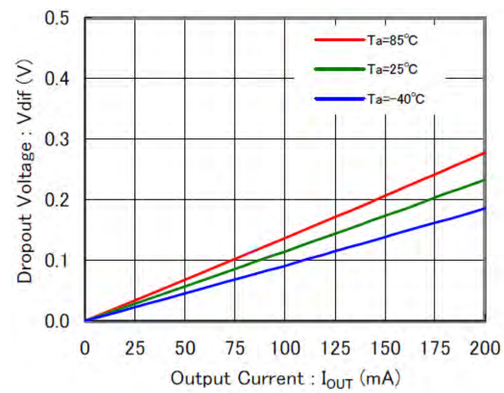
$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 2.8$ V, $V_{OUT} = 1.8$ V, , Ta = 25^{0}C



$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 3.5$ V, $V_{OUT} = 2.5$ V, , Ta = 25^{0}C

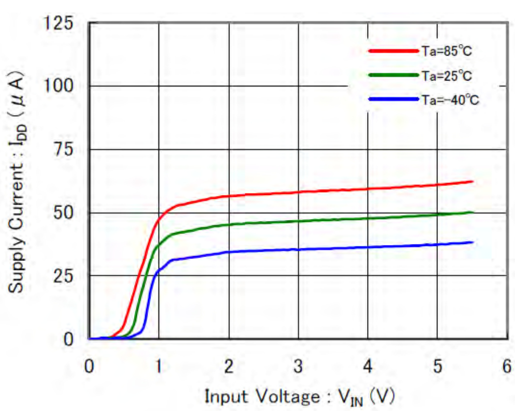


$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 4.3$ V, $V_{OUT} = 3.3$ V, , Ta = 25^{0}C

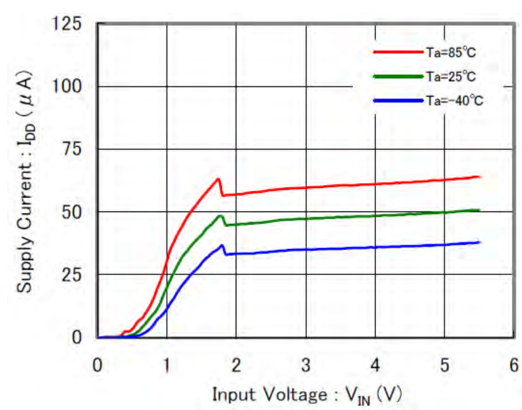


(4) Supply Current vs. Input Voltage

$C_{IN} = C_L = 1$ µF (ceramic), $V_{OUT} = 1.2$ V



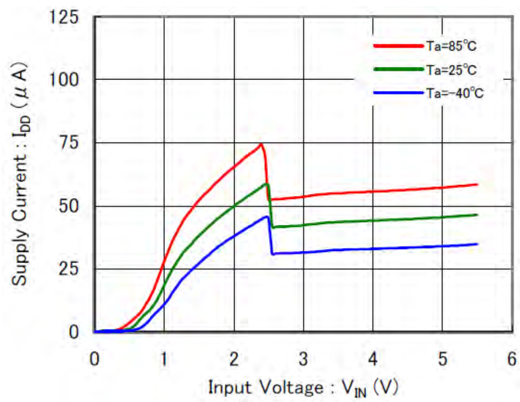
$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = 2.8$ V, $V_{OUT} = 1.8$ V



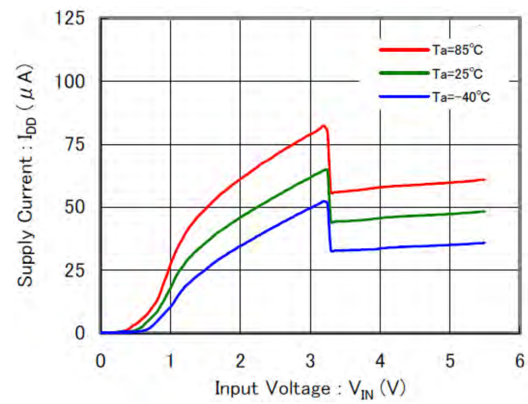
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) Supply Current vs. Input Voltage (Continue)

$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 3.5 V, V_{OUT} = 2.5 V

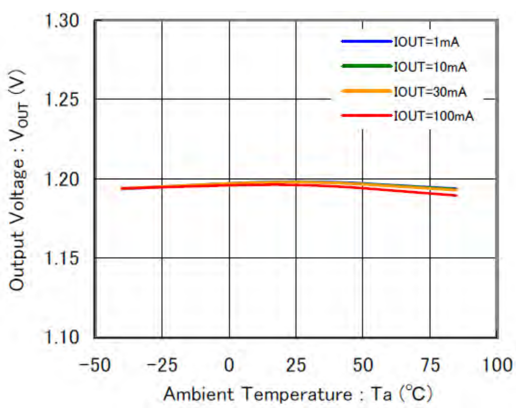


$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 4.3 V, V_{OUT} = 3.3 V,

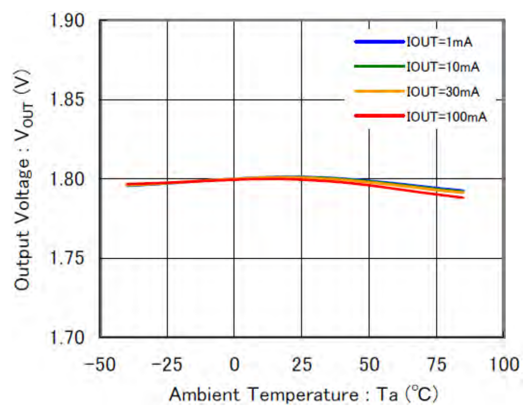


(5) Output Voltage vs. Ambient temperature

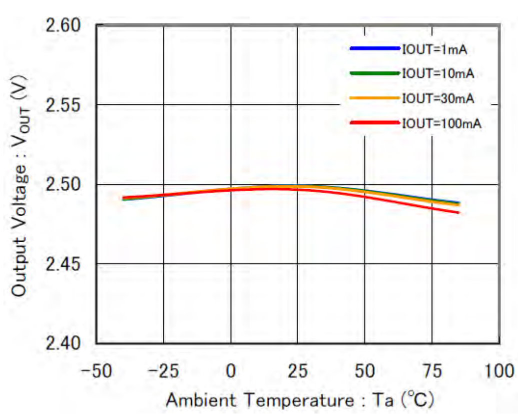
$C_{IN} = C_L$ = 1 μF (ceramic), V_{OUT} = 1.2 V



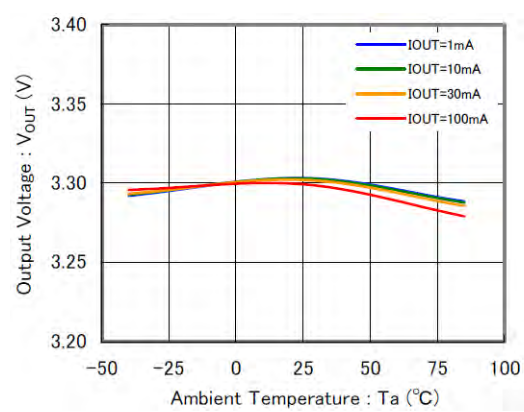
$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 2.8 V, V_{OUT} = 1.8 V



$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 3.5 V, V_{OUT} = 2.5 V



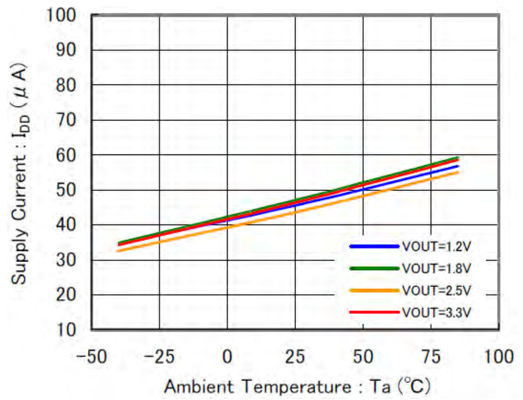
$C_{IN} = C_L$ = 1 μF (ceramic), V_{IN} = 4.3 V, V_{OUT} = 3.3 V,



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

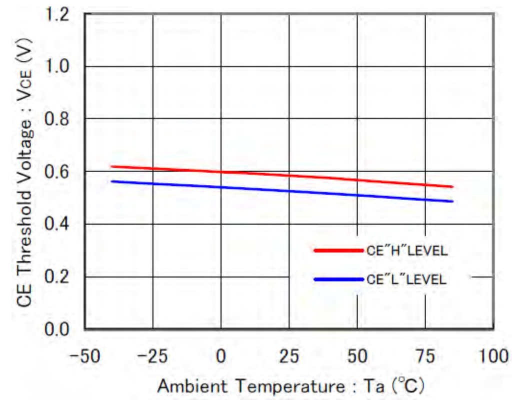
(6) Supply Current vs. Ambient Temperature

$C_{IN} = C_L = 1$ µF (ceramic), $V_{IN} = V_{OUT} + 1.0$ V



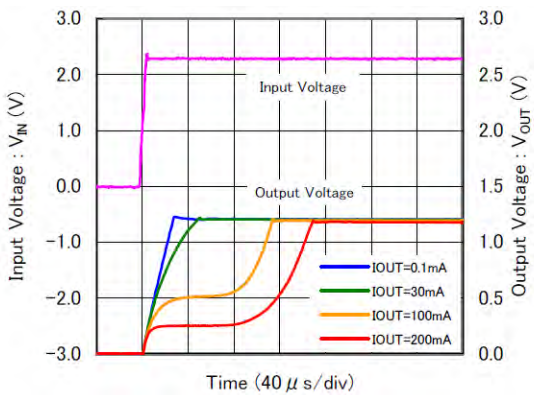
(7) CE Threshold Voltage vs. Ambient Temperature

$C_{IN} = C_L = 1$ µF (ceramic)

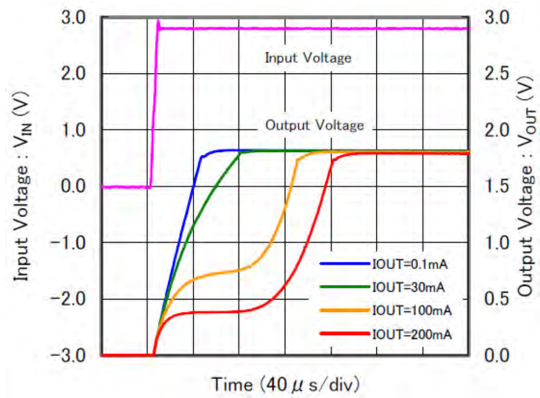


(8) Input Voltage Rising Response Time

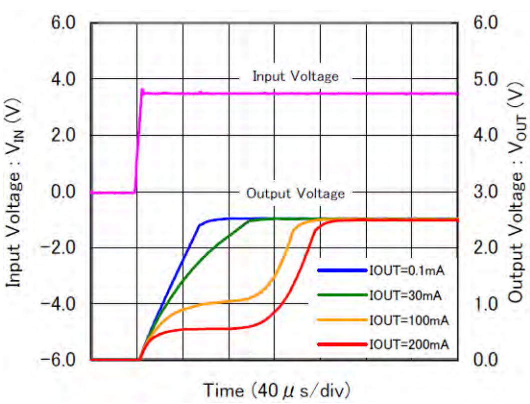
$C_{IN} = C_L = 1$ µF (ceramic), $t_R = 5$ µs, Ta = 25^{0}C, $V_{OUT} = 1.2$ V, $V_{IN} = V_{CE} = 0 \rightarrow 2.2$ V



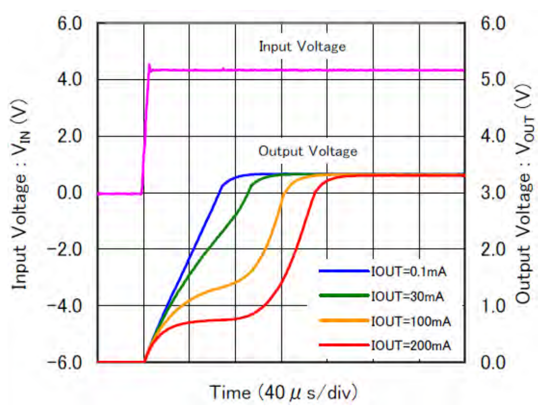
$C_{IN} = C_L = 1$ µF (ceramic), $t_R = 5$ µs, Ta = 25^{0}C, $V_{OUT} = 1.8$ V, $V_{IN} = V_{CE} = 0 \rightarrow 2.8$ V



$C_{IN} = C_L = 1$ µF (ceramic), $t_R = 5$ µs, Ta = 25^{0}C, $V_{OUT} = 2.5$ V, $V_{IN} = V_{CE} = 0 \rightarrow 3.5$ V



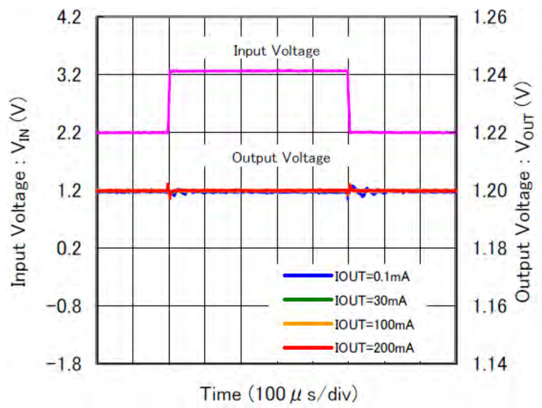
$C_{IN} = C_L = 1$ µF (ceramic), $t_R = 5$ µs, Ta = 25^{0}C, $V_{OUT} = 3.3$ V, $V_{IN} = V_{CE} = 0 \rightarrow 4.3$ V



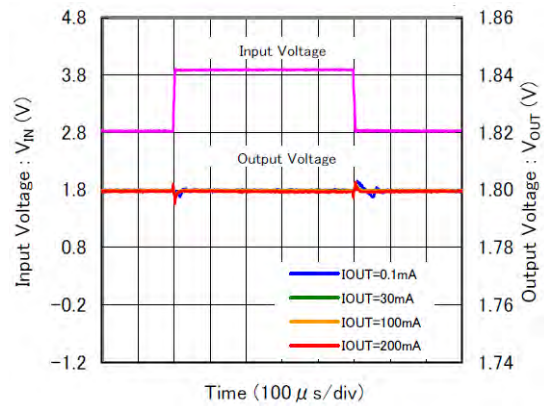
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(9) Input Voltage Transient Response

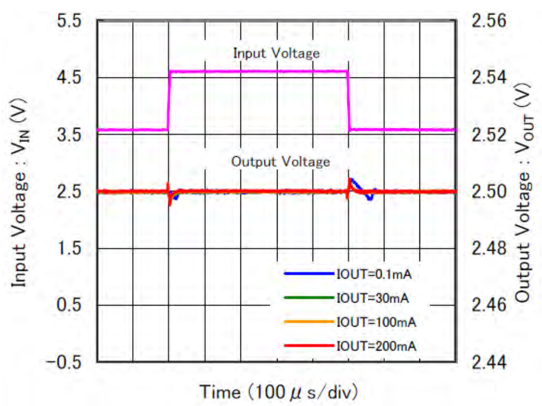
$C_{IN} = C_L = 1$ μF (ceramic), $t_R = t_F = 5$ μs, Ta = 25^{0}C, $V_{OUT} = 1.2$ V, $V_{IN} = 2.2$ V ↔ 3.2 V



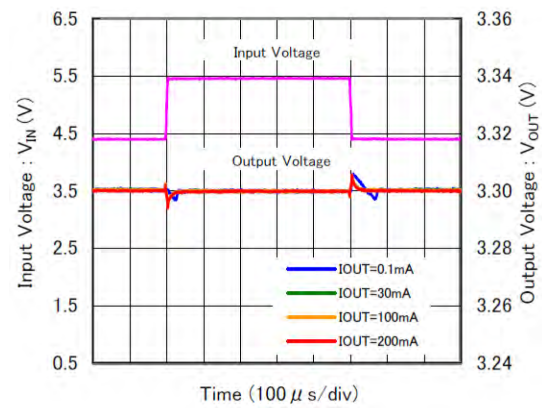
$C_{IN} = C_L = 1$ μF (ceramic), $t_R = t_F = 5$ μs, Ta = 25^{0}C, $V_{OUT} = 1.8$ V, $V_{IN} = 2.8$ V ↔ 3.8 V



$C_{IN} = C_L = 1$ μF (ceramic), $t_R = t_F = 5$ μs, Ta = 25^{0}C, $V_{OUT} = 2.5$ V, $V_{IN} = 3.5$ V ↔ 4.5 V

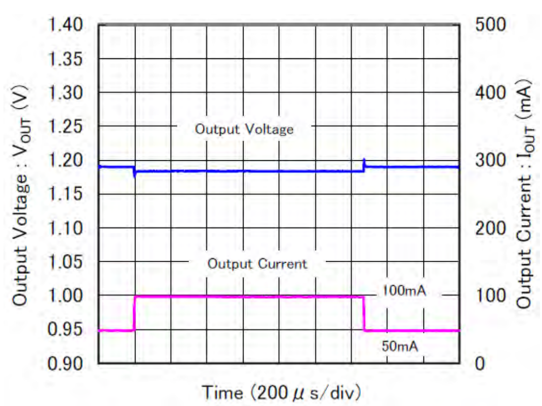


$C_{IN} = C_L = 1$ μF (ceramic), $t_R = t_F = 5$ μs, Ta = 25^{0}C, $V_{OUT} = 3.3$ V, $V_{IN} = 4.3$ V ↔ 5.3 V

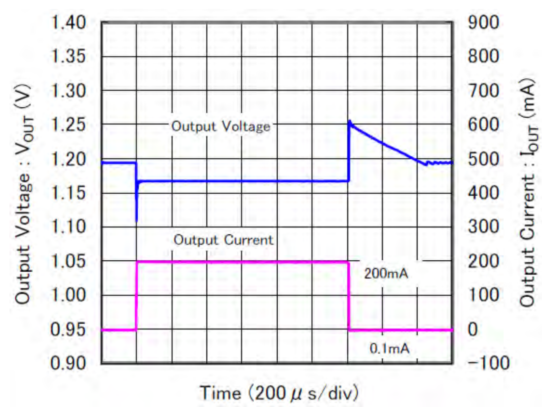


(10) Load Transient Response

$C_{IN} = C_L = 1$ μF (ceramic), $t_R = t_F = 0.5$ μs, Ta = 25^{0}C, $V_{OUT} = 1.2$ V, $V_{IN} = 2.2$ V,
$I_{OUT} = 50$ mA ↔ 100 mA



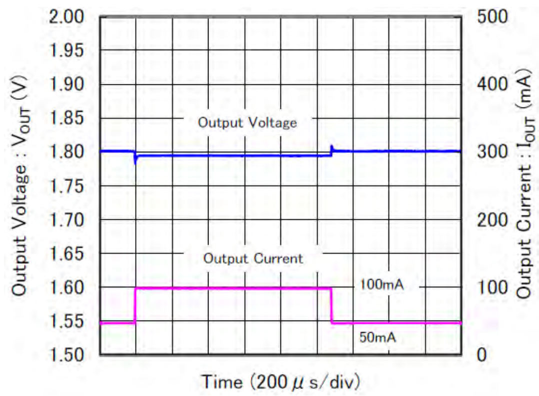
$C_{IN} = C_L = 1$ μF (ceramic), $t_R = t_F = 0.5$ μs, Ta = 25^{0}C, $V_{OUT} = 1.2$ V, $V_{IN} = 2.2$ V,
$I_{OUT} = 0.1$ mA ↔ 200 mA



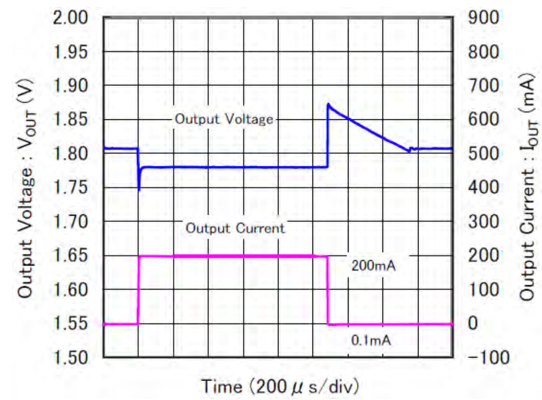
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(10) Load Transient Response (Continued)

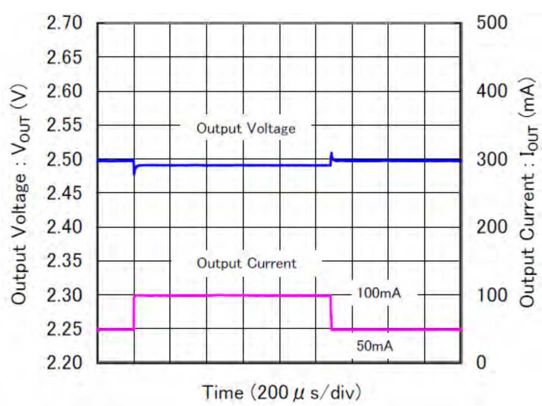
$C_{IN} = C_L$ = 1 µF (ceramic), $t_R = t_F$ = 0.5 µs, Ta = 25^{0}C, V_{OUT} = 1.8 V, V_{IN} = 2.8 V, I_{OUT} = 50 mA ↔ 100 mA



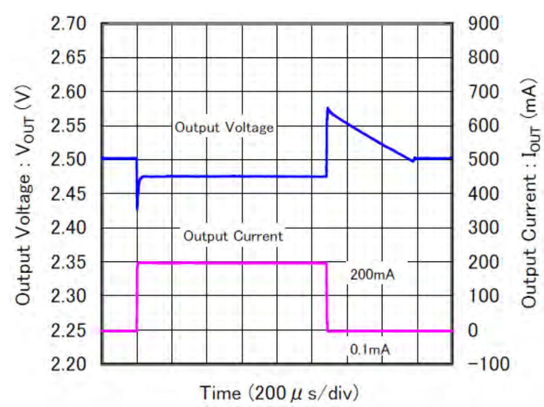
$C_{IN} = C_L$ = 1 µF (ceramic), $t_R = t_F$ = 0.5 µs, Ta = 25^{0}C, V_{OUT} = 1.8 V, V_{IN} = 2.8 V, I_{OUT} = 0.1 mA ↔ 200 mA



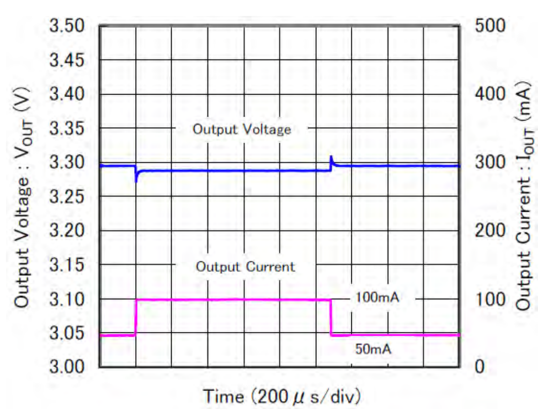
$C_{IN} = C_L$ = 1 µF (ceramic), $t_R = t_F$ = 0.5 µs, Ta = 25^{0}C, V_{OUT} = 2.5 V, V_{IN} = 3.5 V, I_{OUT} = 50 mA ↔ 100 mA



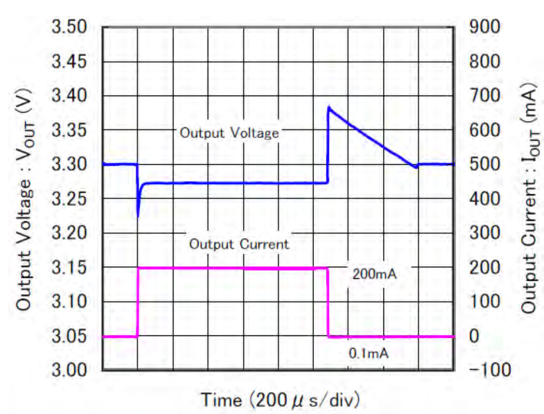
$C_{IN} = C_L$ = 1 µF (ceramic), $t_R = t_F$ = 0.5 µs, Ta = 25^{0}C, V_{OUT} = 2.5 V, V_{IN} = 3.5 V, I_{OUT} = 0.1 mA ↔ 200 mA



$C_{IN} = C_L$ = 1 µF (ceramic), $t_R = t_F$ = 0.5 µs, Ta = 25^{0}C, V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 0.1 mA ↔ 200 mA

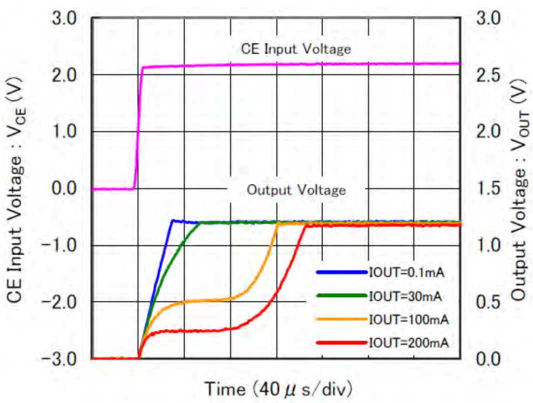


$C_{IN} = C_L$ = 1 µF (ceramic), $t_R = t_F$ = 0.5 µs, Ta = 25^{0}C, V_{OUT} = 3.3 V, V_{IN} = 4.3 V, I_{OUT} = 0.1 mA ↔ 200 mA

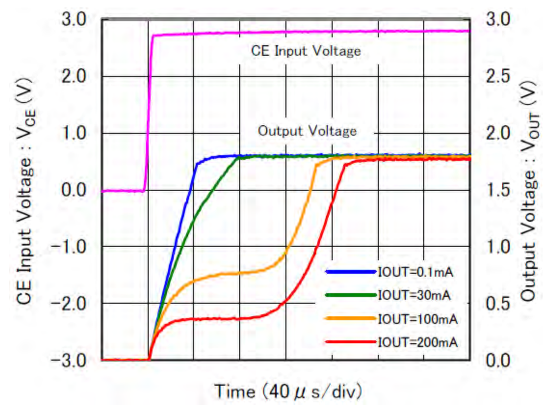


(11) CE Voltage Rising Response Time

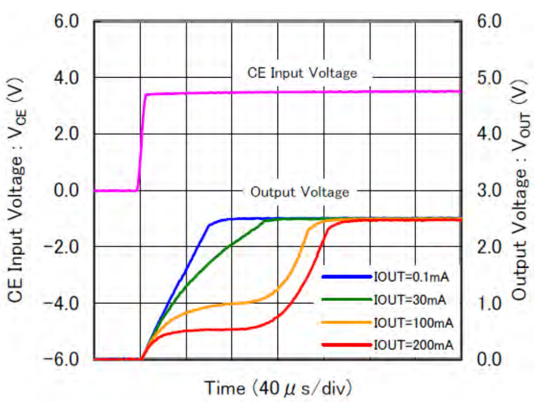
$C_{IN} = C_L = 1\ \mu F$ (ceramic), $t_R = 5\ \mu s$, $Ta = 25^0C$, $V_{OUT} = 1.2\ V$, $V_{IN} = 2.2\ V$, $V_{CE} = 0 \rightarrow 2.2\ V$



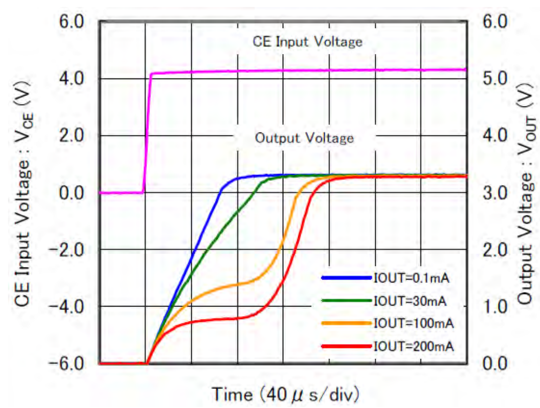
$C_{IN} = C_L = 1\ \mu F$ (ceramic), $t_R = 5\ \mu s$, $Ta = 25^0C$, $V_{OUT} = 1.8\ V$, $V_{IN} = 2.8\ V$, $V_{CE} = 0 \rightarrow 2.8\ V$



$C_{IN} = C_L = 1\ \mu F$ (ceramic), $t_R = 5\ \mu s$, $Ta = 25^0C$, $V_{OUT} = 2{,}5\ V$, $V_{IN} = 3.5\ V$, $V_{CE} = 0 \rightarrow 3.5\ V$

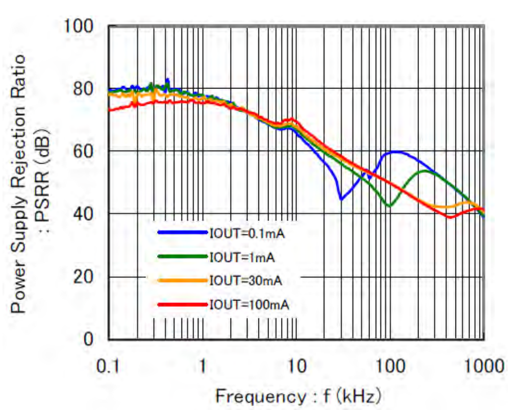


$C_{IN} = C_L = 1\ \mu F$ (ceramic), $t_R = 5\ \mu s$, $Ta = 25^0C$, $V_{OUT} = 3.3\ V$, $V_{IN} = 4.3\ V$, $V_{CE} = 0 \rightarrow 4.3\ V$

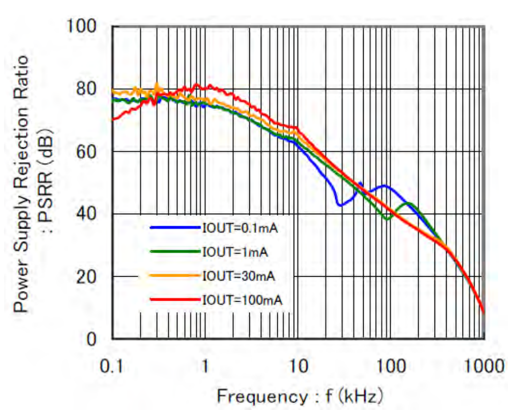


(12) Power Supply Rejection Ratio

$C_{IN} = C_L = 1\ \mu F$ (ceramic), $Ta = 25^0C$, $V_{OUT} = 1.2\ V$, $V_{IN} = 3.0\ V + 0.5\ Vp\text{-}p_{AC}$

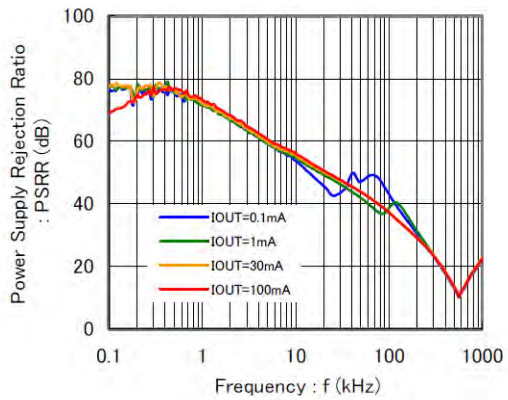


$C_{IN} = C_L = 1\ \mu F$ (ceramic), $Ta = 25^0C$, $V_{OUT} = 1.8\ V$, $V_{IN} = 3.0\ V + 0.5\ Vp\text{-}p_{AC}$

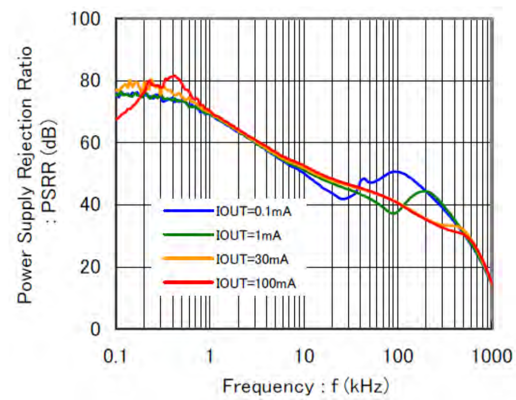


(12) Power Supply Rejection Ratio (Continue)

$C_{IN} = C_L$ = 1 µF (ceramic), Ta = 25^{0}C, V_{OUT} = 2.5 V, V_{IN} = 3.5 V + 0.5 Vp-p_{AC}

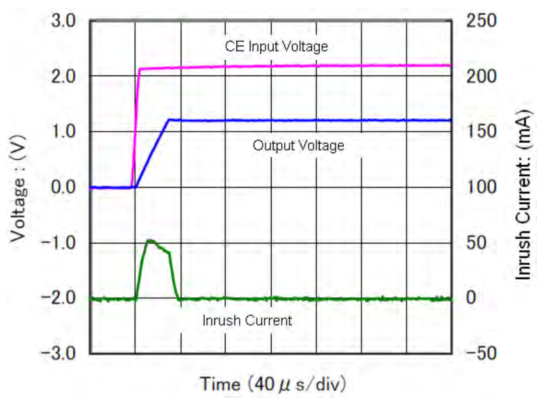


$C_{IN} = C_L$ = 1 µF (ceramic), Ta = 25^{0}C, V_{OUT} = 3.3 V, V_{IN} = 4.3 V + 0.5 Vp-p_{AC}

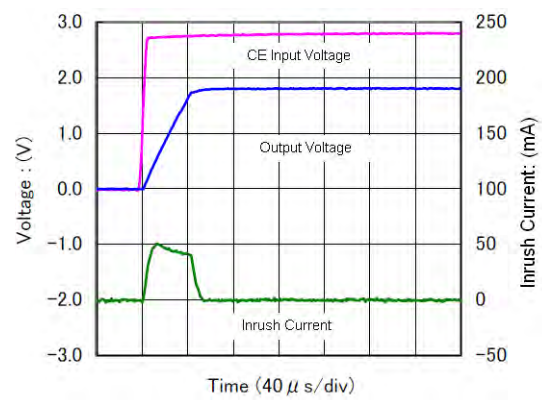


(13) Inrush Current Response

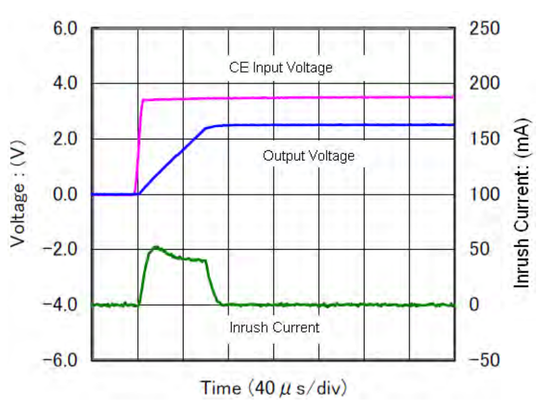
$C_{IN} = C_L$ = 1 µF (ceramic), t_R = 5 µs, Ta = 25^{0}C, V_{OUT} = 1.2 V, V_{IN} = 2.2 V, V_{CE} = 0 → 2.2 V



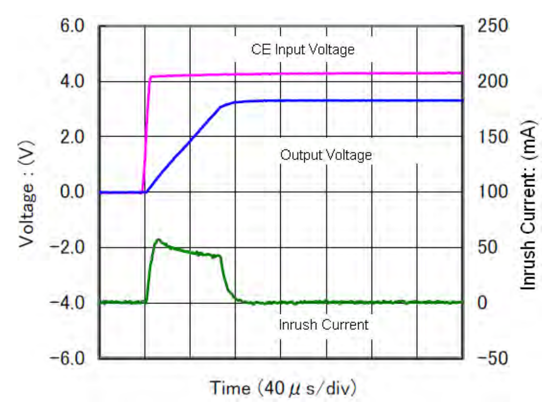
$C_{IN} = C_L$ = 1 µF (ceramic), t_R = 5 µs, Ta = 25^{0}C, V_{OUT} = 1.8 V, V_{IN} = 2.8 V, V_{CE} = 0 → 2.8 V



$C_{IN} = C_L$ = 1 µF (ceramic), t_R = 5 µs, Ta = 25^{0}C, V_{OUT} = 2.5 V, V_{IN} = 3.5 V, V_{CE} = 0 → 3.5 V

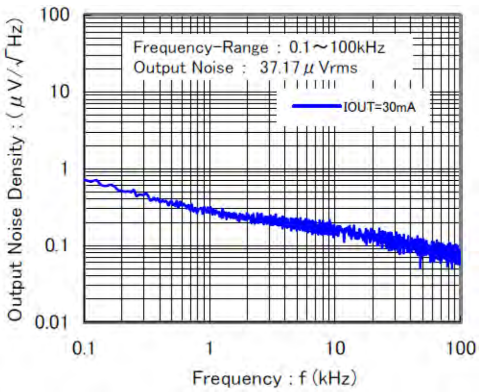


$C_{IN} = C_L$ = 1 µF (ceramic), t_R = 5 µs, Ta = 25^{0}C, V_{OUT} = 3.3 V, V_{IN} = 4.3 V, V_{CE} = 0 → 4.3 V

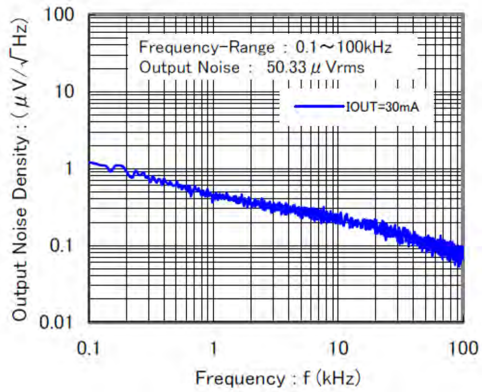


(14) Output Noise Density

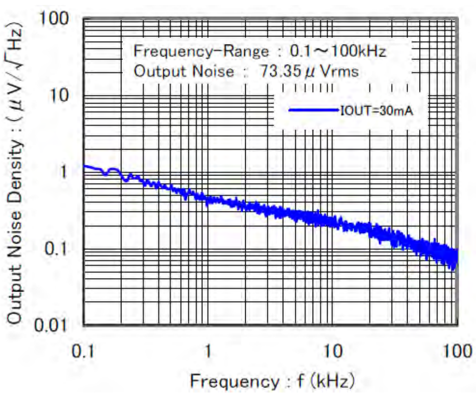
$C_{IN} = C_L$ = 1 μF (ceramic), Ta = 25°C, V_{OUT} = 1.2 V, V_{IN} = 2.2 V



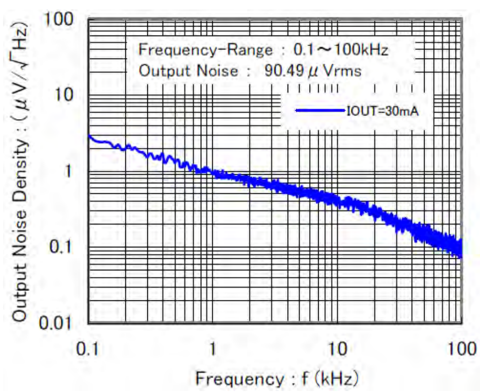
$C_{IN} = C_L$ = 1 μF (ceramic), Ta = 25°C, V_{OUT} = 1.8 V, V_{IN} = 2.8 V



$C_{IN} = C_L$ = 1 μF (ceramic), Ta = 25°C, V_{OUT} = 2.5 V, V_{IN} = 3.5 V



$C_{IN} = C_L$ = 1 μF (ceramic), Ta = 25°C, V_{OUT} = 3.3 V, V_{IN} = 4.3 V



ORDERING INFORMATION

IXD1233①②③④⑤⑥-⑦

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Type of Regulator	H	CE Pull-down, Current Limiter, C_L Auto Discharge, Inrush Current Prevention
②③	Output Voltage[1)]	12 - 36	Output Voltage Range: 0.9 V～6.0 V, e.g. 2.6 V - ② = 2, ③ = 6
④	Output Voltage Accuracy	1	0.10 V increments, Accuracy: ±1%, (V_{OUT} ≥ 2 V) or ± 0.02 V (V_{OUT} < 2 V), e.g. 2.60 V - ② = 2, ③ = 6, ④ = 1
		B	0.05 V increments, Accuracy: ±1%, (V_{OUT} ≥ 2.05 V) or ± 0.02 V (V_{OUT} < 2.05 V), e.g. 2.65 V - ② = 2, ③ = 6, ④ = B
⑤⑥-⑦[(*4)]	Packages (Order Limit)	MR-G	SOT-25 (3000/Reel)
		NR-G	SSOT-24 (3000/Reel)
		GR-G	USP-4 (3000/Reel)

NOTE:

The "-G" suffix denotes Halogen and Antimony free as well as being fully RoHS compliant.

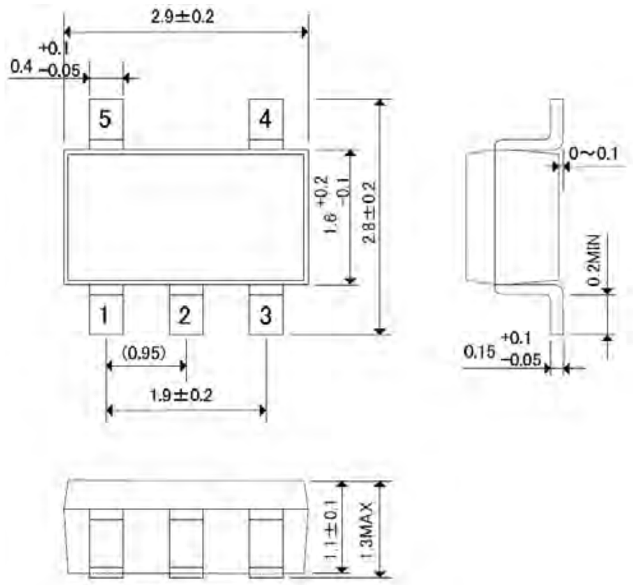
1) Standard output voltages are shown in the table below. Other output voltages as well as other combinations of IC functions available by request. Contact IXYS Sales representative for more information.

STANDARD VOLTAGES

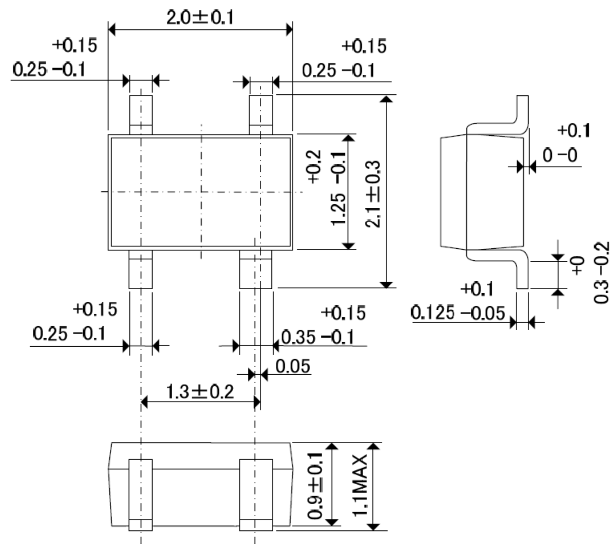
VOUT, V	PACKAGE		
	USP-4	**SSOT-24**	**SOT-25**
1.20	IXD1233H121GR-G	IXD1233H121NR-G	IXD1233H121MR-G
1.50	IXD1233H151GR-G	IXD1233H151NR-G	IXD1233H151MR-G
1.80	IXD1233H181GR-G	IXD1233H181NR-G	IXD1233H181MR-G
2.80	IXD1233H281GR-G	IXD1233H281NR-G	IXD1233H281MR-G
3.30	IXD1233H331GR-G	IXD1233H331NR-G	IXD1233H331MR-G

PACKAGE DRAWING AND DIMENSIONS

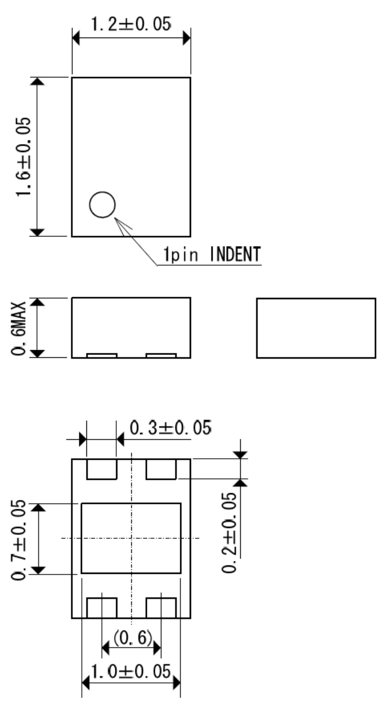
SOT-25, Units: mm



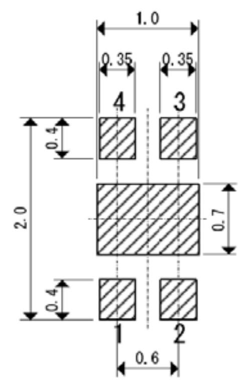
SSOT-24 Units: mm



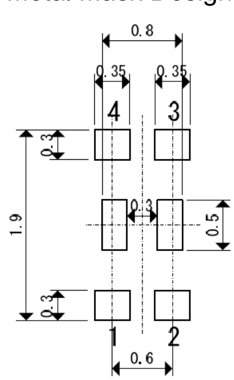
USP-4, Units: mm



USP-4 Reference Pattern Layout, Units: mm



USP-4 Reference Metal Mask Design, Units: mm



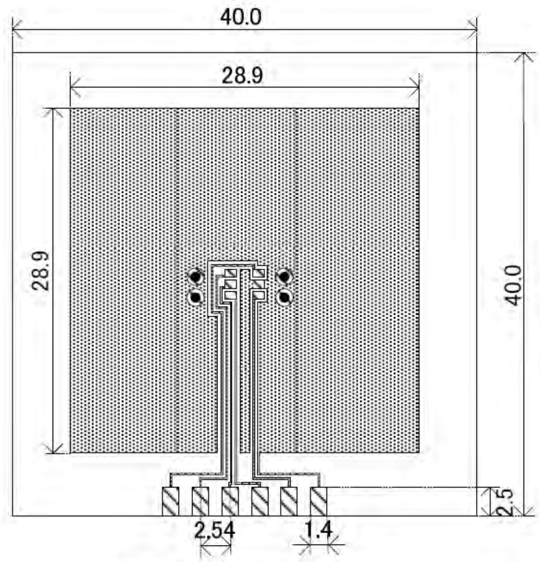
PACKAGE POWER DISSIPATION

SOT-25 Power Dissipation

The power dissipation varies with the mount board conditions.
Please use this data as a reference only.

1. Measurement Conditions:

Condition:	Mount on a board
Ambient:	Natural convection
Soldering:	Lead (Pb) free
Board:	Dimensions 40×40 mm (1600 mm^2 in one side) Copper (Cu) traces occupy 50% of the board area on top and bottom layers Package heat sink tied to the copper traces. (Board of SOT-26 is used)
Material:	Glass Epoxy (FR-4)
Thickness:	1.6 mm
Through-hole:	4 x 0.8 Diameter

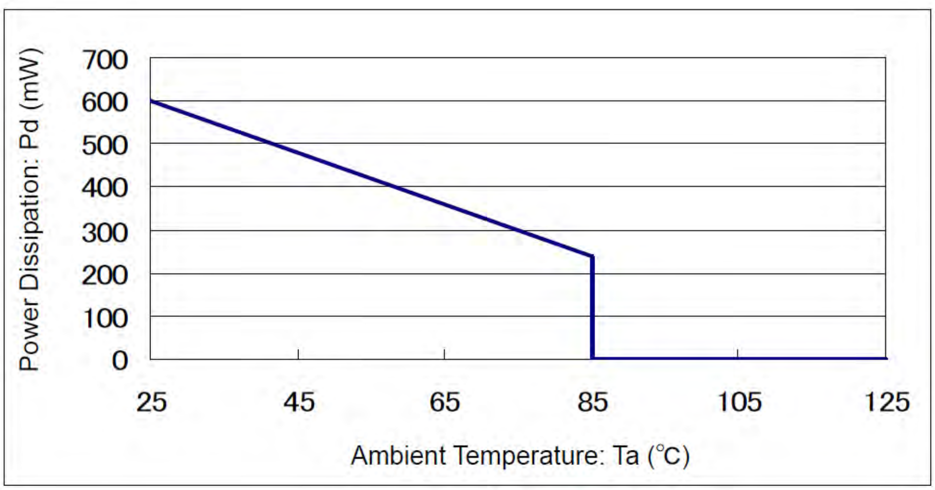


Evaluation Board (unit: mm)

2. Power Dissipation vs. Ambient Temperature

Board Mount (Tjmax = 125 ^{0}C)

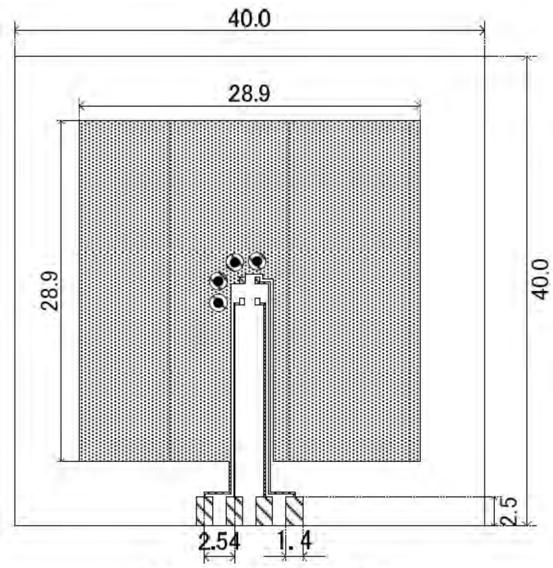
Ambient Temperature, ^{0}C	Power Dissipation Pd, mW	Thermal Resistance, ^{0}C/W
25	600	166.67
85	240	



PACKAGE POWER DISSIPATION (CONTINUED)

SSOT-24 Power Dissipation

The power dissipation varies with the mount board conditions. Please use this data as a reference only.



Evaluation Board (Unit: mm)

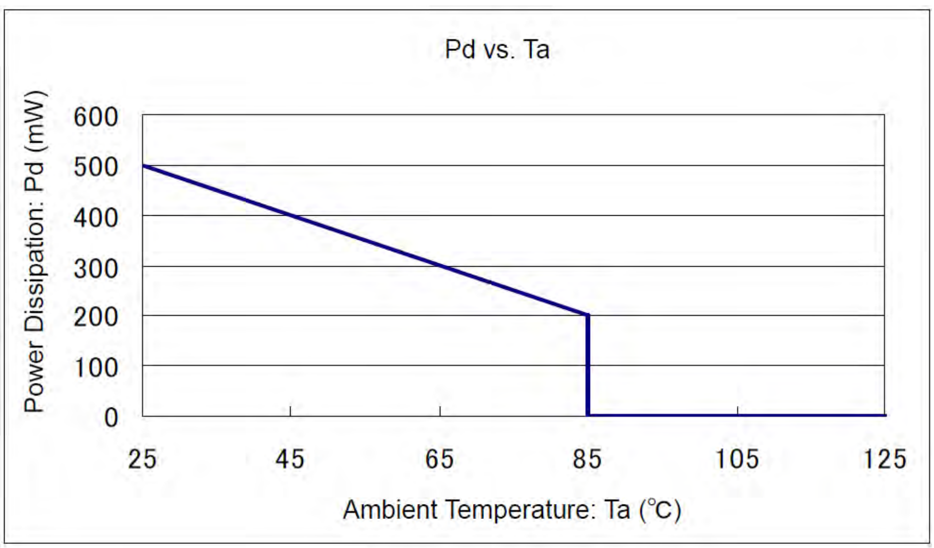
1. Measurement Conditions:

Condition:	Mount on a board
Ambient:	Natural convection
Soldering:	Lead (Pb) free
Board:	Dimensions 40×40 mm (1600 mm^2 in one side) Copper (Cu) traces occupy 50% of the board area on top and bottom layers Package heat sink tied to the copper traces. (Board of SOT-26 is used)
Material:	Glass Epoxy (FR-4)
Thickness:	1.6 mm
Through-hole:	4 x 0.8 Diameter

2. Power Dissipation vs. Ambient Temperature

Board Mount (Tjmax = 125 ^{0}C)

Ambient Temperature, ^{0}C	Power Dissipation Pd, mW	Thermal Resistance, ^{0}C/W
25	500	200.00
85	200	



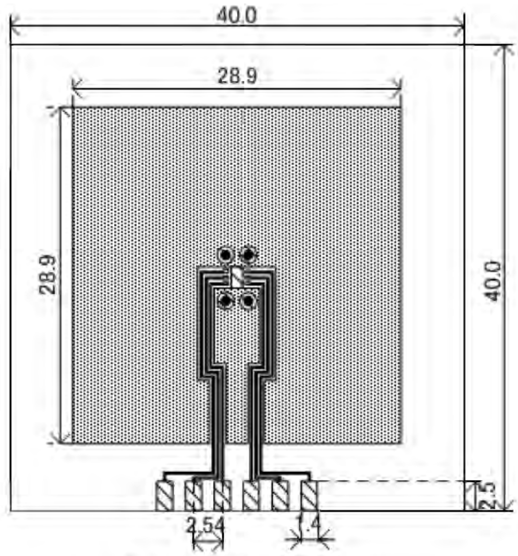
PACKAGE POWER DISSIPATION (CONTINUED)

USP-4 Power Dissipation

The power dissipation varies with the mount board conditions.
Please use this data as a reference only.

1. Measurement Conditions:

Condition:	Mount on a board
Ambient:	Natural convection
Soldering:	Lead (Pb) free
Board:	Dimensions 40×40 mm (1600 mm^2 in one side) Copper (Cu) traces occupy 50% of the board area on top and bottom layers Package heat sink tied to the copper traces. (Board of SOT-26 is used)
Material:	Glass Epoxy (FR-4)
Thickness:	1.6 mm
Through-hole:	4 x 0.8 Diameter

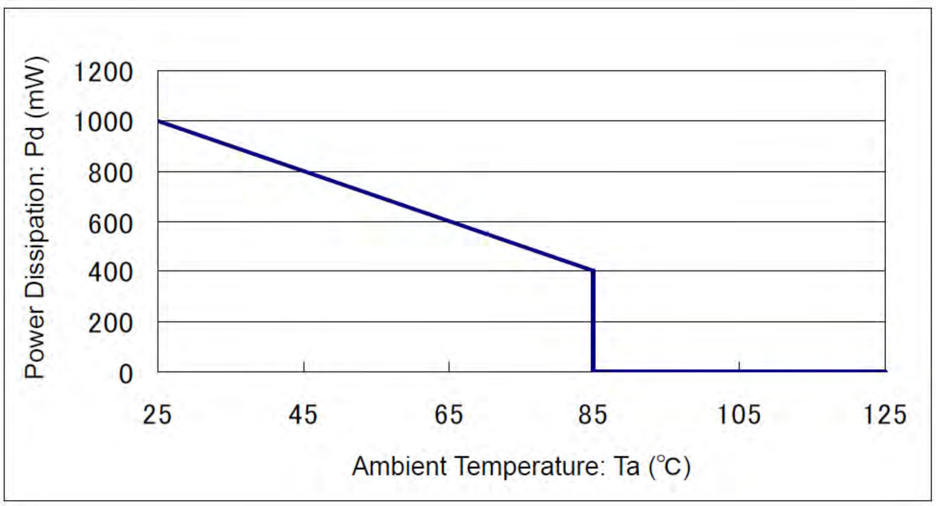


Evaluation Board (unit: mm)

2. Power Dissipation vs. Ambient Temperature

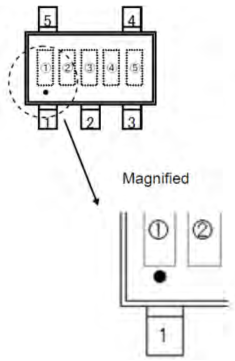
Board Mount (Tjmax = 125 ^{0}C)

Ambient Temperature, ^{0}C	Power Dissipation Pd, mW	Thermal Resistance, ^{0}C/W
25	1000	100.00
85	400	

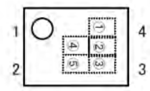


MARKING

SOT-25



USP-4



SOT-25 with the under-dot marking

① - represents product series

MARK	PRODUCT SERIES
1	IXD1233xxxxx-G

② - represents type of regulator

MARK		PRODUCT SERIES
V_{OUT} INCREMENTS		
0.1 V	0.05 V	
K	M	IXD1233Hxxxx-G

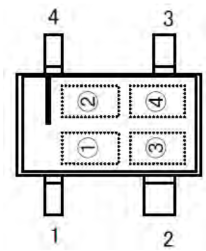
③ - represents output voltage

MARK	OUTPUT VOLTAGE, V	
0	1.2	1.25
1	1.3	1.35
2	1.4	1.45
3	1.5	1.55
4	1.6	1.65
5	1.7	1.75
6	1.8	1.85
7	1.9	1.95
8	2.0	2.05
9	2.1	2.15
A	2.2	2.25
B	2.3	2.35
C	2.4	2.45
D	2.5	2.55
E	2.6	2.65

MARK	OUTPUT VOLTAGE, V	
F	2.7	2.75
H	2.8	2.85
K	2.9	2.95
L	3.0	3.05
M	3.1	3.15
N	3.2	3.25
P	3.3	3.35
R	3.4	3.45
S	3.5	3.55
T	3.6	
U		
V		
X		
Y		
Z		

④⑤ - represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order, (G, I, J, O, Q, W excluded)

MARKING (Continued)



SSOT-24 (With an orientation bar at the top)

① - represents product series and output voltage

MARK	OUTPUT VOLTAGE, V	PRODUCT SERIES
A	1.2 – 2.0	IXD1233H121xx-G - IXD1233H201xx-G
B	2.1 – 2.9	IXD1233H211xx-G - IXD1233H291xx-G
C	3.0 – 3.6	IXD1233H301xx-G - IXD1233H361xx-G
D	1.25 – 2.05	IXD1233H12Bxx-G - IXD1233H20Bxx-G
E	2.15 – 2.95	IXD1233H21Bxx-G - IXD1233H29Bxx-G
F	3.05 – 3.55	IXD1233H30Bxx-G - IXD1233H35Bxx-G

② - represents output voltage

MARK	OUTPUT VOLTAGE, V					
1	1.2	2.1	3.0	1.25	1.95	3.05
2	1.3	2.2	3.1	1.35	2.05	3.15
3	1.4	2.3	3.2	1.45	2.15	3.25
4	1.5	2.4	3.3	1.55	2.25	3.35
5	1.6	2.5	3.4	1.65	2.35	3.45
6	1.7	2.6	3.5	1.75	2.45	3.55
7	1.8	2.7	3.6	1.85	2.55	
8	1.9	2.8		2.85	2.65	
9	2.0	2.9		2.95	2.75	

③④ - represents production lot number

01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order. (G, I, J, O, Q, W excluded)

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