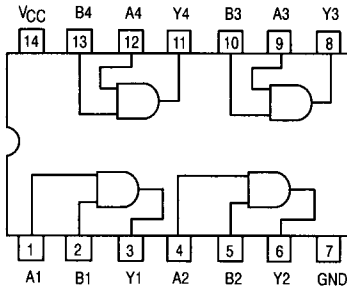




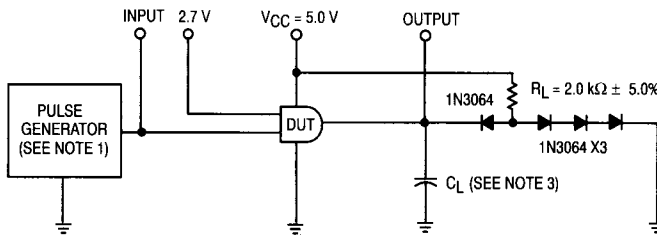
Quad 2-Input Positive AND Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/31004

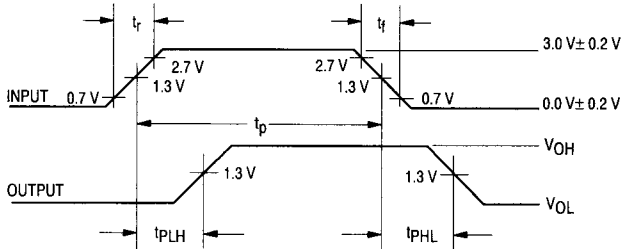
LOGIC DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. Pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_p = 0.5$ μ s, PRR ≤ 1.0 MHz, and $Z_{OUT} = 50$ Ω .
2. Inputs not under test are at 2.7 V.
3. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance.
4. All diodes are 1N3064 or equivalent.
5. Voltage measurements are to be made with respect to network ground terminal.

Military 54LS08



AVAILABLE AS:

- 1) JAN: JM38510/31004BXA
- 2) SMD: N/A
- 3) 883: 54LS08/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	2	VCC
B1	2	2	3	VCC
Y1	3	3	4	VCC
A2	4	4	6	VCC
B2	5	5	8	VCC
Y2	6	6	9	VCC
GND	7	7	10	GND
Y3	8	8	12	VCC
A3	9	9	13	VCC
B3	10	10	14	VCC
Y4	11	11	16	VCC
A4	12	12	18	VCC
B4	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

54LS08

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -400 μA, V _{IH} = 2.0 V, V _{IN} = 2.0 V on other input.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V, V _{IN} = 5.5 V on other input.
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other input is open.
I _{IH1}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 2.7 V, other input = 0 V.
I _{IH2}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other input = 0 V.
I _{IL}	Logical "0" Input Current	-150	-380	-150	-380	-150	-380	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other input = 5.5 V.
I _{OS}	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (both inputs), V _{OUT} = 0 V.
I _{CCH}	Power Supply Current		4.8		4.8		4.8	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (both inputs).
I _{CCL}	Power Supply Current		8.8		8.8		8.8	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (both inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL}	Propagation Delay /Data-Output	2.0	20	2.0	30	2.0	30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PHL}	Output High-Low	—	20	—	25	—	25		V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH}	Propagation Delay /Data-Output	2.0	15	2.0	25	2.0	25	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PLH}	Output Low-High	—	15	—	20	—	20		V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.

NOTE:

- The limits specified for C_L = 15 pF are guaranteed but not tested.