mosaic

Mosaic Semiconductor Inc.

# 128K x 8 SRAM

## MSM8129-025/35

Issue 1.5 : April 1993

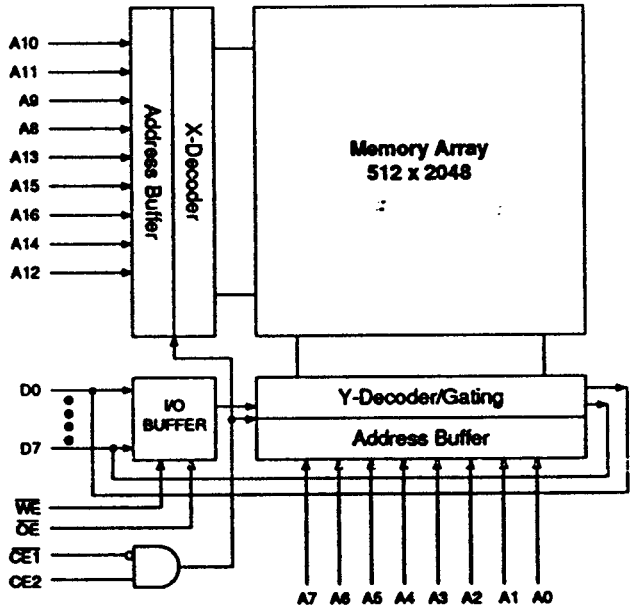
## ADVANCE PRODUCT INFORMATION

131,072 x 8 CMOS High Speed Static RAM

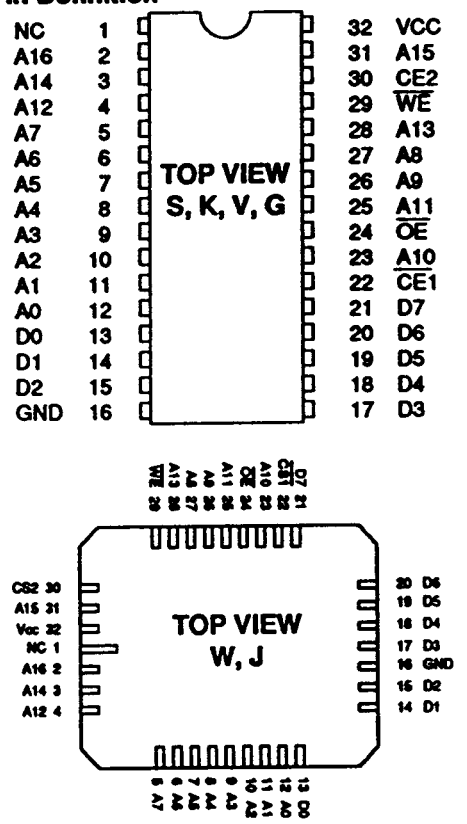
### Features

Very Fast Access Times of 25/35 ns
JEDEC Standard 32 pin DIL footprint
VIL™ High Density Package Available
Active Power 400 mW (typ.)
350 mW (typ.) L -Version
Standby Power 150 mW (typ.)
100 mW (typ.) L -Version
Completely Static Operation
Directly TTL compatible
Common data inputs & outputs
May be processed in accordance with MIL-STD-883

### Block Diagram




### Pin Definition




### Pin Functions

| | |
|---|---|
| A0-A16 | Address Inputs |
| D0-7 | Data Input/Output |
| $\overline{CE1}$ | Chip Enable |
| CE2 | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| NC | No Connect |
| $V_{cc}$ | Power (+5V) |
| GND | Ground |

### Package Details

| Pin Count | Description | Package Type | Material | Pin Out |
|---|---|---|---|---|
| 32 | 0.6" Dual-in-Line (DIP) | S | Ceramic | JEDEC |
| 32 | 0.4" Dual-in-Line (DIP) | K | Ceramic | JEDEC |
| 32 | 0.1" Vertical-in-Line (VIL™) | V | Ceramic | JEDEC |
| 32 | Bottom Brazed Flatpack | G | Ceramic | JEDEC |
| 32 | Leadless Chip Carrier (LCC) | W | Ceramic | JEDEC |
| 32 | J-Leaded Chip Carrier (JLCC) | J | Ceramic | JEDEC |

Package dimensions and outlines are displayed on pages 6&7.

## Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | -0.5V to +7 | V |
| Power Dissipation | $P_T$ | 1.0 | W |
| Storage Temperature | $T_{STG}$ | -65 to +150 | °C |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) $V_T$ can be -3.0V pulse of less than 30ns.

## Recommended Operating Conditions

| | | *min* | *typ* | *max* | |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | - | 6.0 | V |
| Input Low Voltage | $V_{IL}$ | -0.5 | - | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | - | 70 | °C |
| | $T_{AI}$ | -40 | - | 85 | °C (8128I) |
| | $T_{AM}$ | -55 | - | 125 | °C (8128M, MB, MC) |

Notes : (1) $V_{IL}$ can be -3.0V pulse of less than 20ns.

## DC Electrical Characteristics ($V_{CC}$ = 5.0V±10%, $T_A$=-55°C to +125°C)

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$=Gnd to $V_{CC}$ | - | - | 10 | µA |
| OutputLeakage Current | $I_{I/O}$ | $\overline{CE1}$=$V_{IH}$, CE2 =$V_{IL}$, $V_{OUT}$=GND to $V_{CC}$ | - | - | 10 | mA |
| Average Supply Current | $I_{CC1}$ | Min. Cycle, duty=100%, $I_{OUT}$=0mA | - | - | 175 | mA |
| Standby Supply Current | $I_{SB}$ | $\overline{CE1}$=$V_{IH}$, CE2 = $V_{IL}$ $V_{IN}$=$V_{IH}$ or $V_{IL}$ | - | - | 55 | mA |
| - L Version | $I_{SB}$ | As above | - | - | 45 | mA |
| | $I_{SB1}$ | $\overline{CE1}$≥$V_{CC}$-0.2V, CE2 ≤ 0.2V, 0.2V≥$V_{IN}$≥$V_{CC}$-0.2V | - | - | 10 | mA |
| - L Version | $I_{SB1}$ | As above | - | - | 5 | mA |
| Output Voltage | $V_{OL}$ | $I_{OL}$=8.0mA, $V_{CC}$= Min. | - | - | 0.4 | V |
| | $V_{OH}$ | $I_{OH}$=-4.0mA, $V_{CC}$= Min. | 2.4 | - | - | V |

Note 1: Typical values are at $V_{CC}$=5.0V, $T_A$=25°C and specified loading.

## Capacitance ($V_{CC}$=5V±10%, $T_A$=25°C)

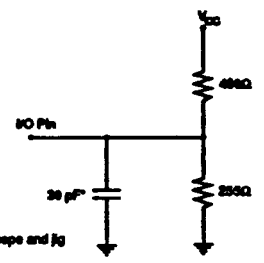
| *Parameter* | *Symbol* | *Test Condition* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| I/P Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 8 | pF |
| I/O Capacitance | $C_{I/O}$ | $V_{I/O}$=0V | - | 8 | pF |

Note: This parameter is sampled and not 100% tested.

## AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: See Load Diagram
* $V_{CC}$=5V±10%

## Output Load

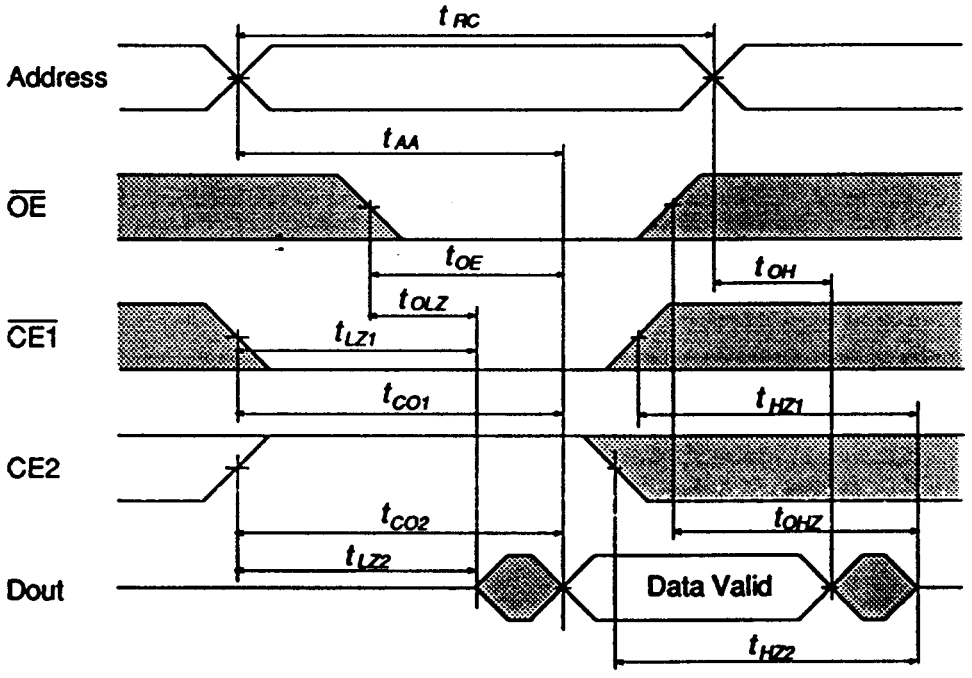


## Electrical Characteristics & Recommended AC Operating Conditions

### Read Cycle

| Parameter | Symbol | 25 min | 25 max | 35 min | 35 max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 25 | - | 35 | - | ns | |
| Address Access Time | $t_{AA}$ | - | 25 | - | 35 | ns | |
| Chip Enable ($\overline{CE1}$) Access Time | $t_{CO1}$ | - | 25 | - | 35 | ns | |
| Chip Enable (CE2) Access Time | $t_{CO2}$ | - | 25 | - | 35 | ns | |
| Output Hold from Address Change | $t_{OH}$ | 3 | - | 3 | - | ns | |
| Chip Enable ($\overline{CE1}$) to O/P in Low Z | $t_{LZ1}$ | 5 | - | 5 | - | ns | 2 |
| Chip Enable (CE2) to O/P in Low Z | $t_{LZ2}$ | 5 | - | 5 | - | ns | 2 |
| Output Enable to Output in Low Z | $t_{OLZ}$ | 0 | - | 0 | - | ns | 2 |
| ChipDisable ($\overline{CE1}$) to O/P in high Z | $t_{HZ1}$ | 0 | 10 | 0 | 15 | ns | 2 |
| Chip Disable (CE2) to O/P in high Z | $t_{HZ2}$ | 0 | 10 | 0 | 15 | ns | 2 |
| Output Enable Access Time | $t_{OE}$ | - | 8 | - | 12 | ns | |
| Output Disable to Output in High Z | $t_{OHZ}$ | - | 10 | - | 12 | ns | 2 |

### Read Cycle Timing Waveform (1)

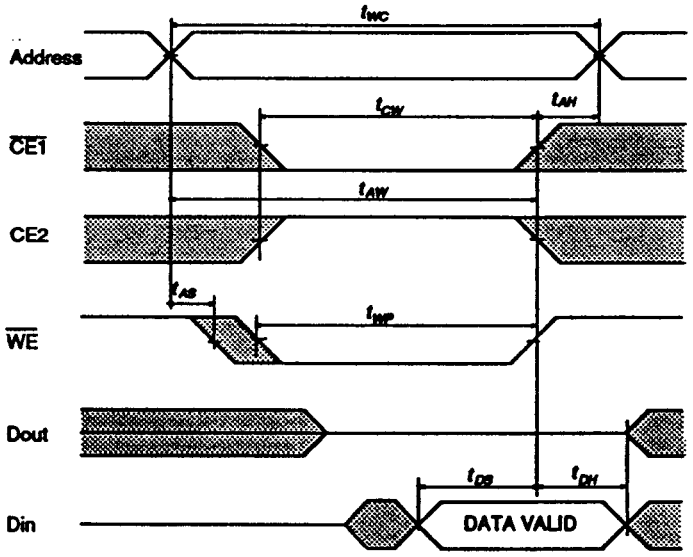



Notes:
(1) $\overline{WE}$ is High for Read Cycle.
(2) $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, $t_{HZ}$ max is less than $t_{LZ}$ min both for a given device and from device to device. This parameter is sampled and not 100% tested.

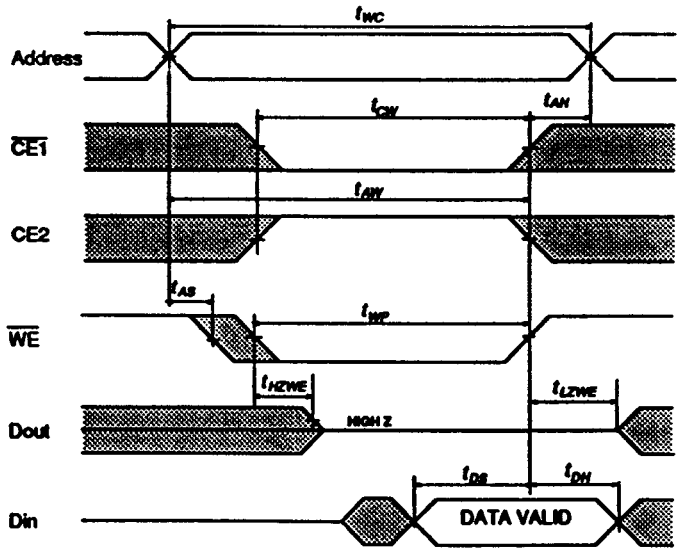
## Write Cycle

| Parameter | Symbol | 25 min | 25 max | 35 min | 35 max | Unit |
|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 25 | - | 35 | - | ns |
| Chip Enable to End of Write | $t_{CW}$ | 15 | - | 20 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 15 | - | 20 | - | ns |
| Address Setup Time | $t_{AS}$ | 0 | - | 0 | - | ns |
| Address Hold to End of Write | $t_{AH}$ | 0 | - | 0 | - | ns |
| Write Pulse Width | $t_{WP}$ | 15 | - | 20 | - | ns |
| Write Disable to Output in Low Z | $t_{WLZ}$ | 0 | - | 0 | - | ns |
| Write Enable to Output in High Z | $t_{WHZ}$ | 0 | 10 | 0 | 15 | ns |
| Data Setup Time | $t_{DS}$ | 10 | - | 15 | - | ns |
| Data Hold Time | $t_{DH}$ | 0 | - | 0 | - | ns |

## Write Cycle No.1 Timing Waveform (Chip Enable Controlled) (1)




## Write Cycle No.2 Timing Waveform (Write Enable Controlled) (1)



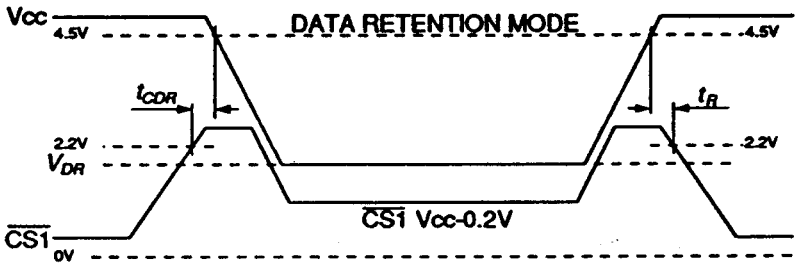

Note : (1) $\overline{OE}$ is continuosly low. ($\overline{OE} = V_{IL}$)

## Low $V_{cc}$ Data Retention Characteristics - L Version Only ($T_A$=-55°C to +125°C)

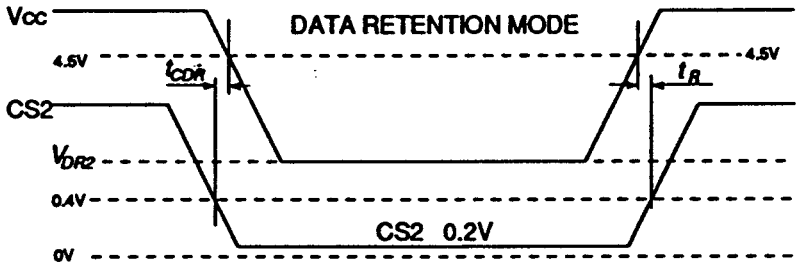
| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | | 2.0 | | - | V |
| Data Retention Current | $I_{CCDR}$ | $V_{CC}$=2.0V, $\overline{CE1}$ ≥$V_{CC}$-0.2V,CE2 ≤ $V_{CC}$-0.2V | - | - | 1 | mA |
| | | $V_{CC}$=3.0V, $V_{IN}$ ≥$V_{CC}$-0.2V or ≤ 0.2V. | - | - | 1.5 | mA |
| Chip Deselect to Data Retention | $t_{CDR}$ | See Retention Waveform | 0 | - | - | ns |
| Operation Recovery Time | $t_R$ | See Retention Waveform | $t_{RC}$ (1) | - | - | ns |

Note: (1) $t_{RC}$ = Read Cycle Time

## Low $V_{CC}$ Data Retention Timing Waveform 1 ($\overline{CE1}$ controlled)

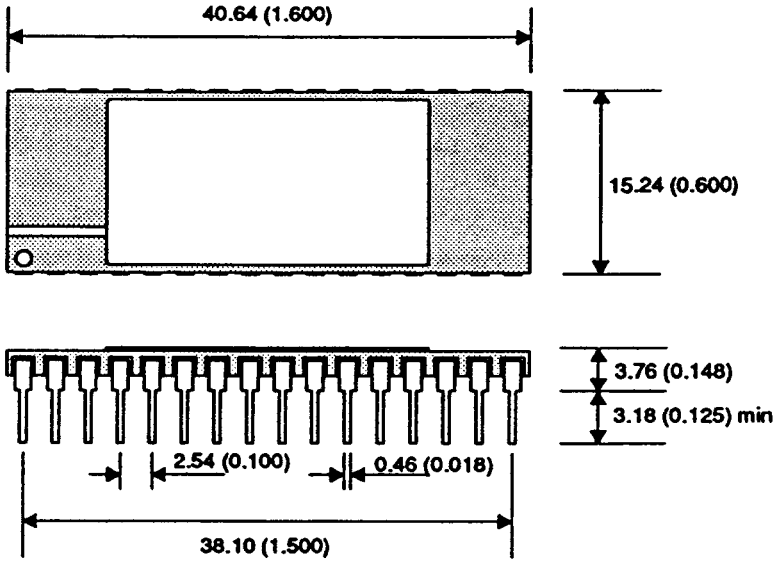



## Low $V_{CC}$ Data Retention Timing Waveform 2 (CE2 controlled)

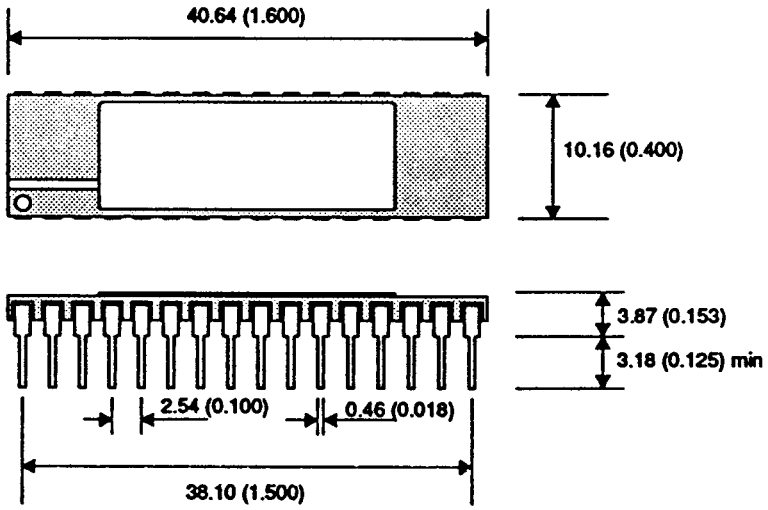


**Package Details** Dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.010)

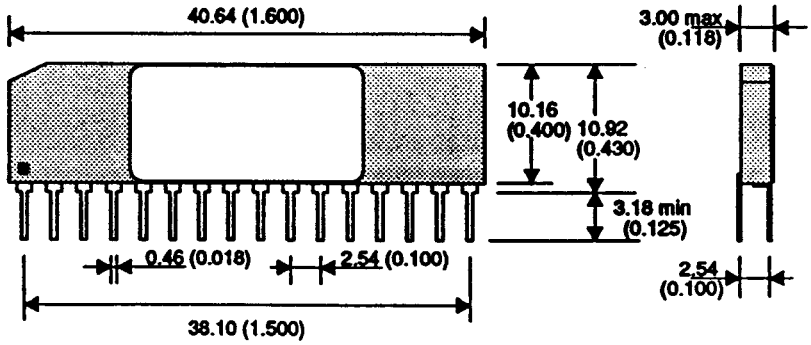
## 32 pin 0.6" Dual-In-Line (DIP) - 'S' Package



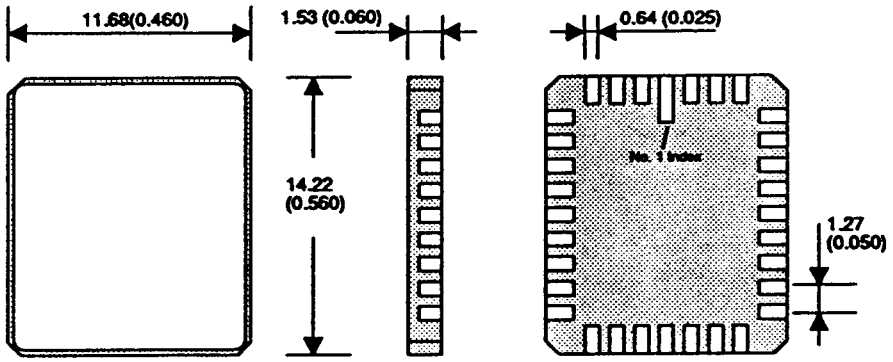

## 32 pin 0.4" Dual-In-Line (DIP) - 'K' Package



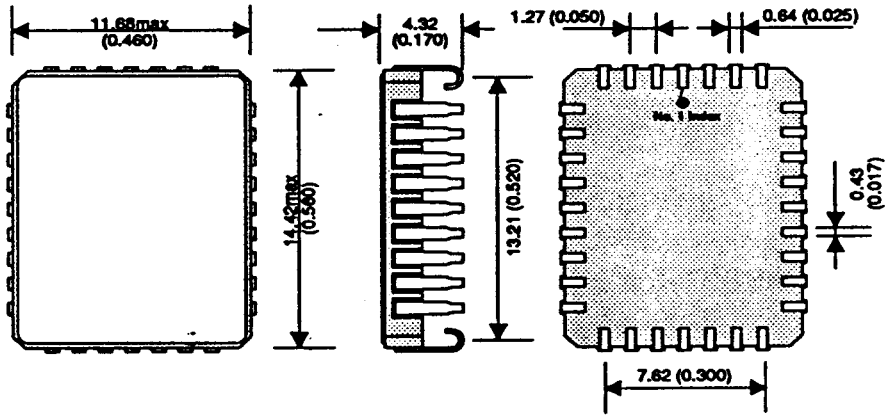

## 32 pin 0.1" Vertical-In-Line (VIL™) - 'V' Package



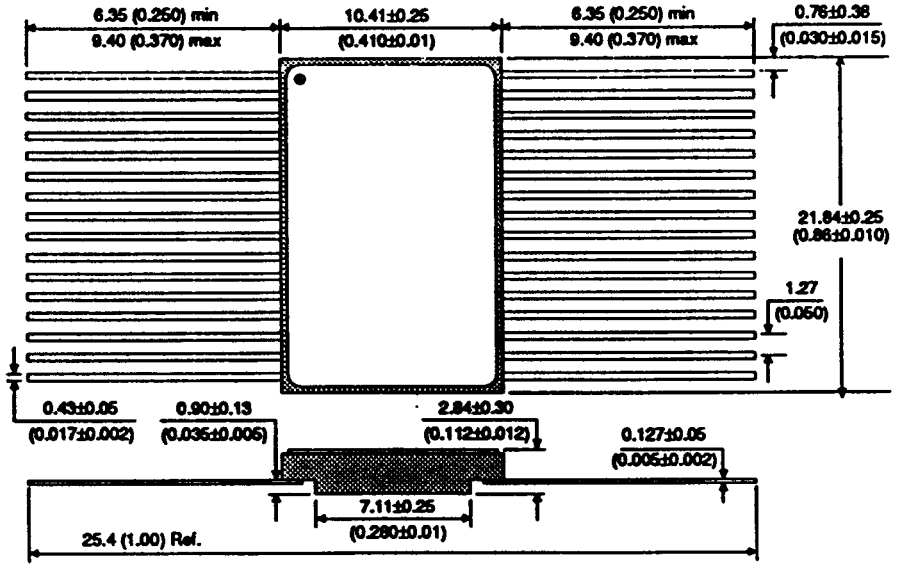
## 32 pin Leadless Chip Carrier (LCC) - 'W' Package




## 32 pin 'J' Leaded Chip Carrier (JLCC) - 'J' Package

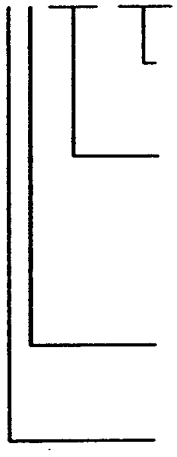



## 32 pin Ceramic Flatpack - 'G' Package



## Ordering Information

**MSM8129VLMB-025**



| | | |
|---|---|---|
| Speed | 025 | = 25 ns |
| | 35 | = 35 ns |
| Temp. range/screening | Blank | = Commercial |
| | I | = Industrial |
| | M | = Military |
| | MB | = Processed to MIL-STD-883 |
| | MC | = Compliant to MIL-STD-883 |
| Power | Blank | = Standard Power |
| | L | = Low Power |
| Package | S | = 32 pin 0.6" DIP |
| | K | = 32 pin 0.4" DIP |
| | V | = 32 pin 0.1" VIL |
| | G | = 32 lead Flatpack |
| | W | = 32 pad LCC |
| | J | = 32 pad JLCC |

**Note:** For more information regarding screening flows, contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'



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