FEATURES

- **Nine or Ten clock outputs:**
  - Outputs operate at frequencies, up to 80 MHz
  - Outputs grouped in two banks of five outputs on SC3517/18/28/29
  - Outputs grouped in a bank of four and a bank of five outputs on the SC3526
  - Outputs grouped in a bank of three and a bank of seven outputs on the SC3527
- **Leading edge skew for all outputs ≤0.35 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **28-pin SOIC package**

APPLICATIONS

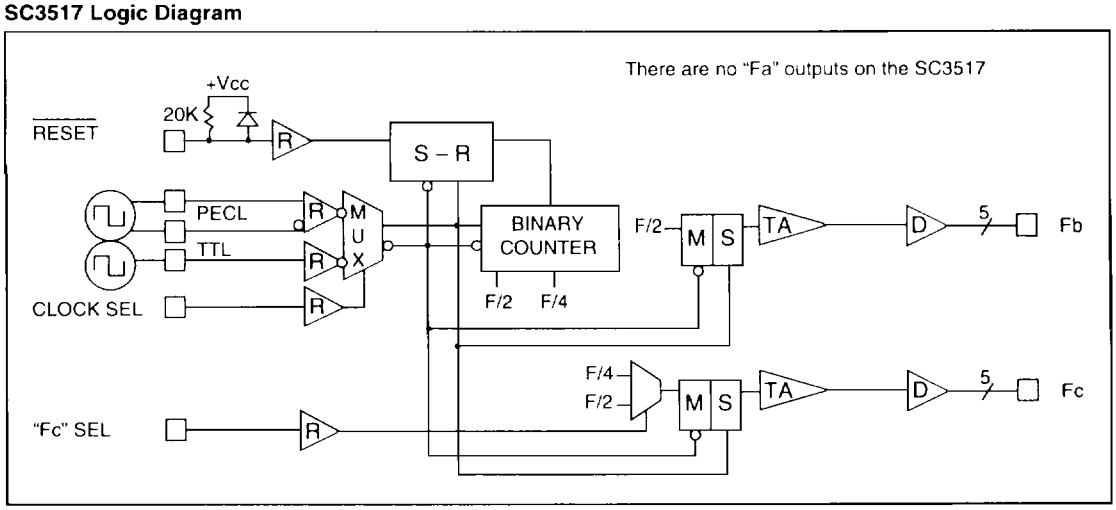
- **Compatible with Intel's Pentium™ processor**
- **Compatible with PowerPC™ processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Datacom and Telecom networks**

GENERAL DESCRIPTION

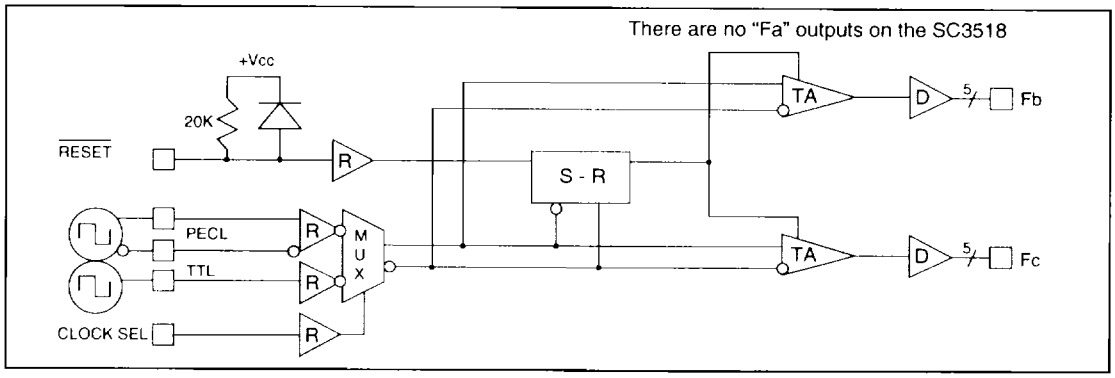
The SC3517, SC3518, SC3526, SC3527, SC3528 and SC3529 are precision low skew clock drivers with nine or ten outputs. They require a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to divide-by-two master-slave flip-flops or to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

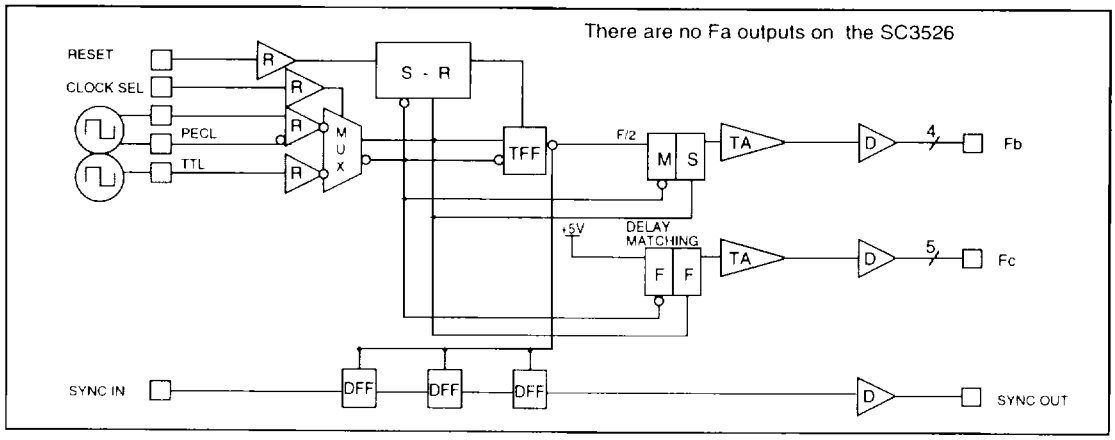
SC3517 Logic Diagram



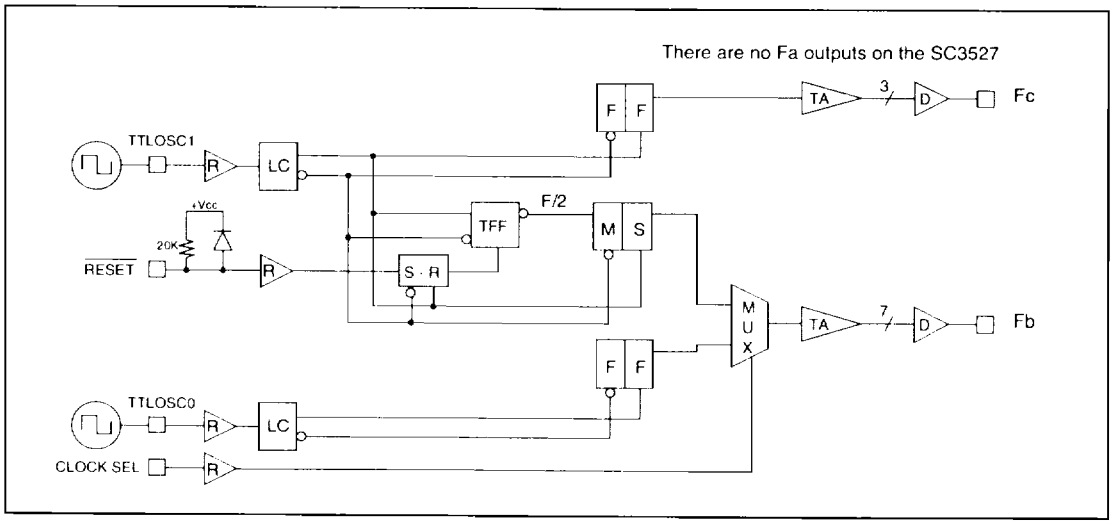
SC3518 Logic Diagram



SC3526 Logic Diagram



SC3527 Logic Diagram



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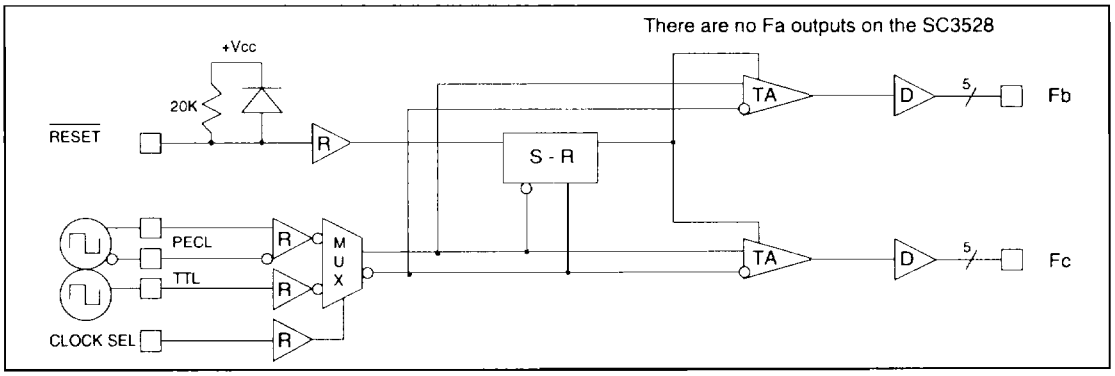
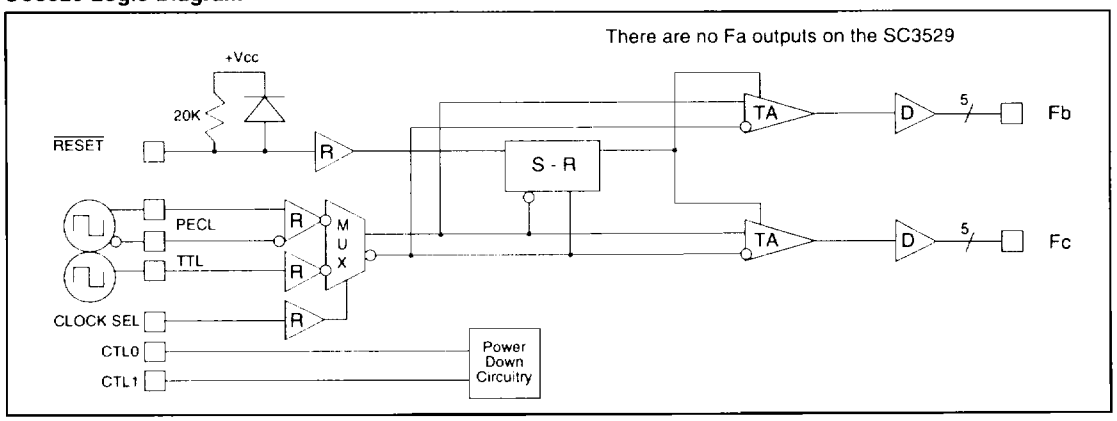
SC3528 Logic Diagram



SC3529 Logic Diagram



SC3517/18/26/27/28/29 Product Selection Guide

	Output Frequency with Respect to Input Frequency					
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Number of Outputs ÷ 2 or 4	Special Features	Package
SC3517	10	5	N/A	5	—	28 SOIC
SC3518	10	10	N/A	N/A	—	28 SOIC
SC3526	9	5	4	N/A	Sync Output	28 SOIC
SC3527	10	3	7	N/A	Selectable single or dual clock input.	28 SOIC
SC3528	10	10	N/A	N/A	—	28 SOIC
SC3529	10	10	N/A	N/A	Power Down	28 SOIC

Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

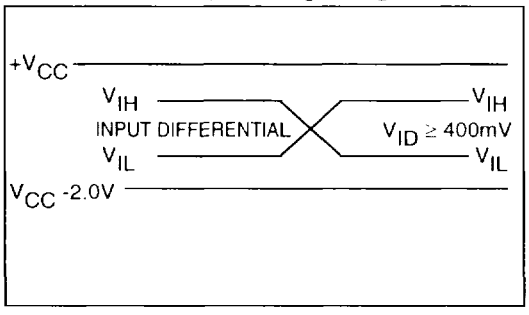
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	RESET	V_{IN} = 2.4V		-200	uA
	TTL, CSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	RESET	V_{IN} = 0.5V		-325	uA
	TTL, CSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	SC3517, 70°C, Typ Pwr=370 mW		600	mW
		SC3518, 70°C, Typ Pwr=250 mW		425	mW
		SC3526, 70°C, Typ Pwr=225 mW		375	mW
		SC3527, 70°C, Typ Pwr=350 mW		350	mW
		SC3528, 70°C, Typ Pwr=425 mW		425	mW
		SC3529, 70°C, Typ Pwr=250 mW		425	mW

1. Maximum test duration, one second.
2. The SC3517/18/26/27/28/29 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the outputs will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications — Using "AC Test/Evaluation Circuit"

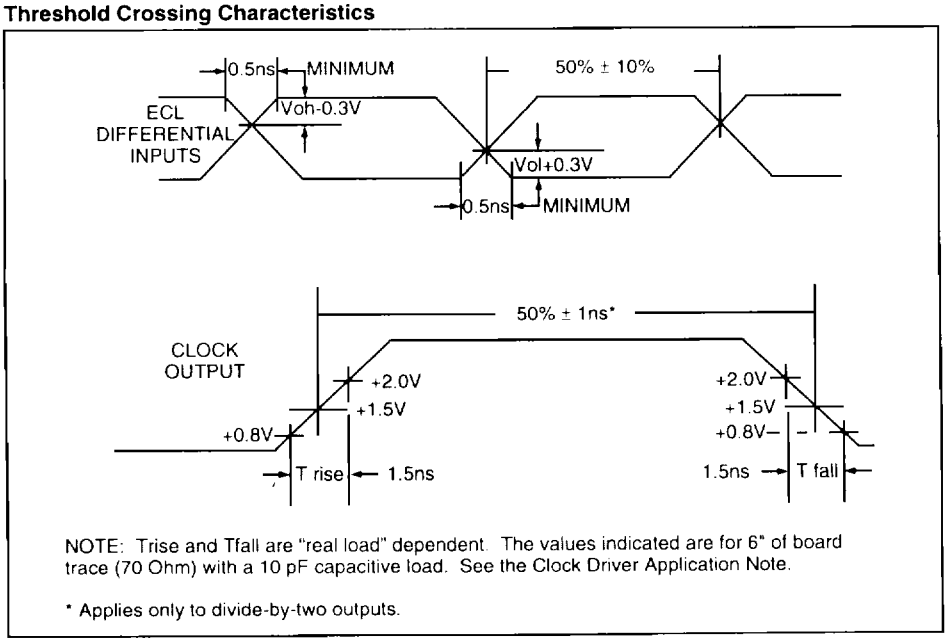
V_{CC} = +5.0V ± 5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3517	SC3518	SC3526	SC3527	SC3528	SC3529	Units
Maximum Skew Across All Outputs Options: Standard −1	1.0 0.5	— 0.5	0.35 —	—	0.35	0.35	ns
Delay of Fb from Fc outputs (CLKSEL = 1) [Tdly]	—	—	—	Min. 50 Typ. 0.9 Max. 1.7	—	—	ps ns ns
Maximum Skew within an Output Group	0.25	0.25	—	Fb .50 Fc .35	—	—	ns
Maximum Output Duty Cycle Asymmetry	±1.0 ns	—	Min. 45% Max. 55%	Min. 45% Max. 55%	—	—	ns or %
Maximum TTL Input Frequency	80	80	80	80	80	80	MHz
Maximum PECL Differential Input Frequency	160	80	80	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

* Applies only to divide-by-two outputs.

DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed single-chip, nine or ten-output clock buffer drivers using AMCC's advanced BiCMOS process. These designs have been optimized for minimum skew.

The clock source input for these devices may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) levels. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. On the SC3527, when CLKSEL is low (or floating) TTLOSC0 is used to drive the FB0-6 outputs, and when CLKSEL is high, both output groups use the TTLOSC1 reference input clock (see SC3527 Application Examples). This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagrams. The output duty cycle asymmetry becomes a function of the output driver slew rate into the AC load for divided outputs. For simple buffered (1x frequency) outputs, the output duty cycle asymmetry becomes a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. For the products with (pullup) resistors on the RESET input, a capacitor (4.7µF ≈ 100 ms) connected between this pin and ground will cause the device to respond with a "power-up reset"—a delay in the clock outputs becoming active. At the assertion of RESET the SC3518/28/29 outputs will go low following four falling edge clock inputs. The SC3527 outputs will go low after three falling edge clock inputs and the SC3517 output will go low after five falling edge clock inputs. At the deassertion of RESET, the SC3518/28/29 outputs will resume operation after four falling edge clock inputs. The SC3527 outputs will resume after three falling edge clock inputs and the SC3517 outputs will resume operation after five falling edge clock inputs.

The RESET input of the SC3526 operates in a different fashion. When RESET is held high (asserted), the FC0-4 outputs will continue to run while the FB0-3 outputs will be driven to a static high. When RESET is de-asserted, the FB0-3 outputs will be active after a fixed three-input clock delay, from a leading edge count origin.

The SC3526 also includes a synchronization circuit. The synchronization circuit provides three serial flip flops clocked by the internally generated F/2 (half reference frequency) clock which can be used to provide a three-stage metastability filter or a three-cycle delay of the F/2 outputs. The circuit receives its input from the SYNCIN input and feeds the D-input to the first flip-flop; the Q output of the flip-flop feeds the D-input of the second flip-flop which, in turn, feeds the third flip-flop. The Q output of the third flip-flop drives the SYNCOUT pin.

For the SC3529, the CTL0 and CTL1 inputs can be used to "power down" two, five, or ten of the SC3529's outputs. The control circuitry is designed to be synchronous with the reference clock to prevent duty cycle distortion during power-up or power-down sequencing.

When the inputs are configured (see "SC3529 Input Confiiguration table"), the appropriate outputs are driven to the minimum power state (LOW). With all outputs disabled, the power of the device is equal to its static dissipation of 250 mW.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to ensure that the clock driver will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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SC3529 Input Configuration

CTL0	CTL1	FUNCTION
0	0	All Outputs enabled
0	1	FC0 – FC4 enabled
1	0	FB0 – FB1 enabled
1	1	All outputs disabled

SC3517 Output Clock Frequency Selection

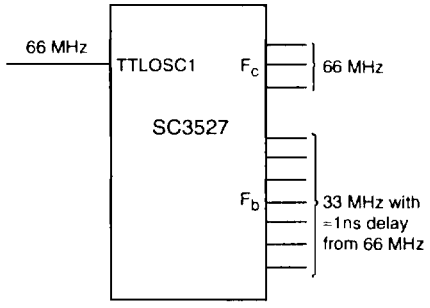
"C" SEL	XCO FREQ	Fb	Fc
LO	F	F/2	F/4
HI	F	F/2	F/2

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non-crystal oscillator sources may be used at the user's discretion. See the Clock Driver Application Note.

SC3527 Application Examples

Example 1.
Low Skew, Single Reference Frequency Mode

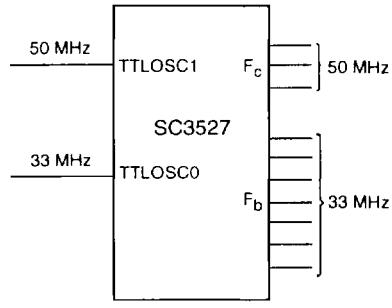
Three outputs at the primary frequency and seven outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈1 ns.



CLKSEL = 1

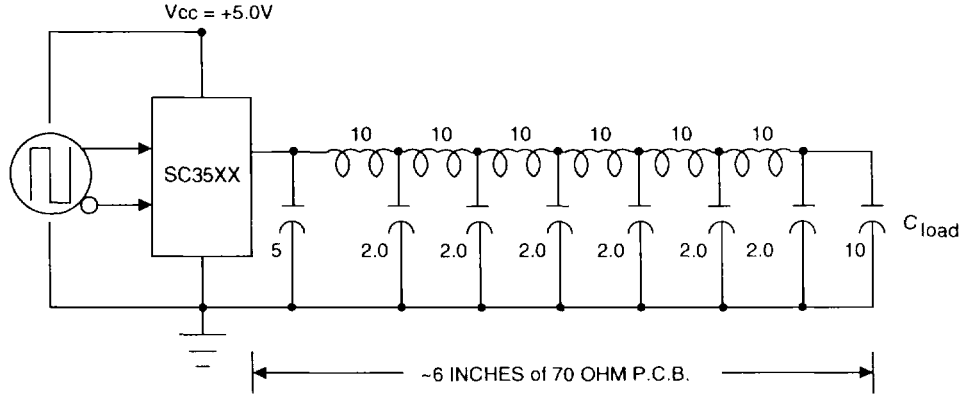
Example 2.
Dual Reference Frequency Mode, Asynchronous

Three outputs at the primary frequency and seven outputs at the secondary frequency with ≈1 ns internal delay at the F_b outputs.



CLKSEL = 0

AC Test/Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see "AC Test/ Evaluation Circuit", for complete load definition).

The output power must be added to the core power (600 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the clock driver. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes a clock driver with 5 Fa outputs driving 10 pF loads at 66 MHz and 4 Fb outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power (SC3517)	= 600 mW
5 Fa, 10 pF, 66 MHz = (5 x 47 mW)	= 235 mW
4 Fb, 15 pF, 33 MHz = (4 x 24 mW)	= 96 mW
1 Fb, no load, 33 MHz = (1 x 12 mW)	= 12 mW
Total Power =	1173 mW

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The clock driver's junction temperature would then be:

70°C + (0.943 watts x 57.7°C/watt) = 124°C

Note this is below the 140°C maximum junction temperature.

Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

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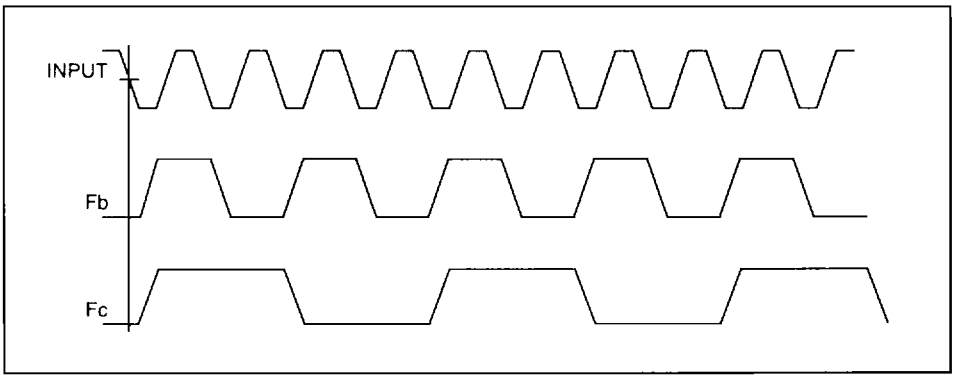
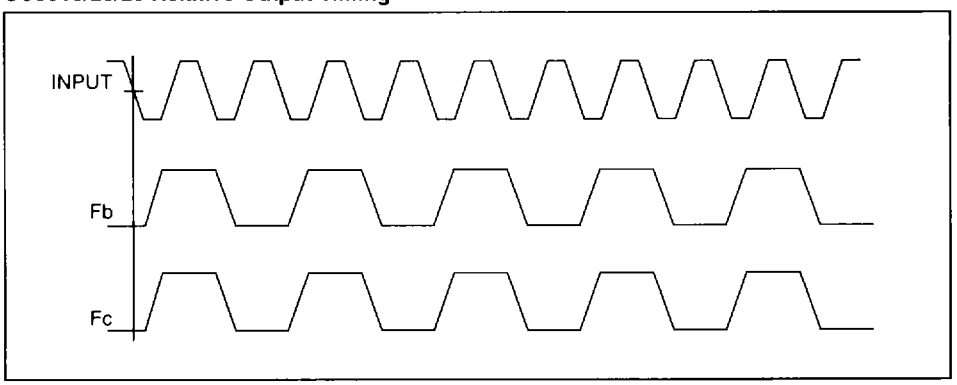
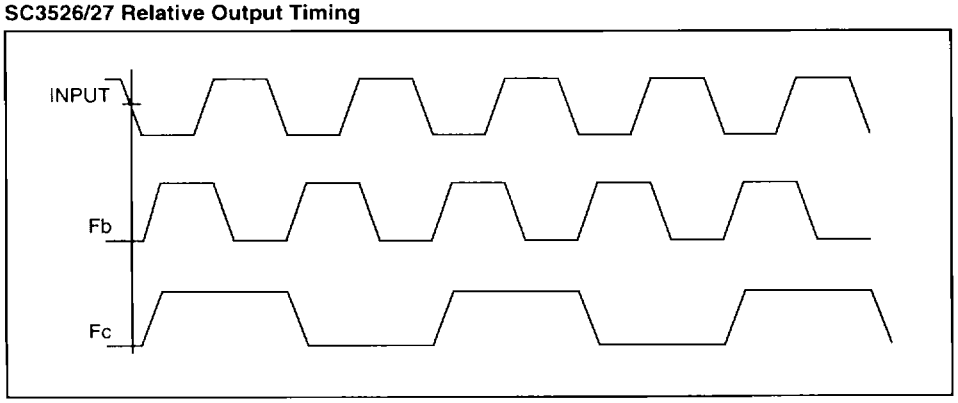
SC3517 Relative Output Timing



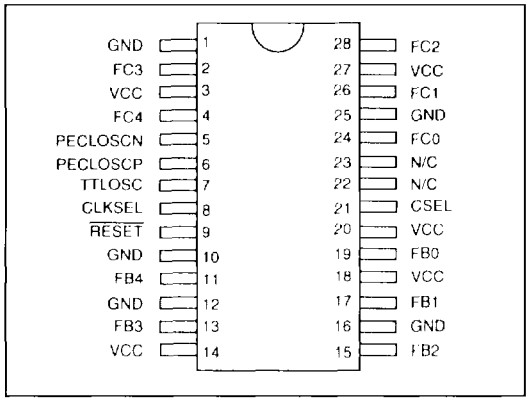
SC3518/28/29 Relative Output Timing



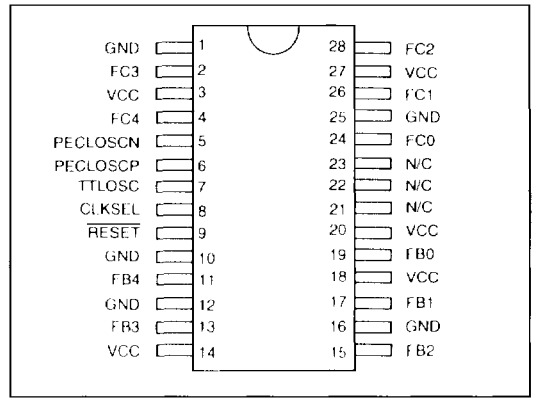
SC3526/27 Relative Output Timing



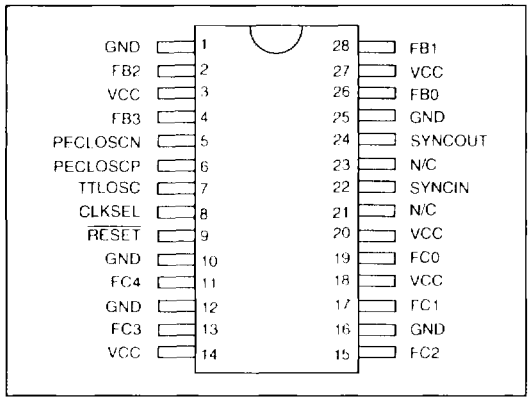
SC3517 Pinout



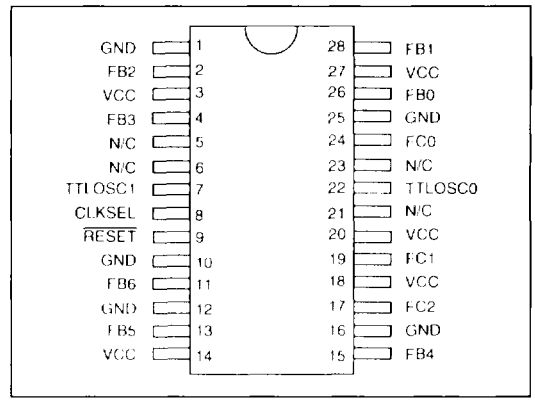
SC3518 Pinout



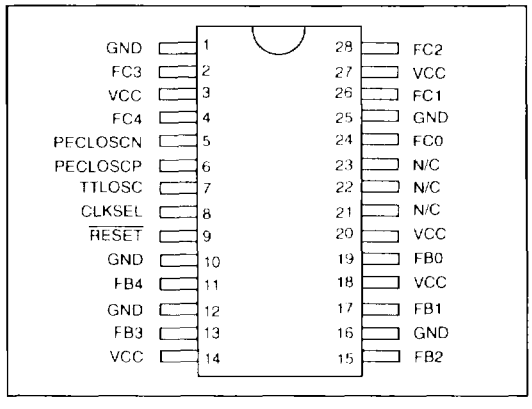
SC3526 Pinout



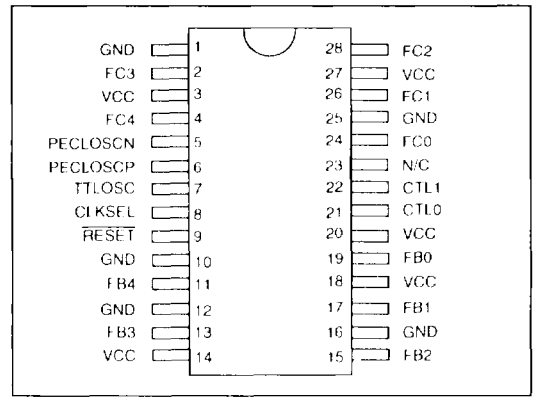
SC3527 Pinout



SC3528 Pinout



SC3529 Pinout



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Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC35XX **S** **-1** **/TD**

Optional Shipping Configuration
Blank = 25-unit tube
/D = dry pack
/TD = tape and reel, dry pack

Skew Option
Blank = standard output-output skew
-1 = 500 ps output-output skew

Package Option
S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC35XXS-1/D
28-pin SOIC package, 500 ps output-output skew, shipped dry packed in the standard tube.

Part Number	Standard	-1
SC3517	✔	✔
SC3518	N/A	✔
SC3526	✔	N/A
SC3527	✔	N/A
SC3528	✔	N/A
SC3529	✔	N/A

3