74VCXH245

Product Preview

Low-Voltage 1.8/2.5/3.3V 8-Bit Transceiver

(3-State, Non-Inverting with Bushold)

The 74VCXH245 is an advanced performance, non-inverting 8-bit transceiver. It is designed for very high-speed, very low-power operation in 1.8 V, 2.5 V or 3.3 V systems.

The VCXH245 is designed as a byte control. The Transmit/Receive (T/$\overline{\text{R}}$n) inputs determine the direction of data flow through the bi-directional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B to A ports. The Output Enable input ($\overline{\text{OE}}$), when HIGH, disables both A and B ports by placing them in a HIGH Z condition. The data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating inputs at a valid logic state.

- Designed for Low Voltage Operation: V_{CC} = 1.65-3.6 V
- High Speed Operation: 3.5 ns max for 3.0 to 3.6 V
  4.2 ns max for 2.3 to 2.7 V
  8.4 ns max for 1.65 to 1.95 V
- Static Drive: ±24 mA Drive at 3.0 V
  ±18 mA Drive at 2.3 V
  ±6 mA Drive at 1.65 V
- Includes Active Bushold to Hold Unused or Floating Data Inputs at a Valid Logic State
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 85°C
- ESD Performance: Human Body Model >2000 V; Machine Model >200 V

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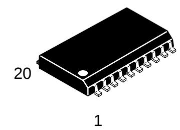
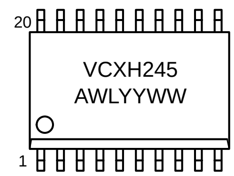
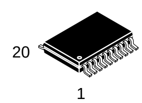
MARKING DIAGRAMS



SO-20
DW SUFFIX
CASE 751D





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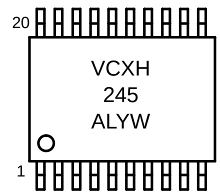
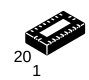
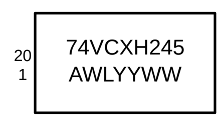
DT SUFFIX
CASE 948E





DQFN
SUFFIX TBD
CASE TBD



A	= Assembly Location
L , WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week

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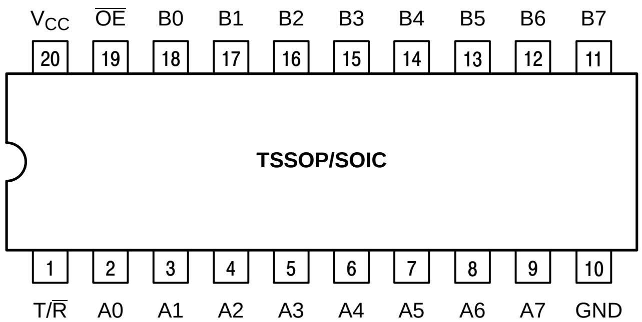


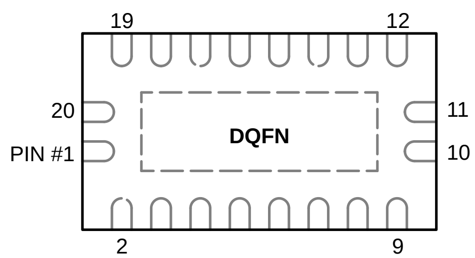


Figure 1. Pinout (Top View)

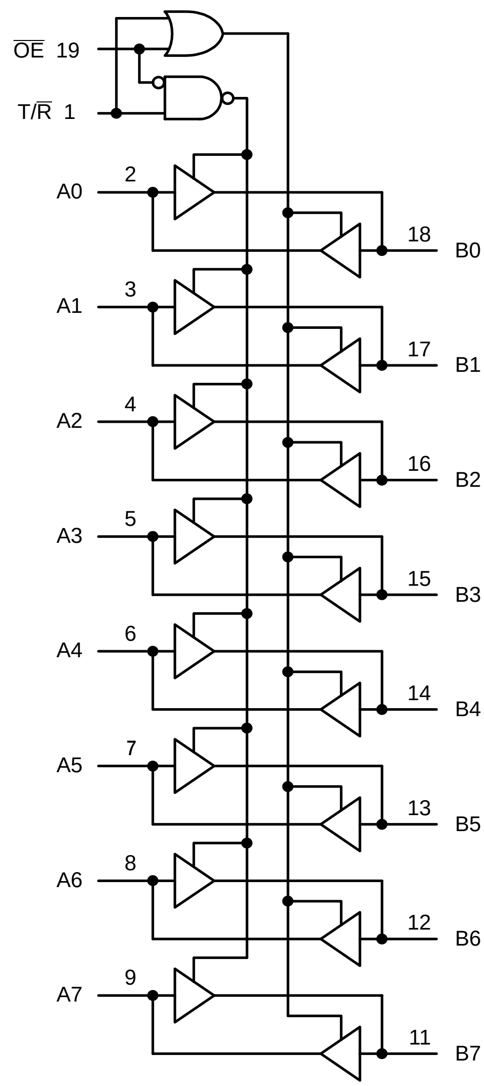


Figure 2. Logic Diagram

PIN NAMES

PINS	FUNCTION
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A0-A7	Side A Bushold Inputs or 3-State Outputs
B0-B7	Side B Bushold Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OPERATING MODE Non-Inverting
$\overline{OE}$	T/$\overline{R}$	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z State

H = High Voltage Level
L = Low Voltage Level
Z = High Impedance State
X = High or Low Voltage Level and Transitions are Acceptable

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	-0.5 to + 4.6		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq V_{CC} + 0.5$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq V_{CC} + 0.5$	Note 1	V
I_{IK}	DC Input Diode Current	-50	V_I < GND	mA
I_{OK}	DC Output Diode Current	-50	V_O < GND	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	-65 to +150		°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	1.65 1.2	3.3 3.3	3.6 3.6	V
V_I	Input Voltage	-0.3		V_{CC}	V
V_O	Output Voltage	0		V_{CC}	V
I_{OH}	HIGH Level Output Current, V_{CC} = 3.0 V - 3.6 V			-24	mA
I_{OL}	LOW Level Output Current, V_{CC} = 3.0 V - 3.6 V			24	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 2.3 V - 2.7 V			-18	mA
I_{OL}	LOW Level Output Current, V_{CC} = 2.3 V - 2.7 V			18	mA
I_{OH}	HIGH Level Output Current, V_{CC} = 1.65 V - 1.95 V			-6	mA
I_{OL}	LOW Level Output Current, V_{CC} = 1.65 V - 1.95 V			6	mA
T_A	Operating Free-Air Temperature	-40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0		10	ns/V

**Floating or unused control inputs must be held HIGH or LOW.

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T_A = -40°C to +85°C Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 2)	1.65 V ≤ V_{CC} < 1.95 V	0.65 x V_{CC}		V
		2.3 V ≤ V_{CC} ≤ 2.7 V	1.6		
		2.7 V < V_{CC} ≤ 3.6 V	2.0		
V_{IL}	LOW Level Input Voltage (Note 2)	1.65 V ≤ V_{CC} < 1.95 V		0.35 x V_{CC}	V
		2.3 V ≤ V_{CC} ≤ 2.7 V		0.7	
		2.7 V < V_{CC} ≤ 3.6 V		0.8	
V_{OH}	HIGH Level Output Voltage	1.65 V ≤ V_{CC} ≤ 3.6 V; I_{OH} = -100 μA	V_{CC} - 0.2		V
		V_{CC} = 1.65 V; I_{OH} = -6 mA	1.25		
		V_{CC} = 2.3 V; I_{OH} = -6 mA	2.0		
		V_{CC} = 2.3 V; I_{OH} = -12 mA	1.8		
		V_{CC} = 2.3 V; I_{OH} = -18 mA	1.7		
		V_{CC} = 2.7 V; I_{OH} = -12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = -18 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = -24 mA	2.2		
V_{OL}	LOW Level Output Voltage	1.65 V ≤ V_{CC} ≤ 3.6 V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 1.65 V; I_{OL} = 6 mA		0.3	
		V_{CC} = 2.3 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 2.3 V; I_{OL} = 18 mA		0.6	
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 18 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
I_I	Input Leakage Current	V_{IN} = V_{CC} or GND; V_{CC} = 3.6 V		±5.0	μA
$I_{I(HOLD)}$	Minimum Bushold Input Current	V_{CC} = 3.0 V, V_{IN} = 0.8 V	75		μA
		V_{CC} = 3.0 V, V_{IN} = 2.0 V	-75		
		V_{CC} = 2.3 V, V_{IN} = 0.7 V	45		
		V_{CC} = 2.3 V, V_{IN} = 1.6 V	-45		
		V_{CC} = 1.65 V, V_{IN} = 0.57 V	25		
		V_{CC} = 1.65 V, V_{IN} = 1.07 V	-25		
$I_{I(OD)}$	Minimum Bushold Over-Drive Current Needed to Change State	V_{CC} = 3.6 V, (Note 3)	450		μA
		V_{CC} = 3.6 V, (Note 4)	-450		
		V_{CC} = 2.7 V, (Note 3)	300		
		V_{CC} = 2.7 V, (Note 4)	-300		
		V_{CC} = 1.95 V, (Note 3)	200		
		V_{CC} = 1.95 V, (Note 4)	-200		
I_{OZ}	3-State Output Current	V_O = V_{CC} or GND; V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}		±10	μA
I_{CC}	Quiescent Supply Current (Note 5)	1.65 V ≤ V_{CC} ≤ 3.6 V; V_I = GND or V_{CC}		20	μA
ΔI_{CC}	Increase in I_{CC} per Input	2.7 V < V_{CC} ≤ 3.6 V; V_{IH} = V_{CC} - 0.6 V		750	μA

2. These values of V_I are used to test DC electrical characteristics only.
3. An external driver must source at least the specified current to switch from LOW-to-HIGH.
4. An external driver must sink at least the specified current to switch from HIGH-to-LOW.
5. Outputs disabled or 3-state only.

AC CHARACTERISTICS (Note 6; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500\ \Omega$)

Symbol	Parameter	Waveform	Limits						Unit
			T_A = -40°C to +85°C						
			V_{CC} = 3.0 V to 3.6 V		V_{CC} = 2.3 V to 2.7 V		V_{CC} = 1.65 V to1.95 V		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	0.6 0.6	3.5 3.5	0.8 0.8	4.2 4.2	1.5 1.5	8.4 8.4	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	0.6 0.6	4.5 4.5	0.8 0.8	5.6 5.6	1.5 1.5	9.8 9.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	0.6 0.6	3.6 3.6	0.8 0.8	4.0 4.0	1.5 1.5	7.2 7.2	ns
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 7)			0.5 0.5		0.5 0.5		0.75 0.75	ns

6. For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

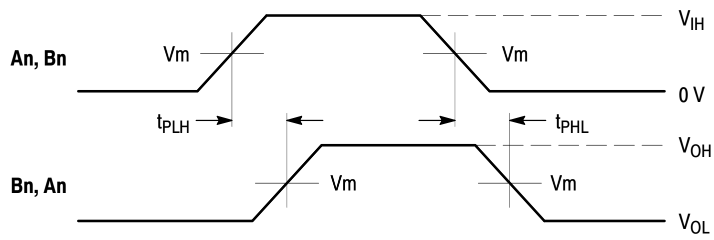
Symbol	Characteristic	Condition	T_A = +25°C Typ	Unit
V_{OLP}	Dynamic LOW Peak Voltage (Note 8)	V_{CC} = 1.8 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	0.3	V
		V_{CC} = 2.5 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	0.7	
		V_{CC} = 3.3 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	1.0	
V_{OLV}	Dynamic LOW Valley Voltage (Note 8)	V_{CC} = 1.8 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	-0.3	V
		V_{CC} = 2.5 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	-0.7	
		V_{CC} = 3.3 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	-1.0	
V_{OHV}	Dynamic HIGH Valley Voltage (Note 9)	V_{CC} = 1.8 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	1.3	V
		V_{CC} = 2.5 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	1.7	
		V_{CC} = 3.3 V, C_L = 30 pF, $V_{IH} = V_{CC}$, V_{IL} = 0 V	2.0	

8. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.
9. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the HIGH state.

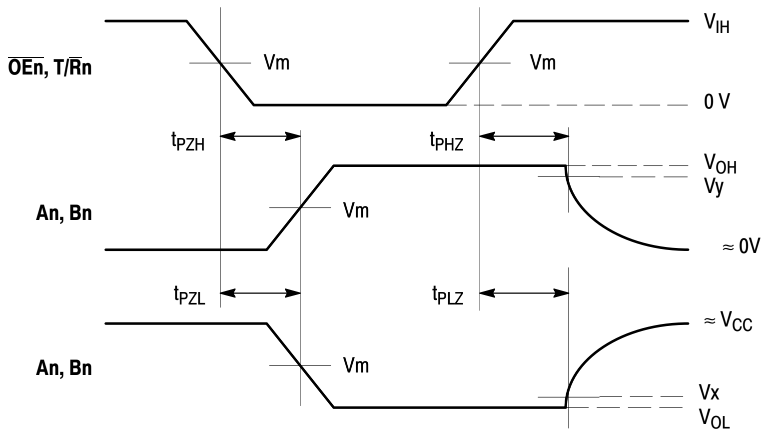
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 10	6	pF
C_{OUT}	Output Capacitance	Note 10	7	pF
C_{PD}	Power Dissipation Capacitance	Note 10, 10 MHz	20	pF

10. V_{CC} = 1.8, 2.5 or 3.3 V; V_I = 0 V or V_{CC}.



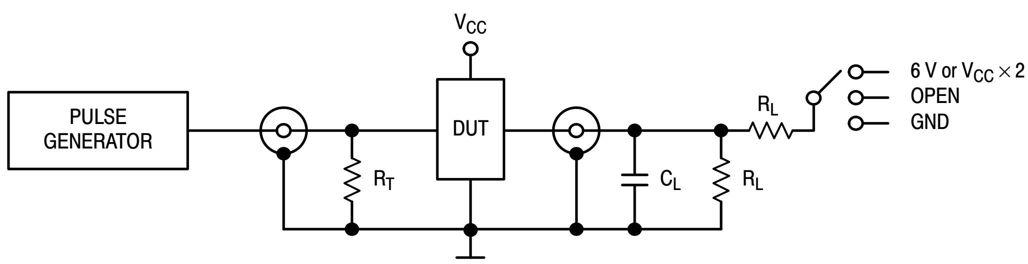
WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F$ = 2.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 3. AC Waveforms

Symbol	V_{CC}		
	3.3 V ± 0.3 V	**2.5 V ± 0.2 V**	**1.8 V ± 0.15 V**
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_m	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_x	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_y	V_{OH} - 0.3 V	V_{OH} - 0.15 V	V_{OH} - 0.15 V



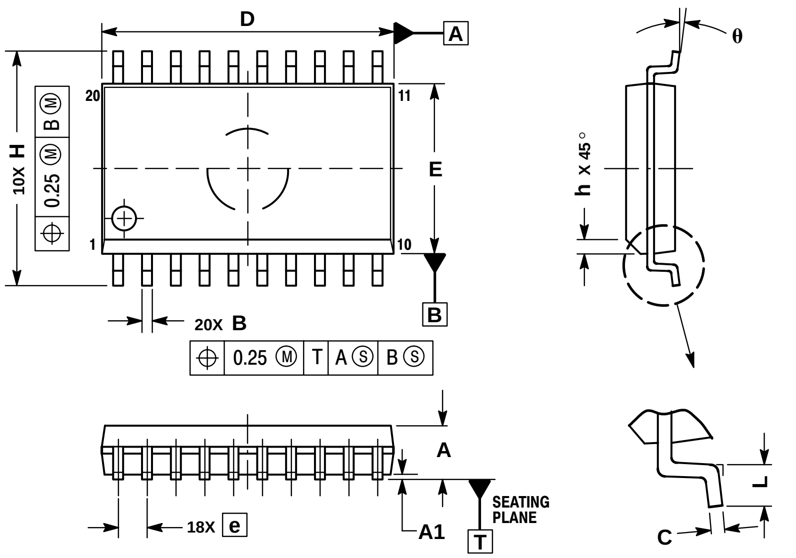
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at V_{CC} = 3.3 ± 0.3 V; V_{CC}× 2 at V_{CC} = 2.5 ± 0.2 V; 1.8 V ± 0.15 V
t_{PZH}, t_{PHZ}	GND

C_L = 30 pF or equivalent (Includes jig and probe capacitance)
R_L = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 4. Test Circuit

PACKAGE DIMENSIONS

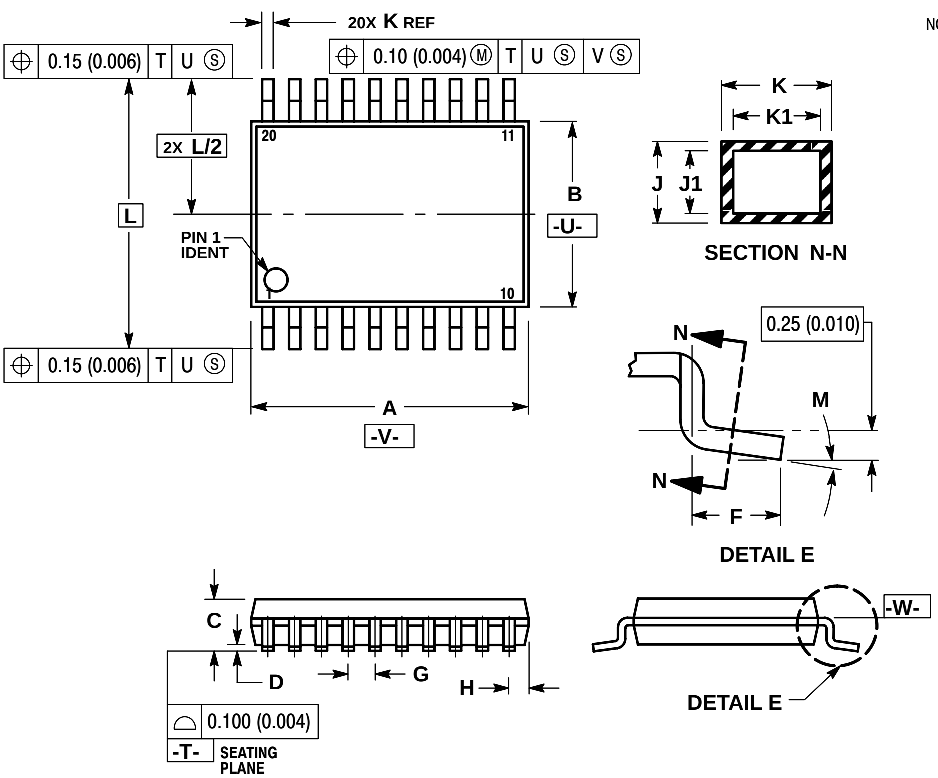
SO-20
DW SUFFIX
CASE 751D-05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE A

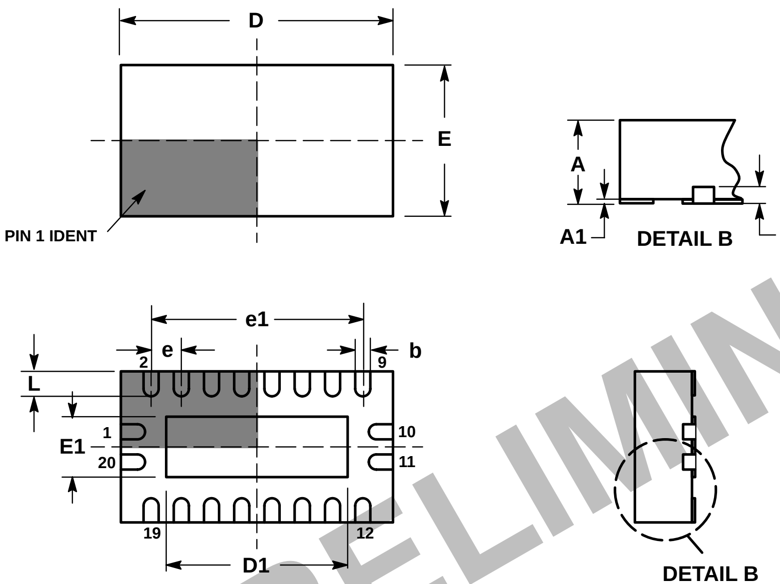


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

DQFN
SUFFIX TBD
CASE TBD
ISSUE O



NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS.
2. DIMENSIONS A, D, AND E DO NOT INCLUDE MOLD PROTRUSION.
3. MAXIMUM MOLD PROTRUSION 0.075 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.00 BSC	
A1	0.00	0.05
b	0.18	0.30
C	0.20 BSC	
D	4.4	4.6
D1	2.85	3.15
E	2.4	2.6
E1	0.85	1.15
e	0.5 BSC	
e1	3.5 BSC	
L	0.3	0.5

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