



MK3732-05 Low Phase Noise VCXO+Multiplier

Description

The MK3732-05 is a low cost, low jitter, high performance VCXO and PLL clock synthesizer designed to replace expensive discrete VCXOs and multipliers. The on-chip Voltage Controlled Crystal Oscillator (VCXO) accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ± 100 ppm. Using ICS' patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 10 MHz to 18 MHz pullable crystal input to produce one or two output clocks.

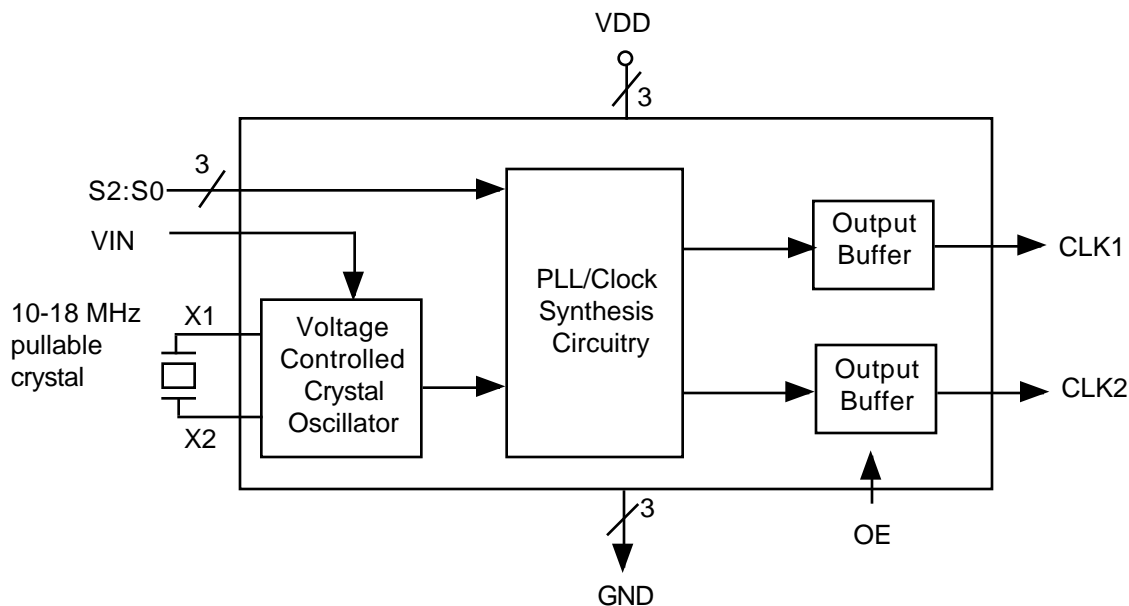
ICS manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult ICS to eliminate VCXOs, crystals and oscillators from your board.

For a 5 V version of this chip use the MK2732-05.

Features

- Packaged in 16 pin narrow SOIC
- Replaces a VCXO and multiplier
- Uses an inexpensive pullable crystal
- Output clocks up to 108 MHz
- On-chip patented VCXO with pull range of 200 ppm (± 100 ppm) minimum
- VCXO tuning voltage of 0 to 3.3 V
- Zero ppm synthesis error in both clocks
- Advanced, low power, sub-micron CMOS process
- 3.3 V operating voltage
- Industrial temperature version available

Block Diagram

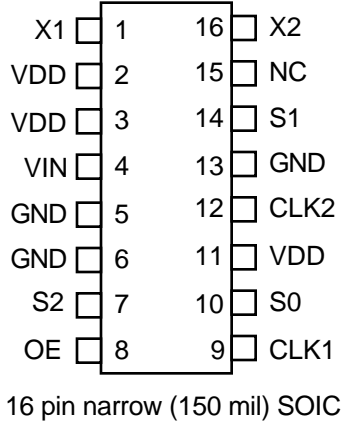




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Pin Assignment



Clock Select Table

S2	S1	S0	CLK1	CLK2
0	0	0	REF/4	REF/2
0	0	M	OFF	x0.666
0	0	1	OFF	x2.6666
0	1	0	OFF	x4
0	1	M	OFF	x1.5
0	1	1	OFF	x1.3333
1	0	0	Test	Test
1	0	M	OFF	x4
1	0	1	OFF	x2
1	1	0	OFF	x3
1	1	M	OFF	x5
1	1	1	OFF	x6

0=connect directly to GND, 1=connect directly to VDD, OFF=output stopped low.

Pin Descriptions

Number	Name	Type	Description
1	X1	XI	Crystal connection. Connect to a pullable crystal of 10-18 MHz.
2, 3	VDD	P	Connect to +3.3V.
4	VIN	VI	Voltage Input to VCXO. Zero to 3.3 V signal which controls the frequency of the VCXO.
5, 6, 13	GND	P	Connect to ground.
7	S2	I	Select input pin 2. Selects outputs per table above.
8	OE	I	Output Enable. Tri-states outputs when low.
9	CLK1	O	Clock Output pin 1 per table above.
10	S0	TI	Select input pin 0. Selects outputs per table above.
11	VDD	P	Connect to +3.3V.
12	CLK2	O	Clock Output pin 2 per table above.
14	S1	I	Select input pin 1. Selects outputs per table above.
15	NC	-	Nothing is connected internally to this pin.
16	X2	XO	Crystal connection. Connect to a pullable crystal of 10-18 MHz.

Key: I = Input with internal pull-up resistors; TI = tri-level input; O = output; P = power supply connection; VI = analog voltage input; XI, XO = crystal pins.

External Components

The MK3732-05 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between VDD and GND on pins 3 and 5, and VDD and GND on pins 11 and 13, as close to the MK3732-05 as possible. A series termination resistor of 33 Ω may be used for each clock output. The input crystal must be connected as close to the chip as possible. The input crystal should be a fundamental mode, parallel resonant, pullable, AT cut. See page 4 for crystal specifications. Consult ICS for recommended suppliers. **IMPORTANT** - consult the application note MAN05 for layout guidelines.



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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Core Operating Voltage, VDD		3.15	3.3	3.45	V
Input High Voltage, VIH, X1 pin only		VDD/2 + 1	VDD/2		V
Input Low Voltage, VIL, X1 pin only			VDD/2	VDD/2 - 1	V
Input High Voltage, VIH, binary inputs	S2, S1, OE	2			V
Input Low Voltage, VIL, binary inputs	S2, S1, OE			0.8	V
Input High Voltage, VIH, trinary input	S0, pin 10	VDD -0.5			V
Input Low Voltage, VIL, trinary input	S0, pin 10			0.5	V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD - 0.4			V
Operating Supply Current, IDD	No Load		12		mA
Short Circuit Current	Each output		±50		mA
Input Capacitance	S2:S0, OE		7		pF
Frequency synthesis error	Both clocks			0	ppm
VIN, VCXO control voltage		0		3.3	V
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Crystal Frequency		10		18	MHz
Output Clock Frequency		2.5		108	MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40		60	%
Maximum Absolute Jitter			±200		ps
Phase Noise, relative to carrier	10 kHz offset		-115		dBc/Hz
Output pullability, note 2	0V VIN 3.3V	±100			ppm

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
 2. With an ICS approved pullable crystal.

See application note MAN05 for crystal information. MAN05 is available on the internet at www.icst.com/pdf/man05.pdf

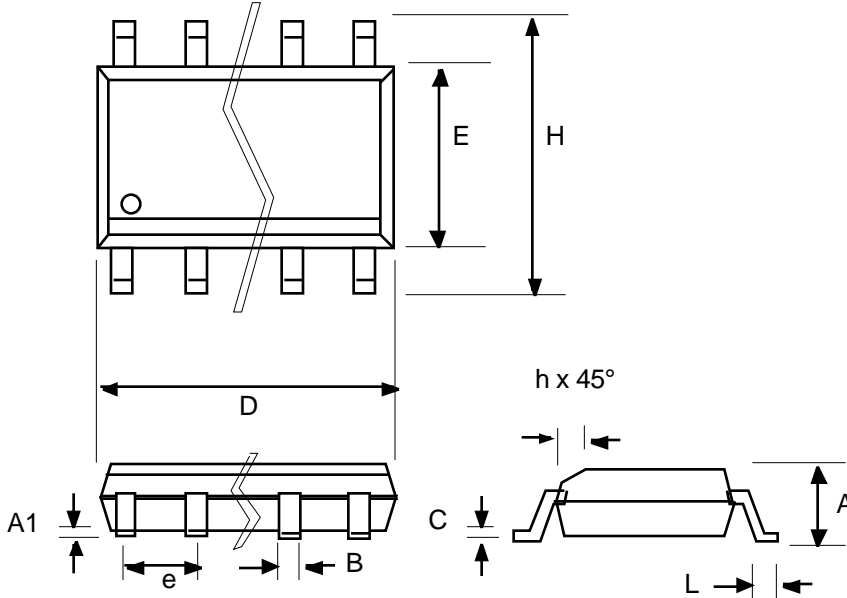


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Package Outline and Package Dimensions
 (For current dimensional specifications, see JEDEC Publication No. 95.)

16 pin SOIC narrow



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.075	0.098	1.91	2.40
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK3732-05S	MK3732-05S	tubes	16 pin SOIC	0-70 °C
MK3732-05STR	MK3732-05S	tape and reel	16 pin SOIC	0-70 °C
MK3732-05SI	MK3732-05SI	tubes	16 pin SOIC	-40-85°C
MK3732-05SITR	MK3732-05SI	tape and reel	16 pin SOIC	-40-85°C

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