INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT

TC518512AF / AFT / ATR – 70, – 80

SILICON GATE CMOS

524,288 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

TENTATIVE

DESCRIPTION

The TC518512A Family is a 4M bit high speed CMOS Pseudo Static RAM organized as 524,288 words by 8 bits. The TC518512A Family utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V±10%. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operation - auto refresh and self refresh. The TC518512A Family also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/W, thus being easy to interface with microprocessor.

The TC518512A Family is moulded in Small Out line plastic flat Package and Thin Small Outline Package.

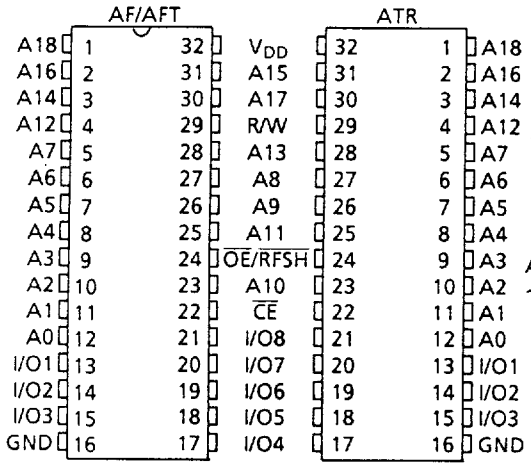
FEATURES

- Organization: 4M bit (524,288 word × 8bit)
- Fast Access Time and Low Power Dissipation

		TC518512A Family	
		-70	-80
t_{CEA} $\overline{CE}$ Access Time		70ns	80ns
t_{OEA} $\overline{OE}$ Access Time		30ns	30ns
t_{RC} Cycle Time		115ns	130ns
Power Dissipation		385mW	330mW
Self Refresh Current	5.5V	100μA	
	3.6V	50μA	
	3.3V	40μA	

- Single Power Supply : 5V±10%
- Data Retention Supply Voltage : 2.7V ~ 5.5V
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- All inputs and outputs : TTL compatible
- 2048 refresh cycle / 32ms
- Logic Compatible: SRAM R/W Pin
- Package : TC518512AF : SOP32-P-525
  TC518512AFT : TSOP32-P-400
  TC518512ATR : TSOP32-P-400A

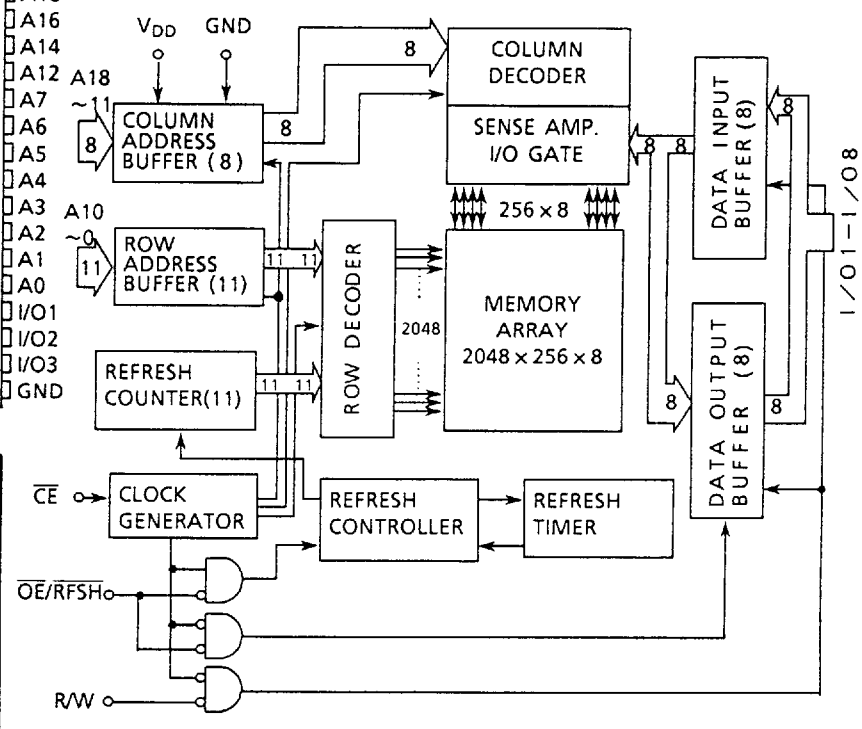
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A18	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable Input Refresh Input
$\overline{CE}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	$\overline{OE}$/$\overline{RFSH}$	R/W	A0 ~ A18	I/O1 ~ 8	CONDITION
L	L	H	V*	OUT	Read
L	*	L	V*	IN	Write
L	H	H	V*	HZ	$\overline{CE}$ only Refresh
H	L	*	*	HZ	Auto/Self Refresh
H	H	*	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· V_{IH} or V_{IL}
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}	Input Voltage	– 1.0~7.0	V	1
V_{OUT}	Output Voltage	– 1.0~7.0	V	
V_{DD}	Power Supply Voltage	– 1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	– 55~150	°C	
T_{SOLDER}	Soldering Temperature (10s)	260	°C	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	
V_{IL}	Input Low Voltage	– 1.0	–	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	NOTE
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	70ns version	–	50	70	mA	3, 4
		80ns version	–	45	60		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{OE/RFSH}$ = V_{IH}		–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} – 0.2V, $\overline{OE/RFSH}$ = V_{DD} – 0.2V		–	–	100	μA	
I_{DDF1}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{IH}, $\overline{OE/RFSH}$ = V_{IL}		–	–	1	mA	
I_{DDF2}	Self Refresh Current (Average Current) $\overline{CE}$ = V_{DD} – 0.2V, $\overline{OE/RFSH}$ = 0.2V		–	–	100	μA	
I_{DDF3}	Auto Refresh Current (Average Current) ($\overline{OE/RFSH}$ cycling : tFC = tFC min)	70ns version	–	–	70	mA	3
		80ns version	–	–	60		
I_{DDF4}	$\overline{CE}$ only Refresh Current (Average Current) ($\overline{CE}$, Address cycling : tRC = tRC min)	70ns version	–	–	70	mA	3
		80ns version	–	–	60		
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other Inputs not under test = 0V		– 10	–	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE}$ = V_{IH} or $\overline{OE/RFSH}$ = V_{IH} or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}		– 10	–	10	μA	
V_{OH}	Output High Level I_{OH} = – 1.0mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 2.1mA		–	–	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A18)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE/RFSH}$, R/W)	–	7	pF
C_{I0}	Input / Output Capacitance	–	7	pF

Note) This parameter periodically sampled is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

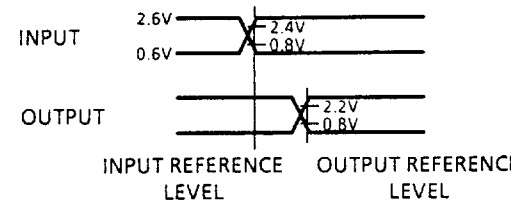
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	– 70		– 80		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	115	–	130	–	ns	
t_{RMW}	Read Modify Write Cycle Time	165	–	180	–	ns	
t_{CE}	$\overline{CE}$ Pulse Width	70	10,000	80	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	35	–	40	–	ns	
t_{CEA}	$\overline{CE}$ Access Time	–	70	–	80	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	30	–	30	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	20	–	20	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	20	0	20	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	20	0	20	ns	9
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	–	10	–	ns	9
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	–	0	–	ns	9
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	
t_{WP}	Write Pulse Width	25	–	25	–	ns	
t_{WCH}	Write Command Hold Time	40	–	40	–	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	25	–	25	–	ns	
t_{DSW}	Data Set-Up Time from R/W	20	–	20	–	ns	10
t_{DSC}	Data Set-Up Time from $\overline{CE}$	20	–	20	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	15	–	20	–	ns	11
t_{FC}	Auto Refresh Cycle Time	130	–	130	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	–	40	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	ns	12
t_{FRS}	$\overline{CE}$ Delay Time form $\overline{RFSH}$ (Self Refresh)	160	–	160	–	ns	12
t_{REF}	Refresh Period (2048 cycle, A0~A10)	–	32	–	32	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO}, I_{DDF3} and I_{DDF4} depend on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements assume t_T = 5ns.
7) Timing reference level

Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V

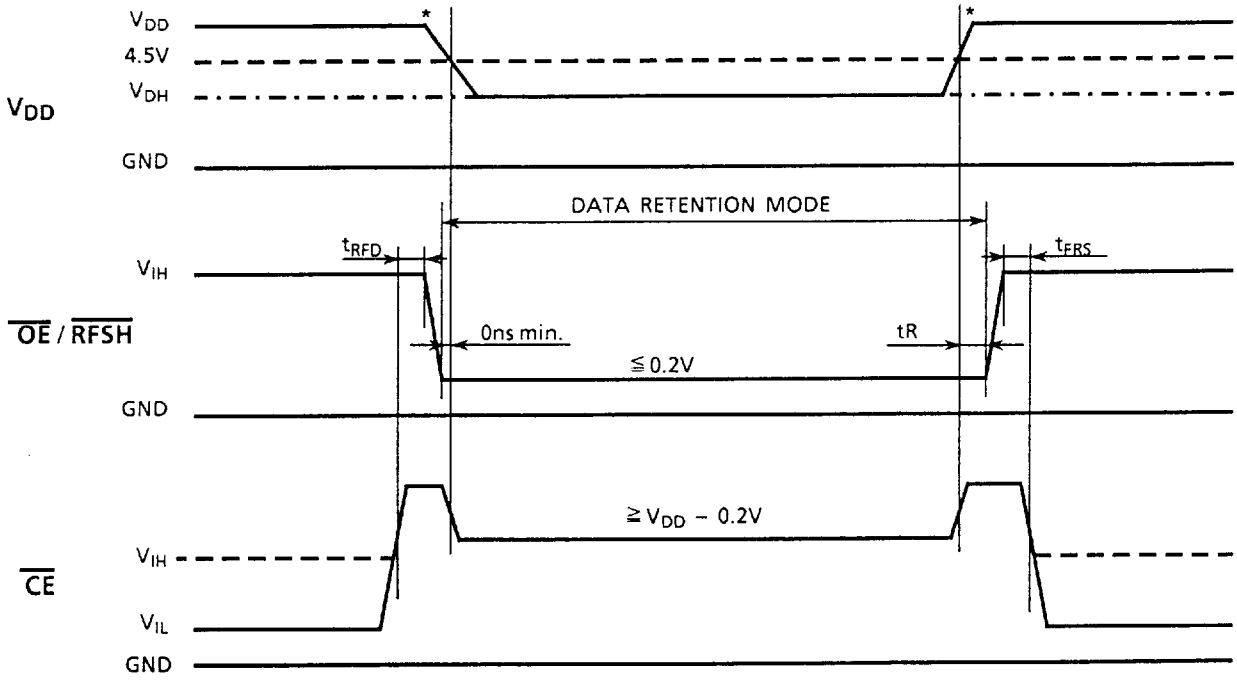


8) Measured with a load equivalent to 1 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for device proper operation in the following conditions.
    - after self refresh
    - in case of $\overline{OE}/\overline{RFSH}$ = "L" after power-up

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.7	–	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.3V	–	–	40	μA
		V_{DH} = 3.6V	–	–	50	μA
		V_{DH} = 5.5V	–	–	100	μA
t_R	Recovery Time		5	–	–	mS

* The raising and falling slope of V_{DD} must be more than 50ms in order to operate the device safely. (20ms/V)



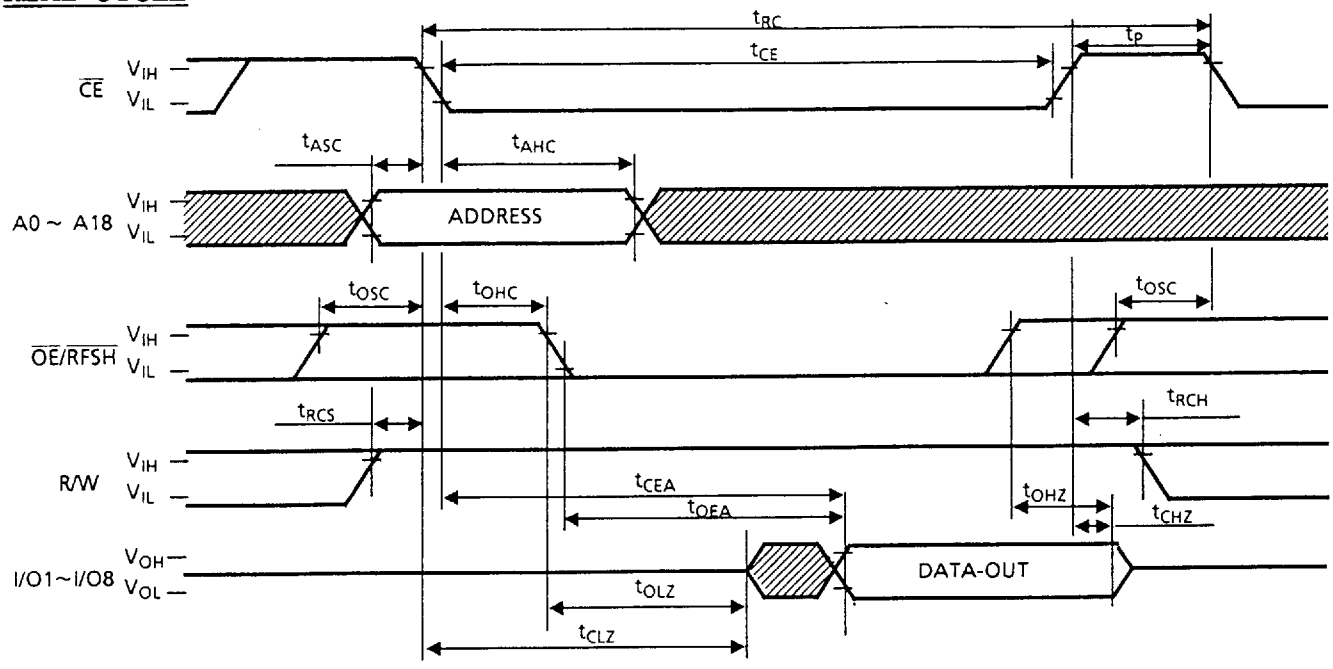
(Note)◦ R/W, A0~A18 = V_{IH} or V_{IL}

◦ I_{DDF1} is applied in $\overline{OE}$ / $\overline{RFSH}$ = V_{IL} max., $\overline{CE}$ = V_{IH} min.

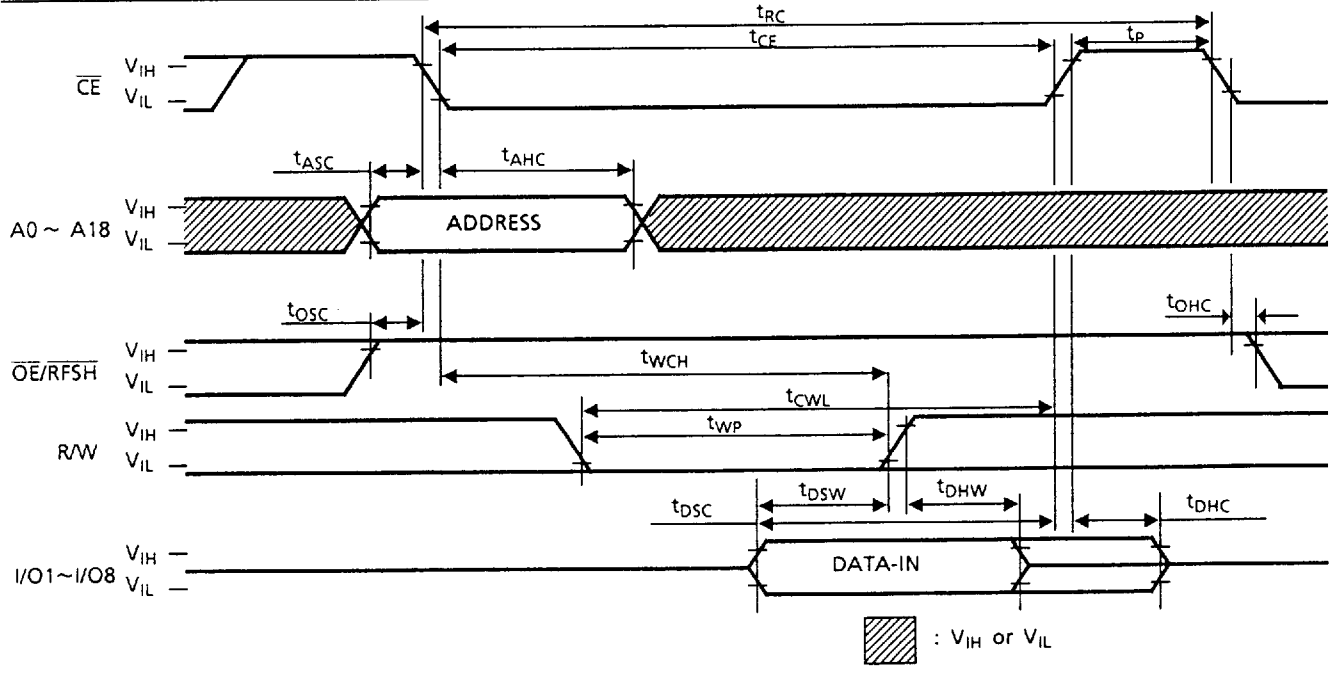
◦ At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 2048cycle / 32ms is required.

TIMING WAVEFORMS

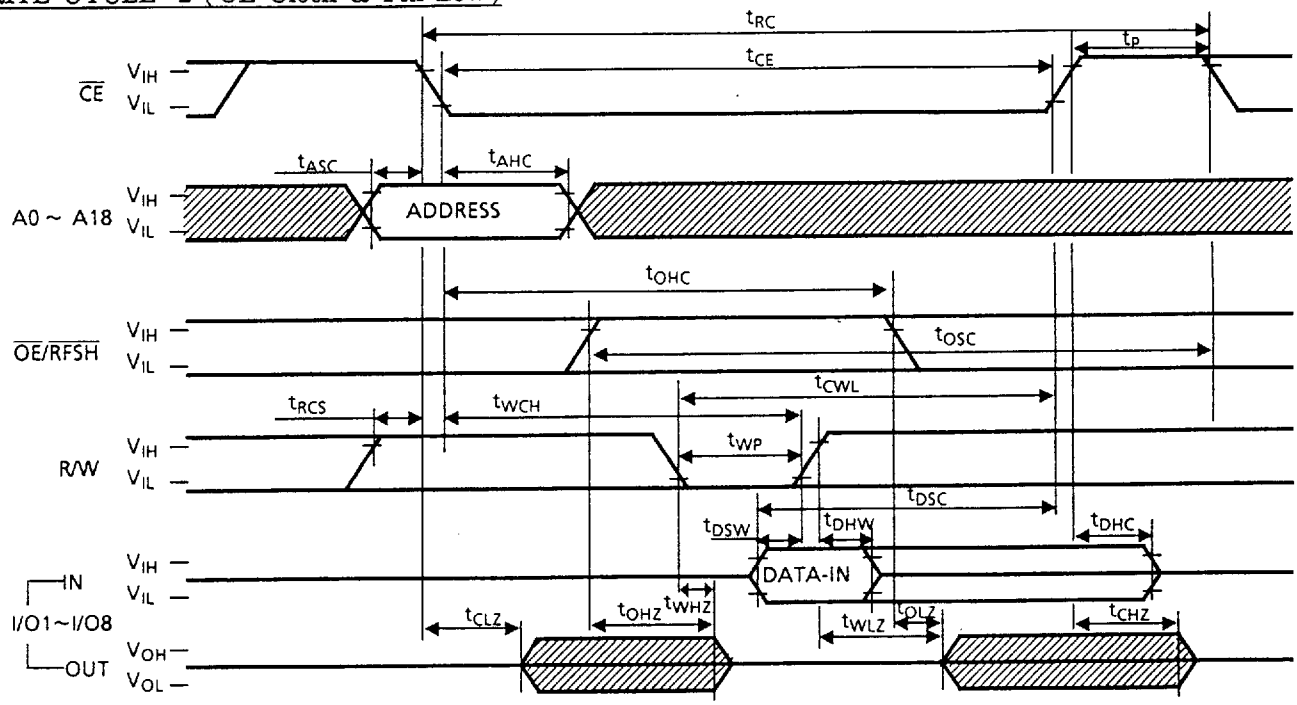
READ CYCLE



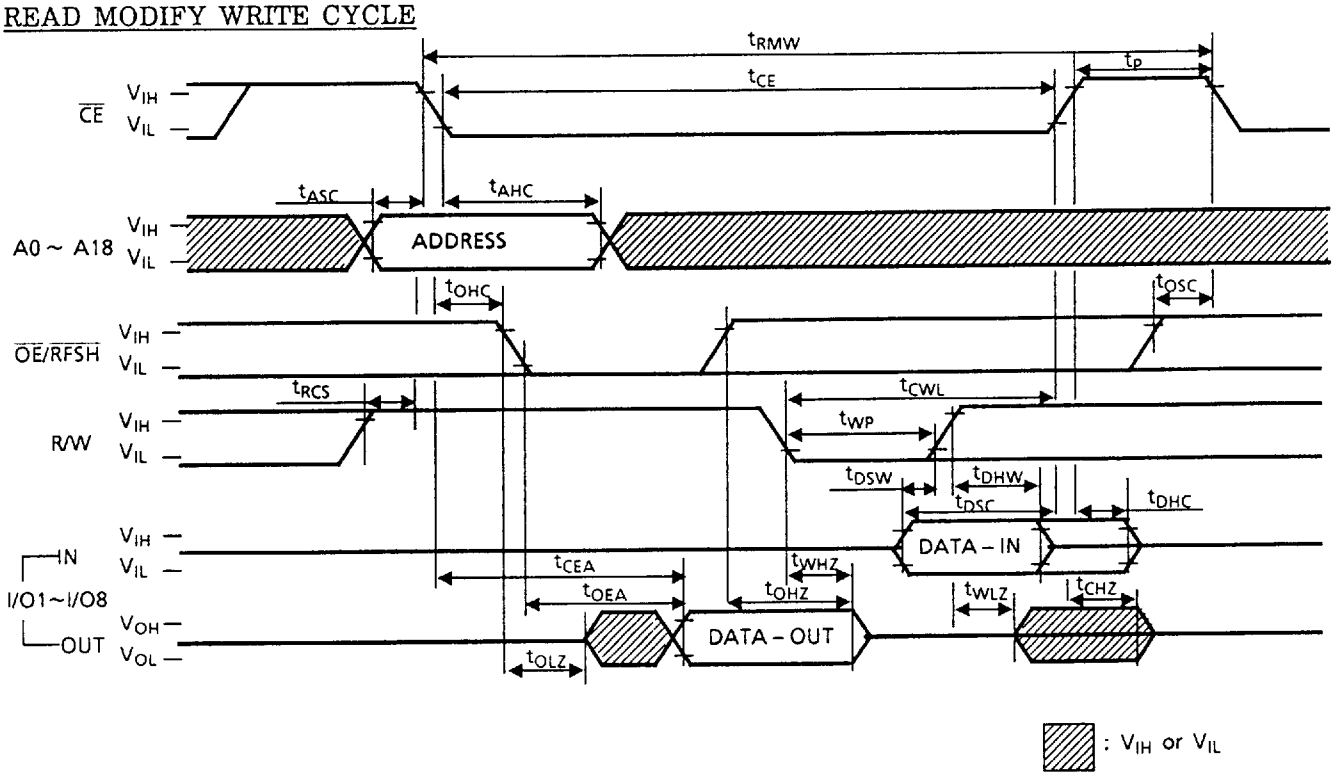
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



WRITE CYCLE - 2 ($\overline{OE}$ Clock & Fix Low)

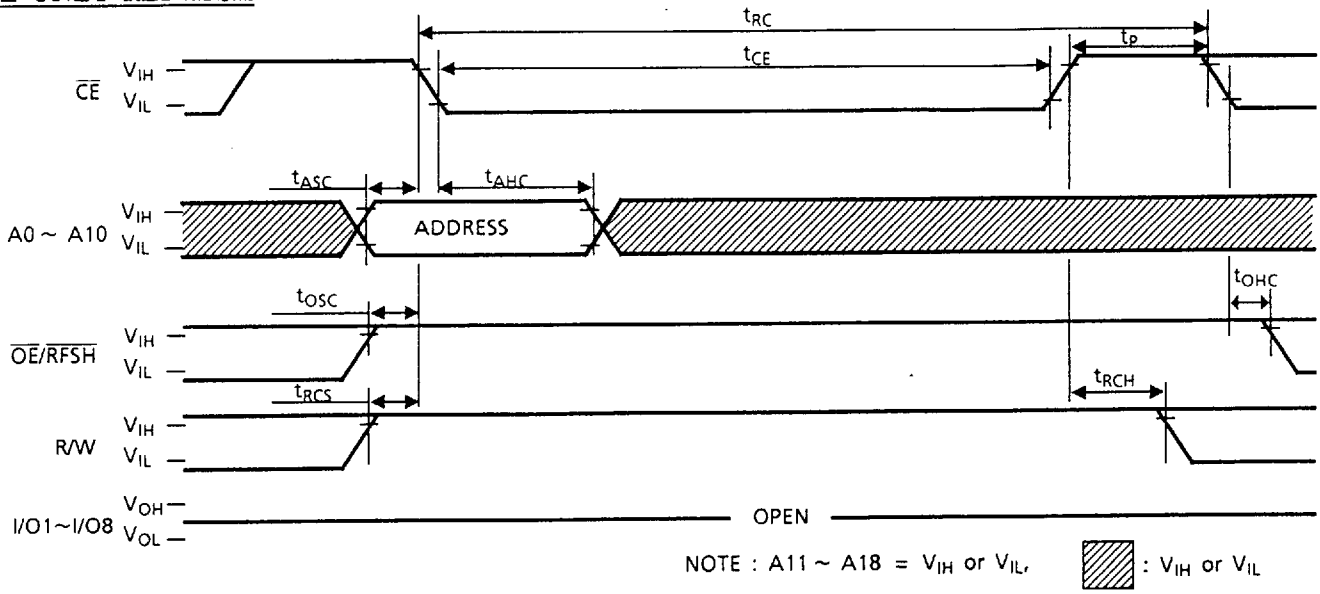


READ MODIFY WRITE CYCLE



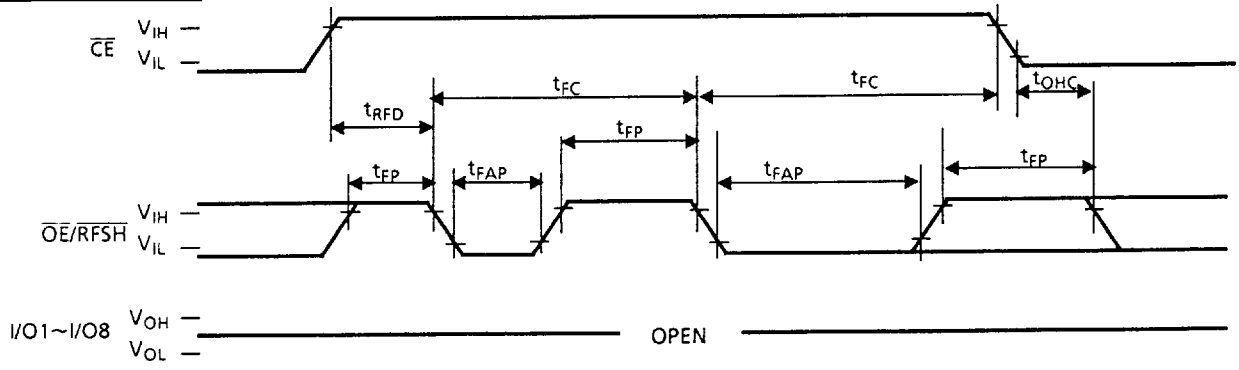
: V_{IH} or V_{IL}

$\overline{CE}$ ONLY REFRESH



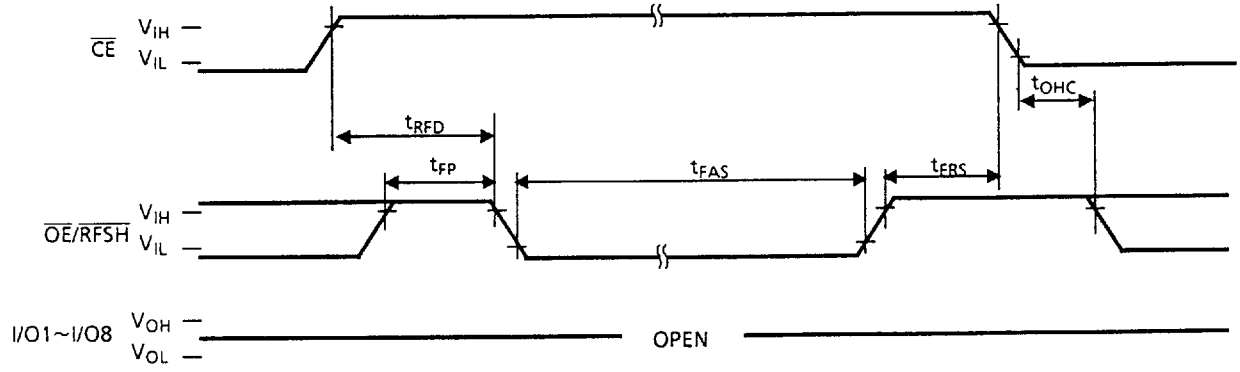
NOTE : A11 ~ A18 = V_{IH} or V_{IL}, ▨ : V_{IH} or V_{IL}

AUTO REFRESH



NOTE : R/W, A0 ~ A18 = V_{IH} or V_{IL}

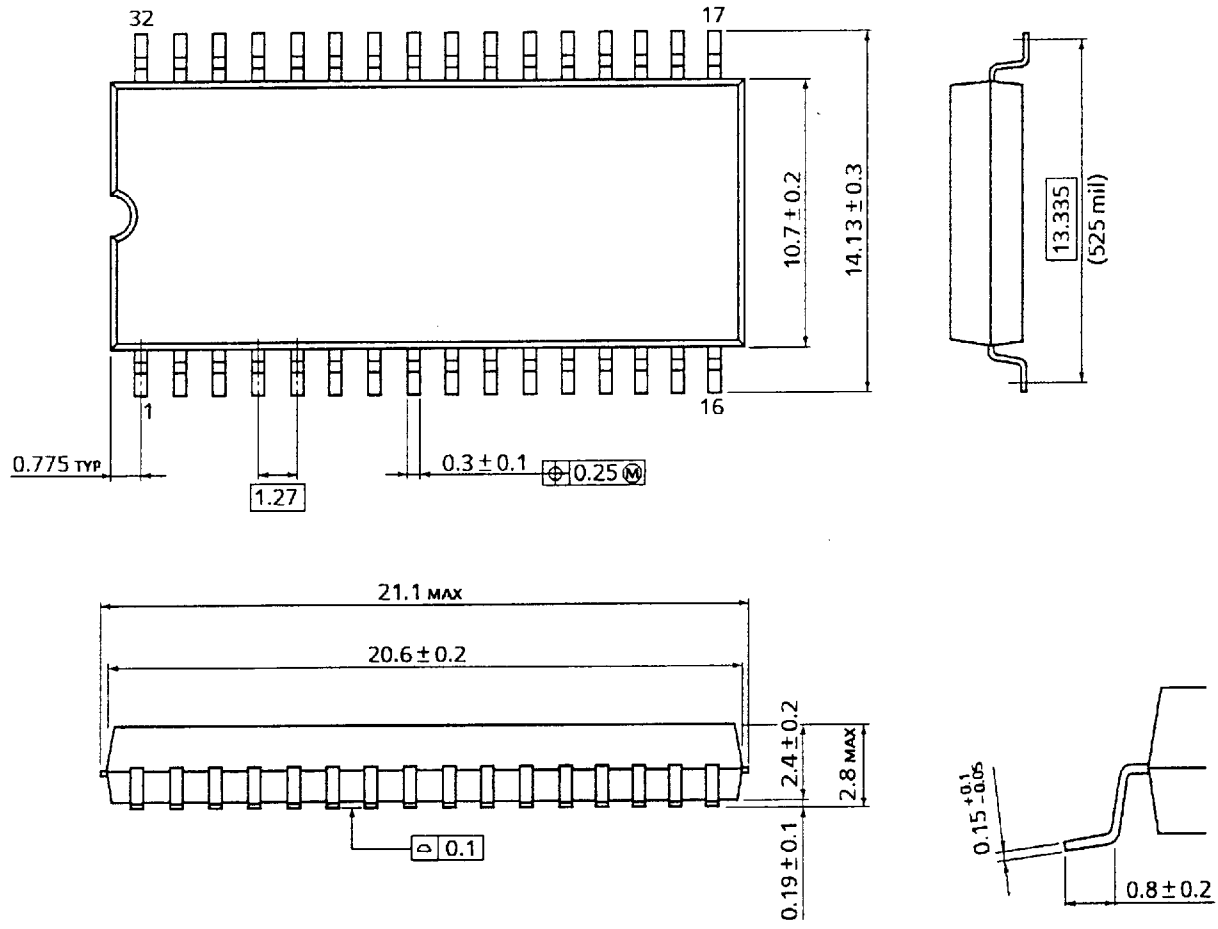
SELF REFRESH



NOTE : R/W, A0 ~ A18 = V_{IH} or V_{IL}

OUTLINE DRAWING (SOP32 – P – 525)

Unit in mm

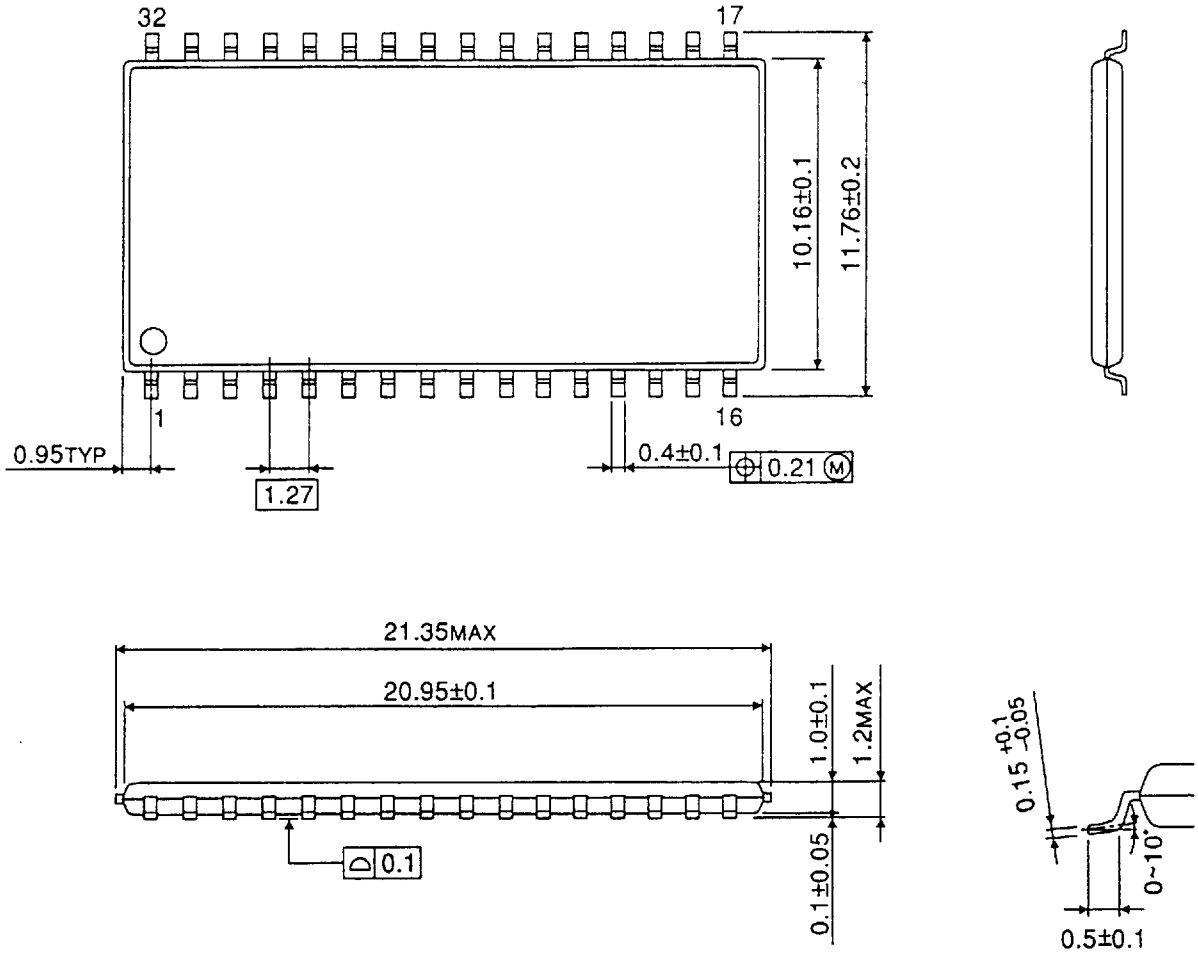


Weight : 1.10g (Typ.)

TC518512AF - 70, - 80

OUTLINE DRAWING (TSOP32 – P – 400)

Unit in mm

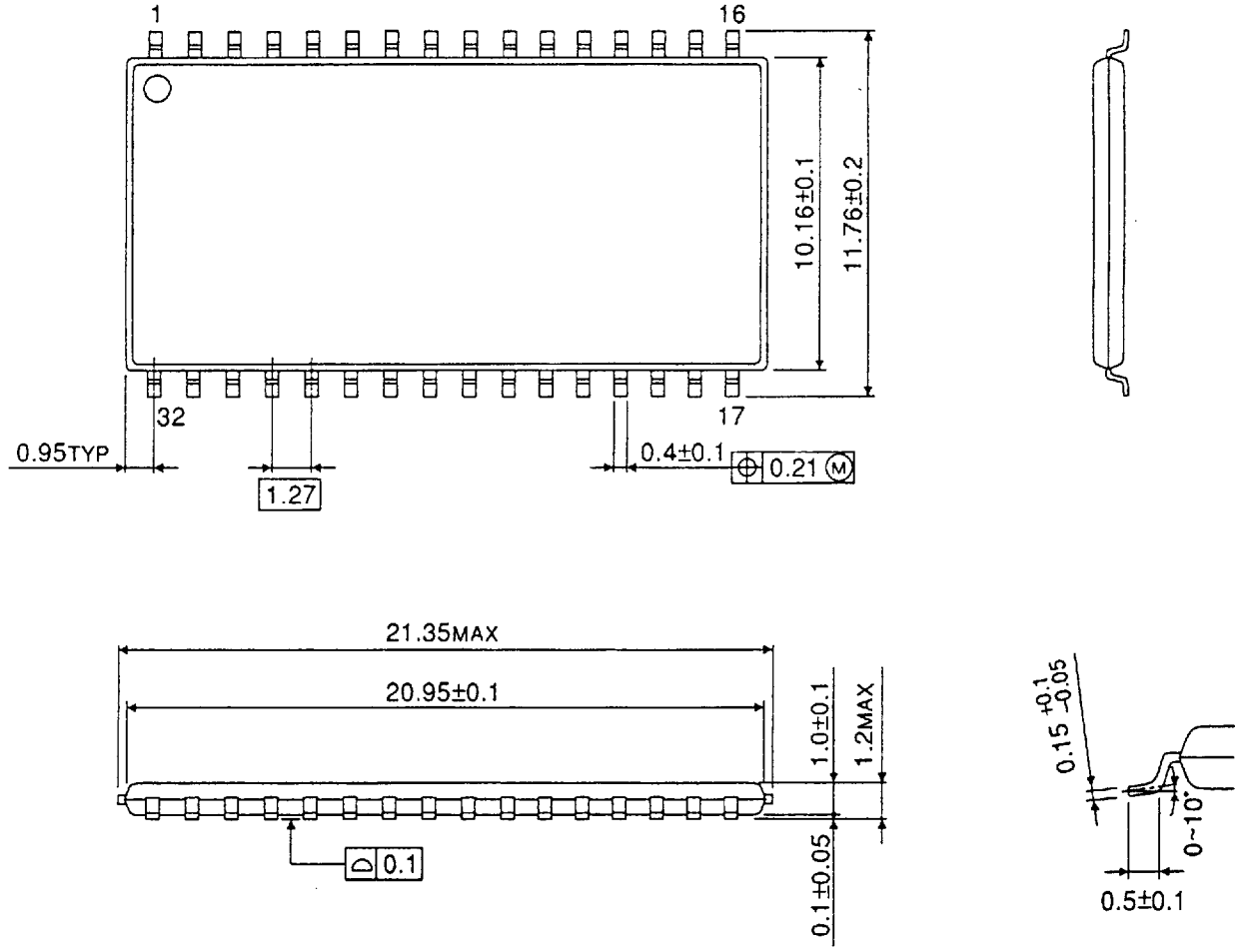


Weight : 0.51g (Typ.)

TC518512AFT - 70, - 80

OUTLINE DRAWING (TSOP32 – P – 400A)

Unit in mm



Weight : 0.51g (Typ.)

TC518512ATR - 70, - 80