

RENESAS LSIs

M5M5256DFP,VP-55LL,-70LL,-70LLI, -55XL,-70XL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5256DFP,VP is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 poly silicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

Especially the M5M5256DVP are packaged in a 28-pin thin small outline package.

FEATURE

Type	Access time (max)	Operating Temperature	Power supply current	
			Active (max)	Stand-by (max)
M5M5256DFP,VP-55LL M5M5256DFP,VP-70LL	55ns 70ns	0~70°C	50mA (V _{CC} =5.5V)	20µA (V _{CC} =5.5V)
M5M5256DFP,VP-70LLI	70ns	-40~85°C		40µA (V _{CC} =5.5V)
M5M5256DFP,VP-55XL M5M5256DFP,VP-70XL	55ns 70ns	0~70°C		5µA (V _{CC} =5.5V) 0.05µA (V _{CC} =3.0V, Typical)

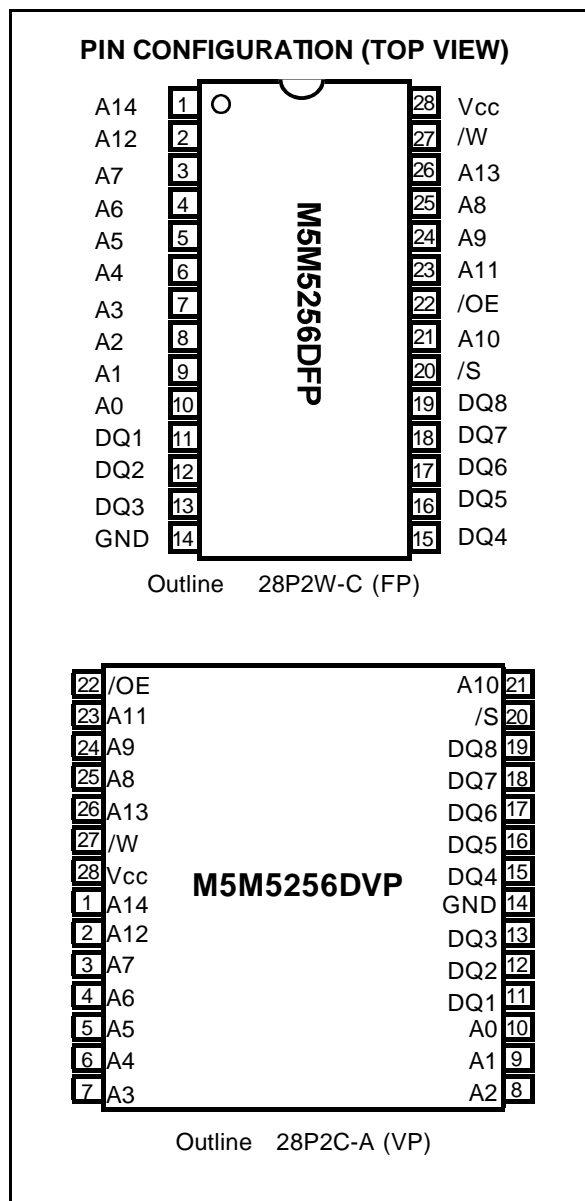
- Single +5V power supply
- No clocks, no refresh
- Data-Hold on +2.0V power supply
- Directly TTL compatible : all inputs and outputs
- Three-state outputs : OR-tie capability
- /OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Low stand-by current 0.05µA(typ.)

PACKAGE

M5M5256DFP : 28 pin 450 mil SOP
M5M5256DVP : 28pin 8 X 13.4 mm² TSOP

APPLICATION

Small capacity memory units



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FUNCTION

The operation mode of the M5M5256DFP,VP is determined by a combination of the device control inputs /S, /W and /OE. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with the low level /S. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable /OE directly controls the output stage. Setting the /OE at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting /W at a high level and /OE at a low level while /S are in an active state.

When setting /S at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /S. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

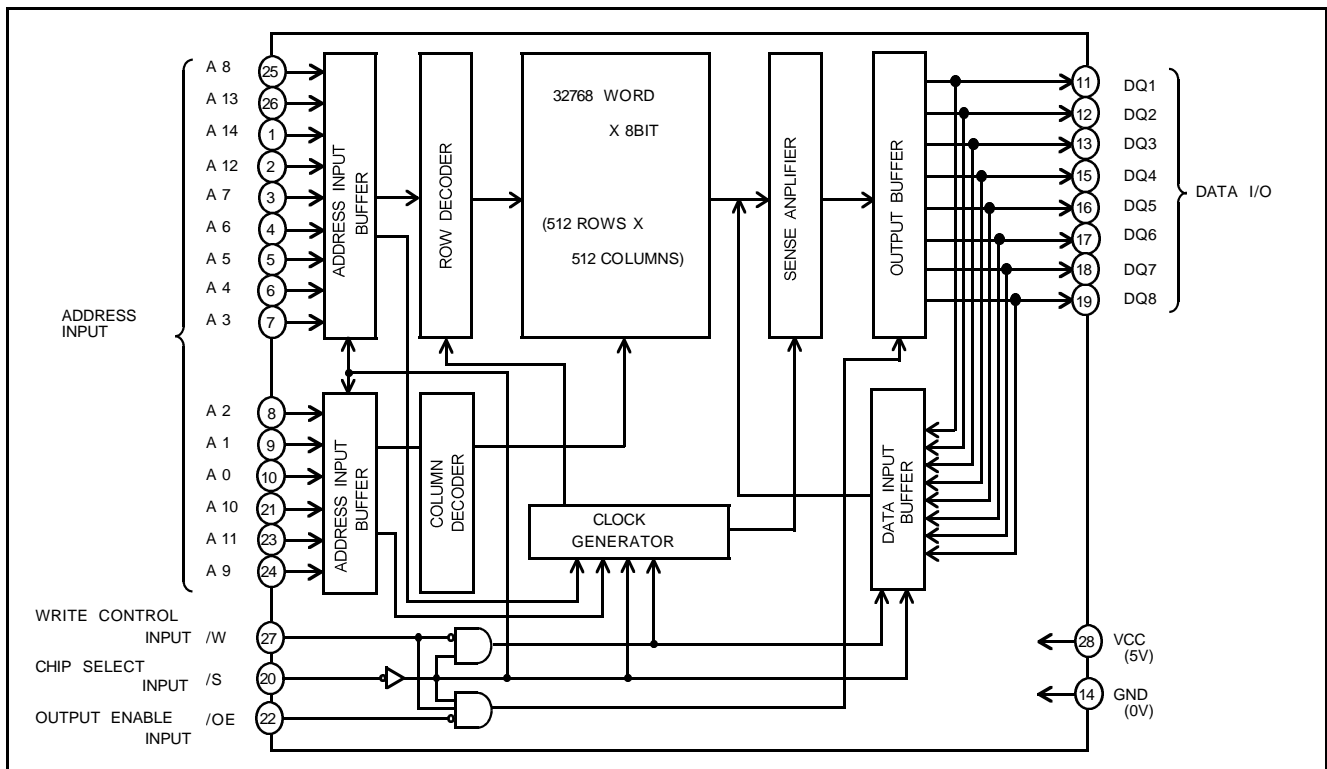
FUNCTION TABLE

/S	/W	/OE	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D _{IN}	Active
L	H	L	Read	D _{OUT}	Active
L	H	H		High-impedance	Active

Note • "H" and "L" in this table mean V_{IH} and V_{IL}, respectively.

• "X" in this table should be "H" or "L".

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	-0.3*~7.0	V
V _i	Input voltage		-0.3*~V _{cc} +0.3 (Max 7.0)	V
V _o	Output voltage		0~V _{cc}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature	-LL, -XL	0~70	°C
		-LLI	-40~85	
T _{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width < 30ns)

DC ELECTRICAL CHARACTERISTICS (V_{cc}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V _{IH}	High-level input voltage		2.2		V _{cc} +0.3	V	
V _{IL}	Low-level input voltage		-0.3*		0.8	V	
V _{OH1}	High-level output voltage 1	I _{OH} =-1mA	2.4			V	
V _{OH2}	High-level output voltage 2	I _{OH} =-0.1mA	V _{cc} -0.5			V	
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	V	
I _i	Input current	V _i =0~V _{cc}			±1	μA	
I _o	Output current in off-state	/S=V _{IH} or /OE=V _{IH} , V _{I/O} =0~V _{cc}			±1	μA	
I _{cc1}	Active supply current (AC, MOS level)	/S≤0.2V, Other inputs<0.2V or >V _{cc} -0.2V Output-open	55ns	30	45	mA	
			70ns	25	40		
			1MHz	2	4		
I _{cc2}	Active supply current (AC, TTL level)	/S=V _{IL} , other inputs=V _{IH} or V _{IL} Output-open	55ns	30	50	mA	
			70ns	25	45		
			1MHz	4	8		
I _{cc3}	Stand-by current	/S>V _{cc} -0.2V, other inputs=0~V _{cc}	~25°C	-LL, -LLI		2	μA
				-XL	0.1	0.4	
			~40°C	-LL, -LLI		6	
				-XL		1.2	
			~70°C	-LL, -LLI		20	
-XL		5					
~85°C	-LLI		40				
I _{cc4}	Stand-by current	/S=V _{IH} , other inputs=0~V _{cc}			3	mA	

* -3.0V in case of AC (Pulse width < 30ns)

CAPACITANCE (V_{cc}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _i	Input capacitance	V _i =GND, V _i =25mVrms, f=1MHz			6	pF
C _o	Output capacitance	V _o =GND, V _o =25mVrms, f=1MHz			8	pF

Note 0: Direction for current flowing into an IC is positive (no mark).

1: Typical value is one at T_a = 25°C.

2: C_i, C_o are periodically sampled and are not 100% tested.

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AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, unless otherwise noted)

(1) READ CYCLE

Symbol	Parameter	Limits				Unit
		-55LL, 55XL		-70LL, -70LLI, -70 XL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
$t_a(A)$	Address access time		55		70	ns
$t_a(S)$	Chip select access time		55		70	ns
$t_a(OE)$	Output enable access time		30		35	ns
$t_{dis}(S)$	Output disable time after /S high		20		25	ns
$t_{dis}(OE)$	Output disable time after /OE high		20		25	ns
$t_{en}(S)$	Output enable time after /S low	5		5		ns
$t_{en}(OE)$	Output enable time after /OE low	5		5		ns
$t_v(A)$	Data valid time after address	10		10		ns

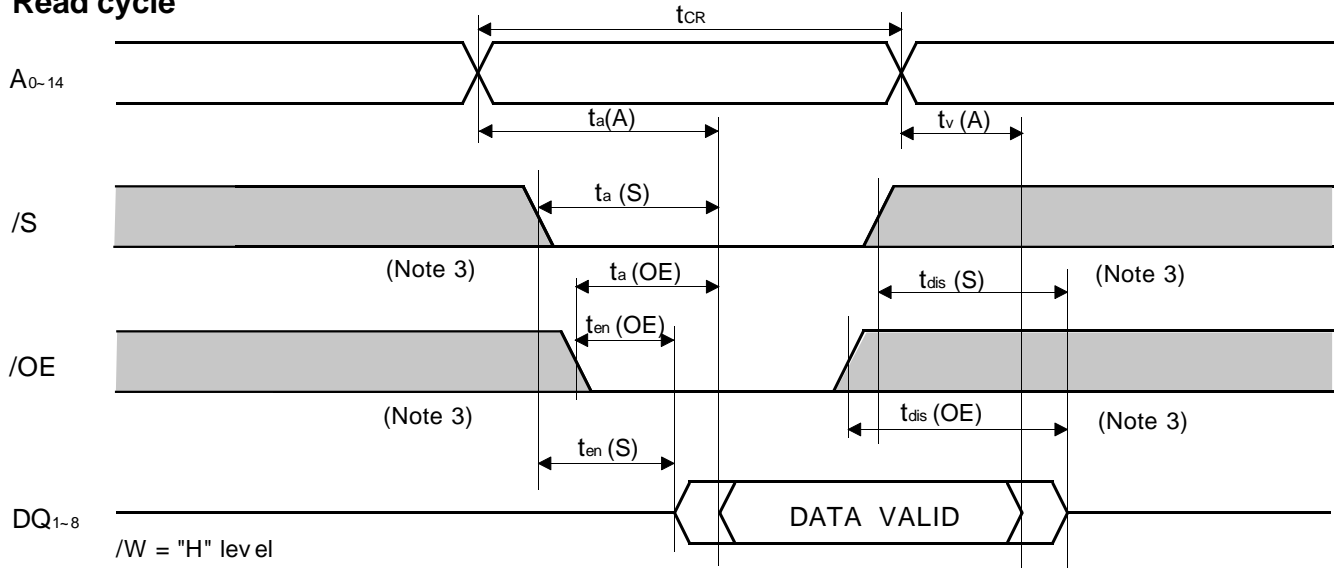
(2) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		-55LL, -55XL		-70LL, -70LLI, -70 XL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
$t_w(W)$	Write pulse width	40		50		ns
$t_{su}(A)$	Address setup time	0		0		ns
$t_{su}(A-WH)$	Address setup time with respect to /W high	50		65		ns
$t_{su}(S)$	Chip select setup time	50		65		ns
$t_{su}(D)$	Data setup time	25		30		ns
$t_h(D)$	Data hold time	0		0		ns
$t_{rec}(W)$	Write recovery time	0		0		ns
$t_{dis}(W)$	Output disable time from /W low		20		25	ns
$t_{dis}(OE)$	Output disable time from /OE high		20		25	ns
$t_{en}(W)$	Output enable time from /W high	5		5		ns
$t_{en}(OE)$	Output enable time from /OE low	5		5		ns

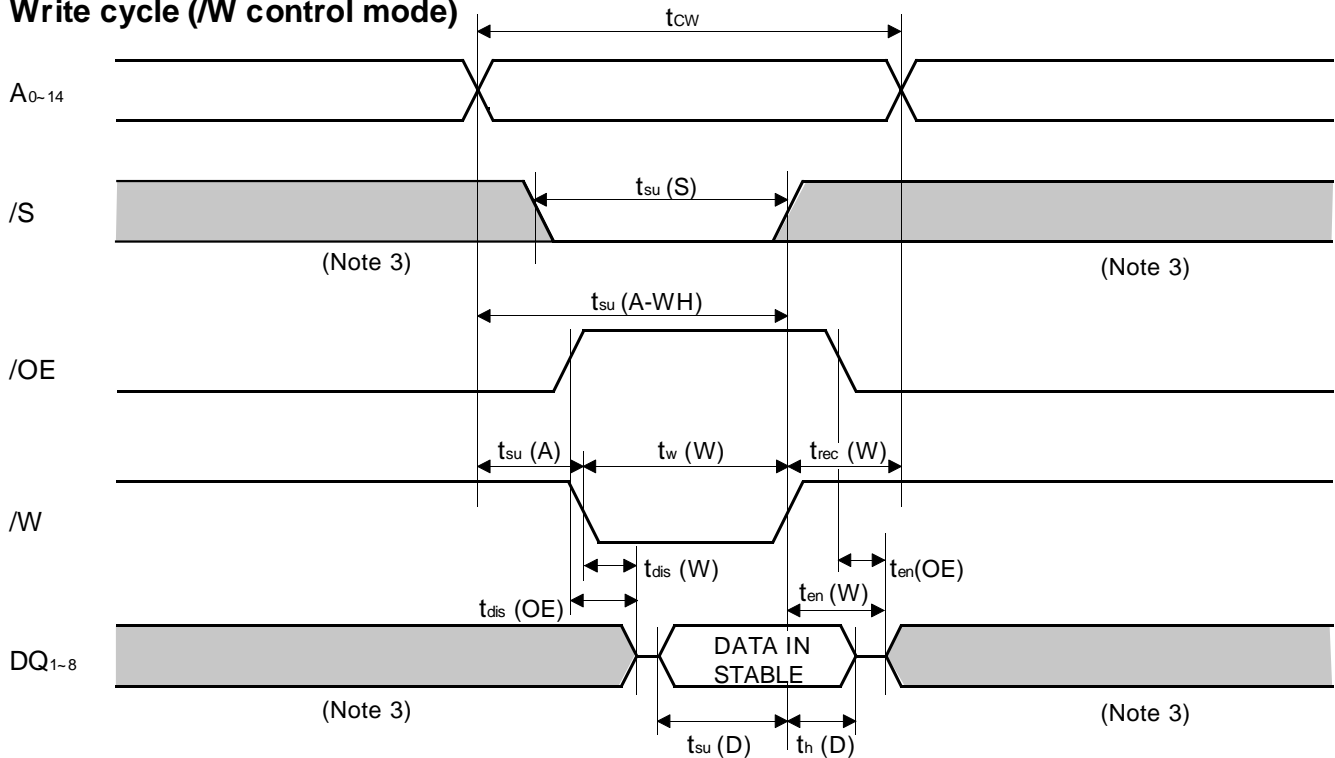
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(3) TIMING DIAGRAMS

Read cycle



Write cycle (/W control mode)

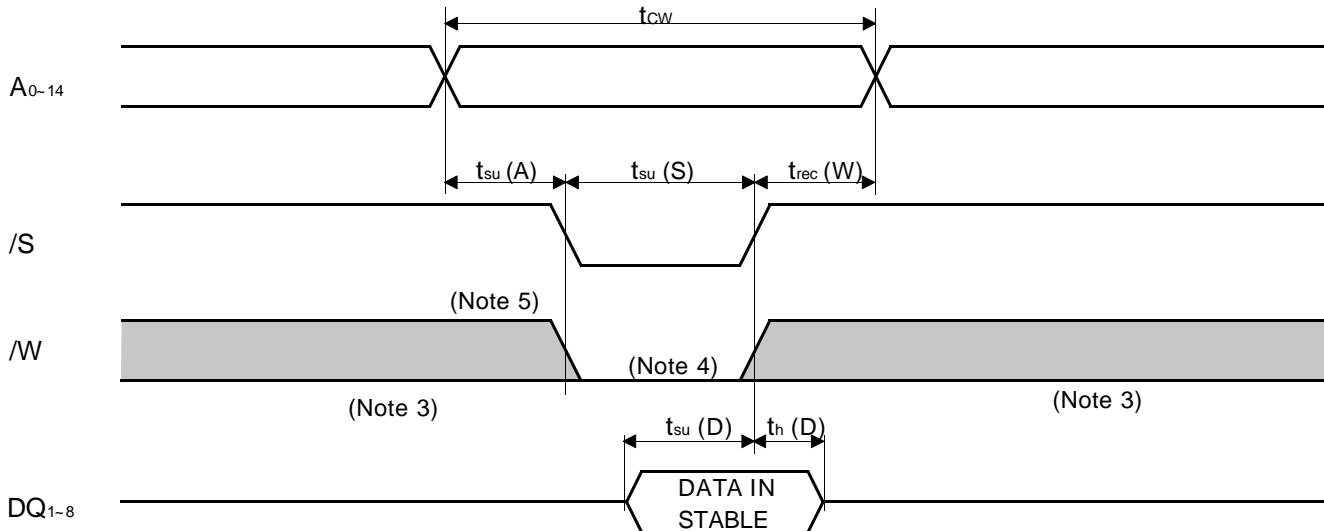


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Write cycle (/S control mode)



Note 3 : Hatching indicates the state is "don't care".

4 : Writing is executed in overlap of /S and /W low.

5 : If /W goes low simultaneously with or prior to /S, the outputs remain in the high impedance state.

6 : Don't apply inverted phase signal externally when DQ pin is output mode.

7 : t_{en} , t_{dis} are periodically sampled and are not 100% tested.

(4) MEASUREMENT CONDITIONS

Input pulse level $V_{IH}=2.4V, V_{IL}=0.6V$

Input rise and fall time 5ns

Reference level $V_{OH}=V_{OL}=1.5V$

Output load Fig.1 $CL=50pF$ (-55LL,-55XL)

$CL=100pF$ (-70LL,-70LLI,-70XL)

$CL=5pF$ (for t_{en}, t_{dis})

Transition is measured $\pm 500mV$ from steady state voltage. (for t_{en}, t_{dis})

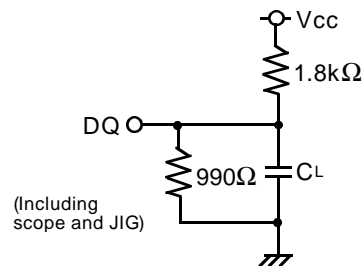


Fig.1 Output load

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, unless otherwise noted)

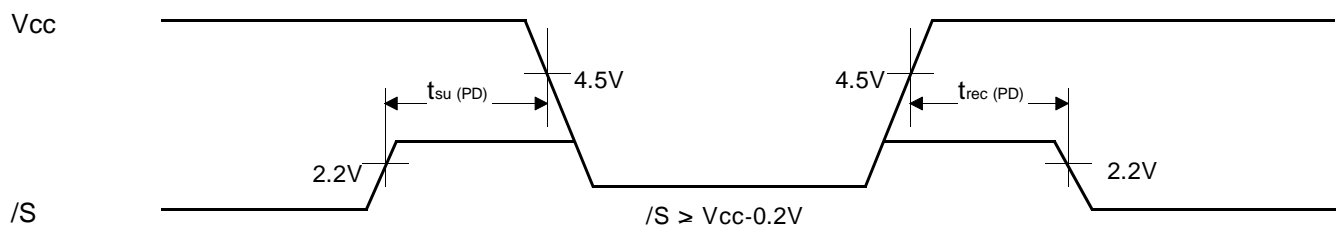
Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
$V_{CC(PD)}$	Power down supply voltage		2			V	
$V_I (/S)$	Chip select input /S	$2.2V \leq V_{CC(PD)}$	2.2			V	
		$2V \leq V_{CC(PD)} \leq 2.2V$		$V_{CC(PD)}$		V	
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3V, /S \geq V_{CC}-0.2V,$ Other inputs=0~ V_{CC}	~25°C	-LL,-LLI		1	μA
				-XL	0.05	0.2	
			~40°C	-LL,-LLI		3	
				-XL		0.6	
			~70°C	-LL,-LLI		10	
-XL		2					
~85°C	-LLI		20				

(2) TIMING REQUIREMENTS ($V_{CC}=5V\pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		tCR			ns

(3) POWER DOWN CHARACTERISTICS

/S control mode



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