



## 2.5V Wide Range Frequency Clock Driver (33MHz - 233MHz)

### Recommended Application:

DDR Memory Modules / Zero Delay Board Fan Out

### Product Description/Features:

- Low skew, low jitter PLL clock driver
  - 1 to 10 differential clock distribution (SSTL2)
  - Feedback pins for input to output synchronization
  - PD# for power management
  - Spread Spectrum-tolerant inputs
  - Auto PD when input signal removed
  - Choice of static phase offset available, for easy board tuning;
- XXX = device pattern number for options listed below.

- ICS95V857 ..... 0ps
- ICS95V857-130 .. +50ps

### Specifications:

- Meets or exceeds JEDEC standard #82-1 for registered DDR clock driver.
- Meets or exceeds proposed DDR1-400 specifications
- Covers all DDR1 speed grades

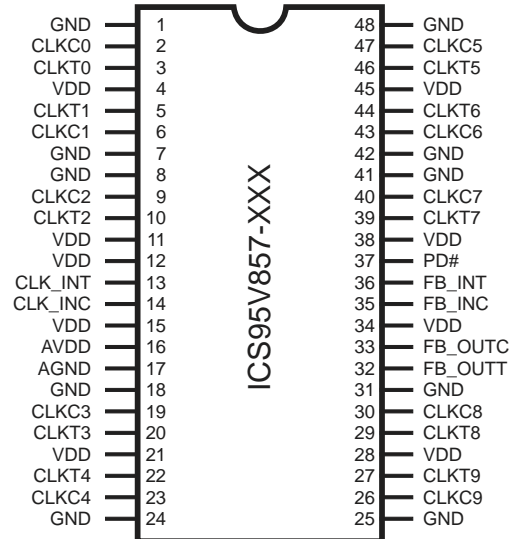
### Switching Characteristics:

- CYCLE - CYCLE jitter (>100MHz): <50ps
- OUTPUT - OUTPUT skew: <30ps
- Output Rise and Fall Time: 650ps - 950ps
- DUTY CYCLE: 49.5% - 50.5%

### Functionality

INPUTS				OUTPUTS				PLL State
AVDD	PD#	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
2.5V (nom)	L	L	H	Z	Z	Z	Z	off
2.5V (nom)	L	H	L	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20MHz <sup>(1)</sup>		Z	Z	Z	Z	off

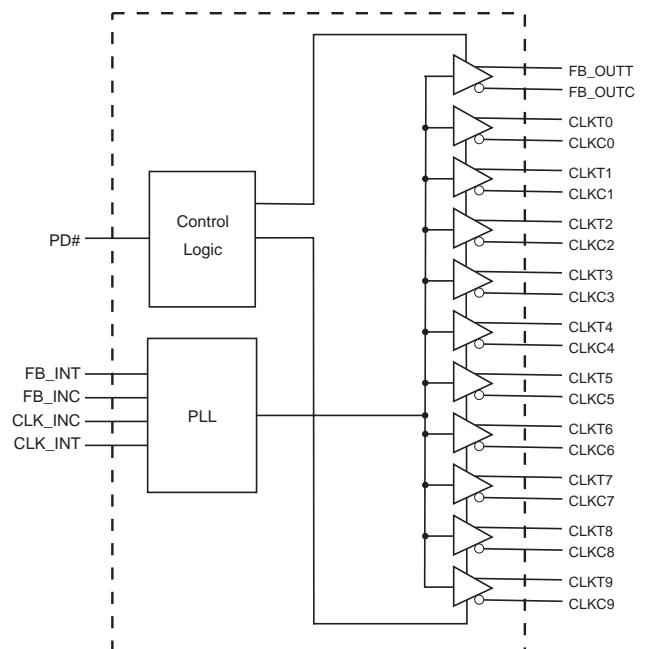
### Pin Configuration



### 48-Pin TSSOP/TVSOP

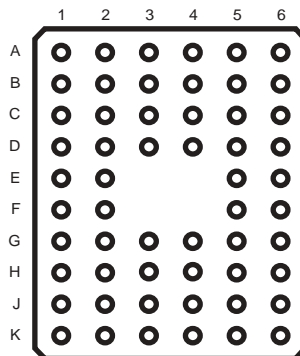
6.10 mm Body, 0.50 mm Pitch = TSSOP  
4.40 mm Body, 0.40 mm Pitch = TVSOP

### Block Diagram



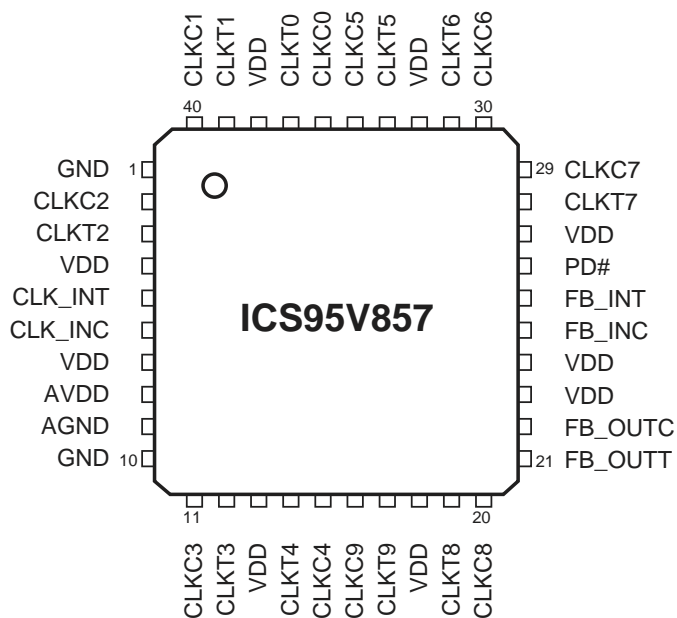


### Pin Configuration



**56-Ball BGA**

	1	2	3	4	5	6
A	CLKT0	CLKC0	GND	GND	CLKC5	CLKT5
B	CLKC1	CLKT1	VDD	VDD	CLKT6	CLKC6
C	GND	GND	NC	NC	GND	GND
D	CLKT2	CLKC2	NC	NC	CLKC7	CLKT7
E	VDD	VDD	NB	NB	VDD	PD#
F	CLK_INT	CLK_INC	NB	NB	FB_INC	FB_INT
G	VDD	AVDD	NC	NC	FB_OUTC	VDD
H	AGND	GND	NC	NC	GND	FB_OUTT
J	CLKC3	CLKT3	VDD	VDD	CLKT8	CLKC8
K	CLKT4	CLKC4	GND	GND	CLKC9	CLKT9



**40-Pin MLF**



### Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
4, 11, 12, 15, 21, 28, 34, 38, 45,	VDD	PWR	Power supply 2.5V
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	PWR	Ground
16	AVDD	PWR	Analog power supply, 2.5V
17	AGND	PWR	Analog ground.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	OUT	"True" Clock of differential pair outputs.
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	OUT	"Complementary" clocks of differential pair outputs.
14	CLK_INC	IN	"Complementary" reference clock input
13	CLK_INT	IN	"True" reference clock input
33	FB_OUTC	OUT	"Complementary" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
32	FB_OUTT	OUT	"True" Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
36	FB_INT	IN	"True" Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
35	FB_INC	IN	"Complementary" Feedback input, provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
37	PD#	IN	Power Down. LVCMOS input

This PLL Clock Buffer is designed for a  $V_{DD}$  of 2.5V, an  $AV_{DD}$  of 2.5V and differential data input and output levels.

The **ICS95V857** is a zero delay buffer that distributes a differential clock input pair (CLK\_INC, CLK\_INT) to ten differential pair of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock output (FB\_OUT, FB\_OUTC). The clock outputs are controlled by the input clocks (CLK\_INC, CLK\_INT), the feedback clocks (FB\_INT, FB\_INC) the 2.5-V LVCMOS input (PD#) and the Analog Power input (AV<sub>DD</sub>). When input (PD#) is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are Tri-Stated. When AV<sub>DD</sub> is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than the operating frequency of the PLL, approximately 20MHz, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the (PD#) input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FB\_INT, FB\_INC) and the input clock pair (CLK\_INC, CLK\_INT).

The PLL in the **ICS95V857** clock driver uses the input clocks (CLK\_INC, CLK\_INT) and the feedback clocks (FB\_INT, FB\_INC) provide high-performance, low-skew, low-jitter output differential clocks (CLKT [0:9], CLKC [0:9]). The **ICS95V857** is also able to track Spread Spectrum Clock (SSC) for reduced EMI.

The **ICS95V857** is characterized for operation from 0°C to 85°C.

# ICS95V857-XXX

## Preliminary Product Preview



### Absolute Maximum Ratings

Supply Voltage (VDD & AVDD)	-0.5V to 4.6V
Logic Inputs	GND -0.5 V to V <sub>DD</sub> + 0.5 V
Ambient Operating Temperature	0°C to +85°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 85°C; Supply Voltage A<sub>VDD</sub>, V<sub>DD</sub> = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I <sub>IH</sub>	V <sub>I</sub> = V <sub>DD</sub> or GND	5			μA
Input Low Current	I <sub>IL</sub>	V <sub>I</sub> = V <sub>DD</sub> or GND			5	μA
Operating Supply Current	I <sub>DD2.5</sub>	C <sub>L</sub> = 0pf @ 200MHz			145	mA
	I <sub>DDPD</sub>	C <sub>L</sub> = 0pf			100	μA
High Impedance Output Current	I <sub>OZ</sub>	V <sub>DD</sub> = 2.7V, V <sub>out</sub> = V <sub>DD</sub> or GND			±10	mA
Input Clamp Voltage	V <sub>IK</sub>	V <sub>DD</sub> = 2.3V I <sub>in</sub> = -18mA			-1.2	V
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 0.1			V
		I <sub>OH</sub> = -12 mA	1.7V			V
Low-level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.1	V
		I <sub>OH</sub> = 12 mA			0.6	V
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	V <sub>I</sub> = GND or V <sub>DD</sub>	2.5		3.5	pF

<sup>1</sup>Guaranteed by design at 233MHz, not 100% tested in production.



### Recommended Operating Condition (see note 1)

$T_A = 0 - 85^\circ\text{C}$ ; Supply Voltage AVDD, VDD = 2.5 V +/- 0.2V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}, A_{VDD}$		2.3		2.7	V
Low level input voltage	$V_{IL}$	CLKT, CLKC, FB_INC			$V_{DD}/2 - 0.18$	V
		PD#	-0.3		0.7	V
High level input voltage	$V_{IH}$	CLKT, CLKC, FB_INC	$V_{DD}/2 + 0.18$			V
		PD#	1.7		$V_{DD} + 0.6$	V
DC input signal voltage (note 2)			-0.3		$V_{DD}$	V
Differential input signal voltage (note 3)	$V_{ID}$	DC - CLKT, FB_INT	0.36		$V_{DD} + 0.6$	V
		AC - CLKT, FB_INT	0.7		$V_{DD} + 0.6$	V
Output differential cross-voltage (note 4)	$V_{OX}$		$V_{DD}/2 - 0.15$		$V_{DD}/2 + 0.15$	V
Input differential cross-voltage (note 4)	$V_{IX}$		$V_{DD}/2 - 0.2$		$V_{DD}/2 + 0.2$	V
High level output current	$I_{OH}$				-4.5	mA
Low level output current	$I_{OL}$				4.5	mA
Input slew rate	$S_R$		1		4	V/ns
Operating free-air temperature	$T_A$		0		85	$^\circ\text{C}$

#### Notes:

- Unused inputs must be held high or low to prevent them from floating.
- DC input signal voltage specifies the allowable DC execution of differential input.
- Differential inputs signal voltages specifies the differential voltage [VTR-VCP] required for switching, where VT is the true input level and VCP is the complementary input level.
- Differential cross-point voltage is expected to track variations of  $V_{CC}$  and is the voltage at which the differential signal must be crossing.

# ICS95V857-XXX

## Preliminary Product Preview



### Timing Requirements

$T_A = 0 - 85^\circ\text{C}$ ; Supply Voltage  $A_{VDD}$ ,  $V_{DD} = 2.5\text{ V} \pm 0.2\text{V}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Max clock frequency	$f_{req_{op}}$	$2.5\text{V} \pm 0.2\text{V} @ 25^\circ\text{C}$	33	233	MHz
Application Frequency Range	$f_{req_{App}}$	$2.5\text{V} \pm 0.2\text{V} @ 25^\circ\text{C}$	95	170	MHz
Input clock duty cycle	$d_{tin}$		40	60	%
CLK stabilization	$T_{STAB}$			100	$\mu\text{s}$

### Switching Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Low-to high level propagation delay time	$t_{PLH}^1$	CLK_IN to any output		5.5		ns
High-to low level propagation delay time	$t_{PLL}^1$	CLK_IN to any output		5.5		ns
Output enable time	$t_{EN}$	PD# to any output		5		ns
Output disable time	$t_{dis}$	PD# to any output		5		ns
Period jitter	$T_{jit(per)}$	100/125/133/167/200MHz	-40		40	ps
Half-period jitter	$t(jit\_hper)$	100/133/167/200MHz	-50		50	ps
Input clock slew rate	$t_{sl(i)}$		1		4	V/ns
Output clock slew rate	$t_{sl(o)}$		1		2.5	V/ns
Cycle to Cycle Jitter <sup>1</sup>	$T_{cyc} - T_{cyc}$	100/125/133/167/200MHz			50	ps
Phase error	$t_{(phase\ error)}^4$		-50	0	50	ps
Output to Output Skew	$T_{skew}$				30	ps
Duty cycle	$D_C^2$	100MHz to 200MHz	49.5		50.5	%
Rise Time, Fall Time	$t_r, t_f$	Load = 120 $\Omega$ /16pF	650	800	950	ps

#### Notes:

- Refers to transition on noninverting output in PLL bypass mode.
- While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle =  $t_{wH}/t_c$ , where the cycle ( $t_c$ ) decreases as the frequency goes up.
- Switching characteristics guaranteed for application frequency range.
- Static phase offset shifted by design.



### Parameter Measurement Information

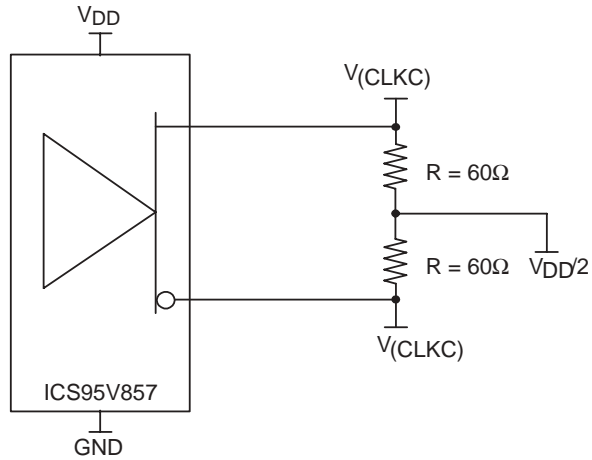
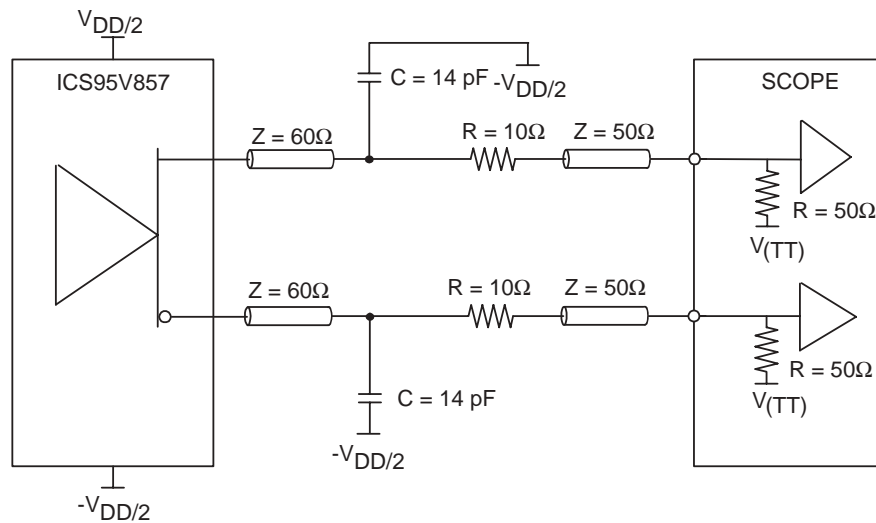


Figure 1. IBIS Model Output Load



NOTE:  $V_{(TT)} = \text{GND}$

Figure 2. Output Load Test Circuit

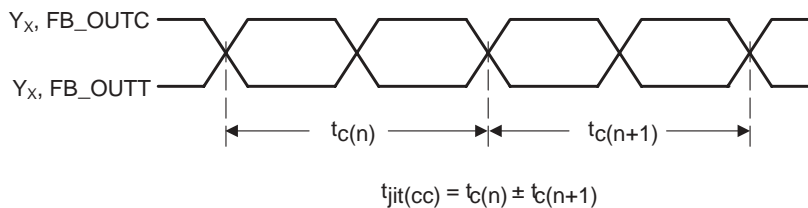
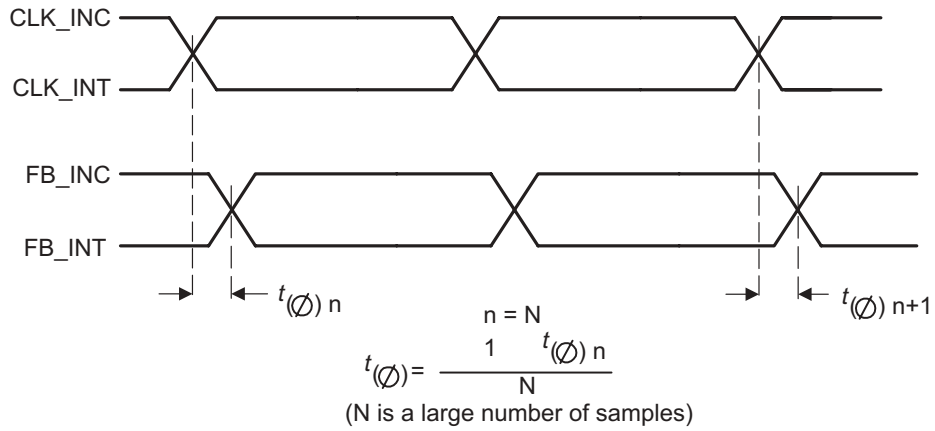


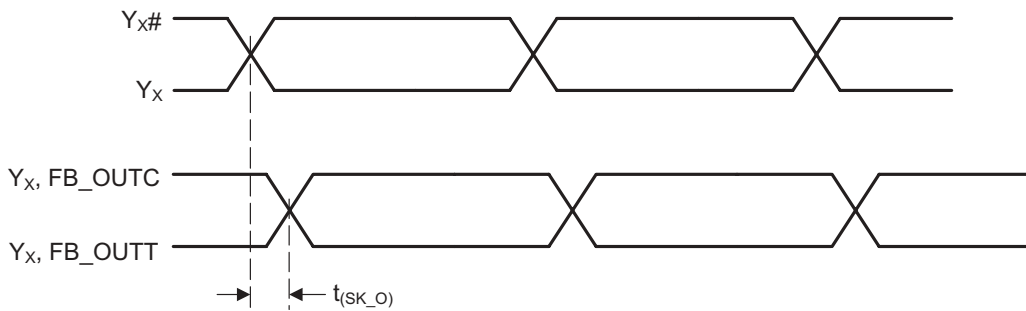
Figure 3. Cycle-to-Cycle Jitter



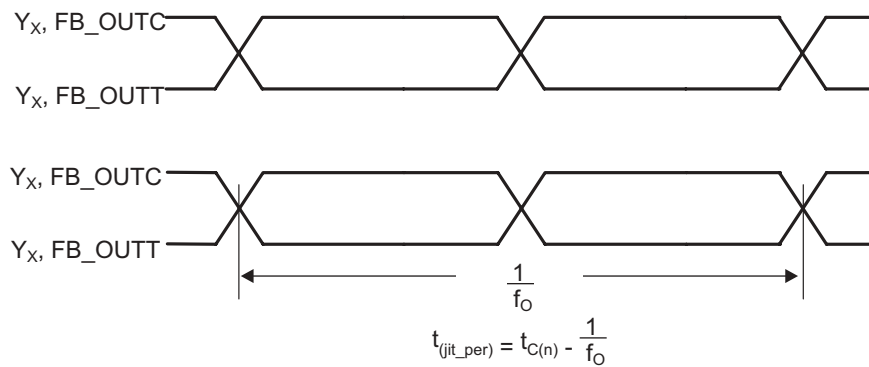
**Parameter Measurement Information**



**Figure 4. Static Phase Offset**



**Figure 5. Output Skew**



**Figure 6. Period Jitter**





Parameter Measurement Information

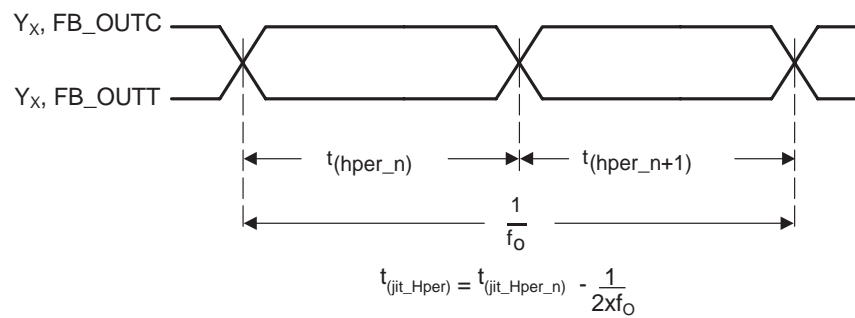


Figure 7. Half-Period Jitter

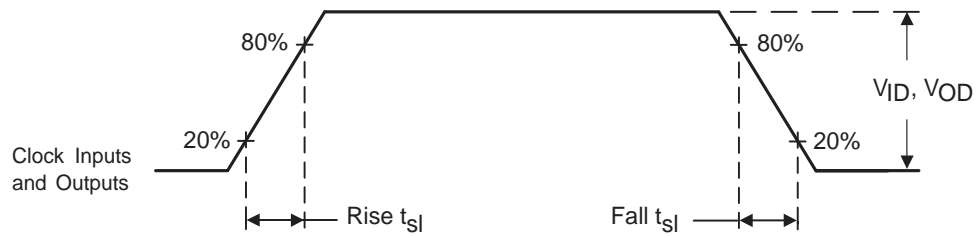
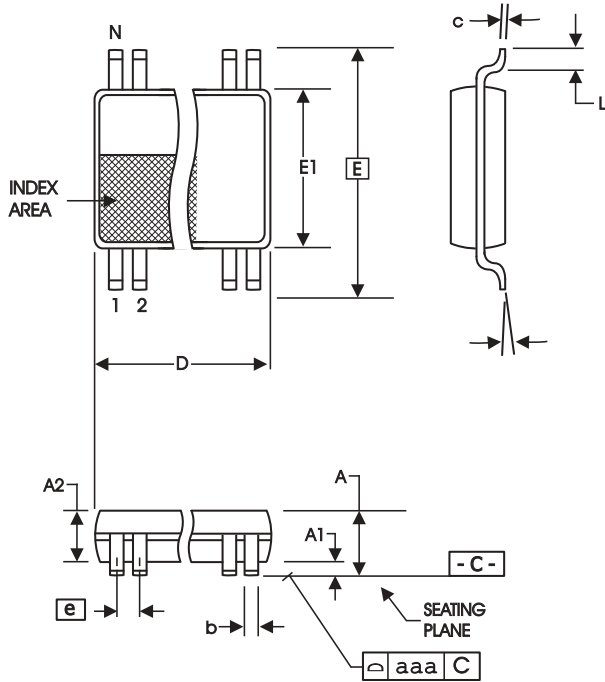


Figure 8. Input and Output Slew Rates

# ICS95V857-XXX

## Preliminary Product Preview



6.10 mm. Body, 0.50 mm. pitch TSSOP  
(240 mil) (0.020 mil)

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

### VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

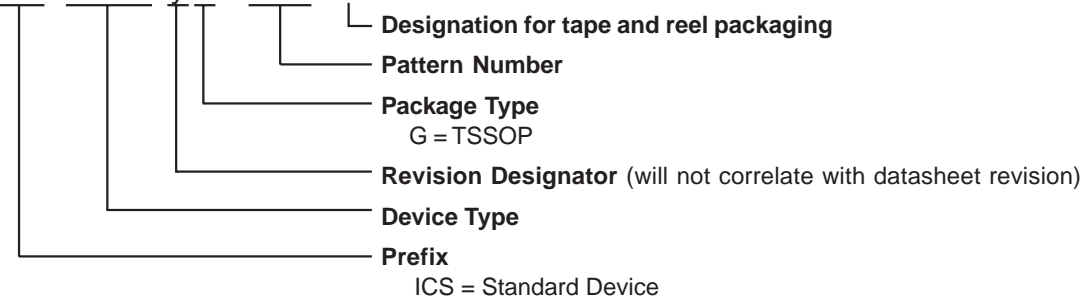
10-0039

## Ordering Information

ICS95V857yGT, ICS95V857yG-130

Example:

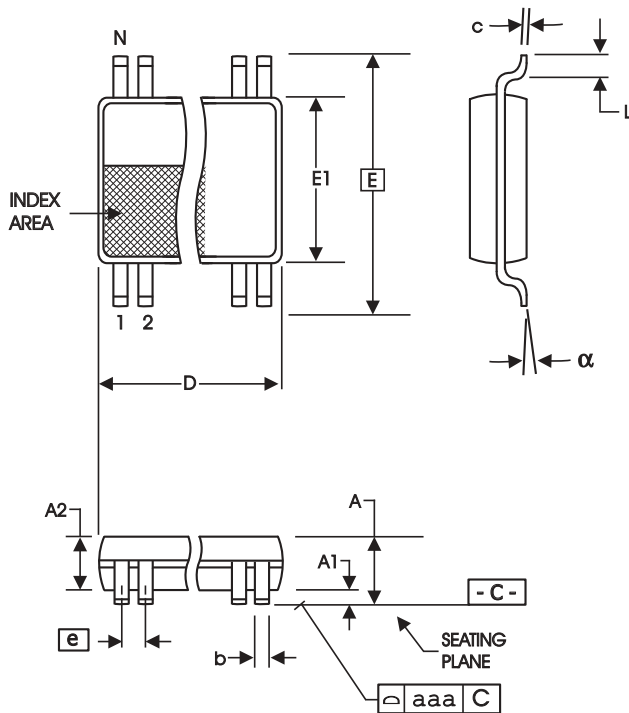
ICS XXXX y G - PPP - T





# ICS95V857-XXX

## Preliminary Product Preview



SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.13	0.23	.005	.009
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.40 BASIC		0.016 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.08	--	.003

### VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153  
10-0037

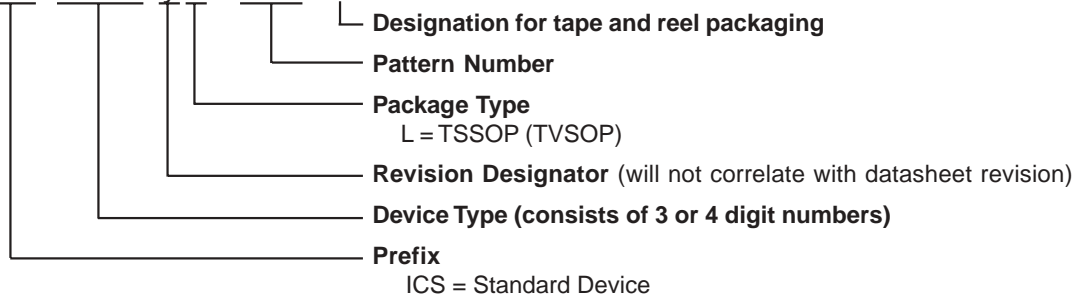
**4.40 mm. Body, 0.40 mm. pitch TSSOP**  
(173 mil)      (16 mil)

## Ordering Information

**ICS95V857yL-130**

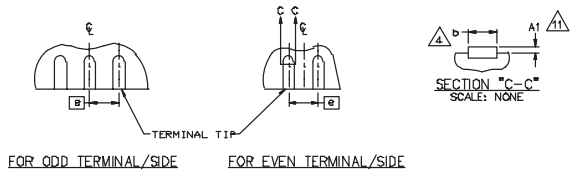
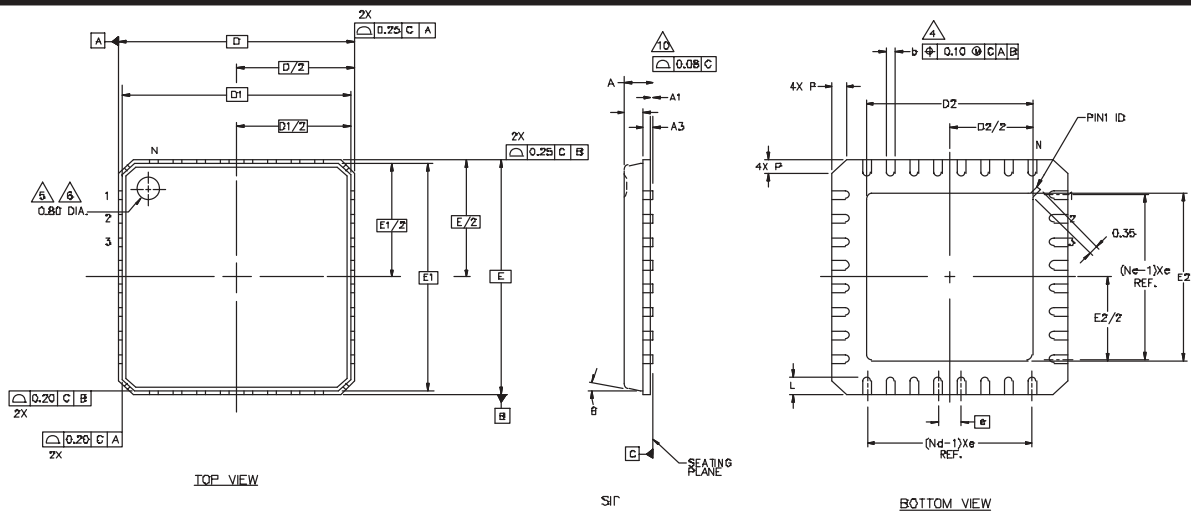
Example:

**ICS XXXX y L - PPP - T**



# ICS95V857-XXX

## Preliminary Product Preview



### 40-Pin MLF

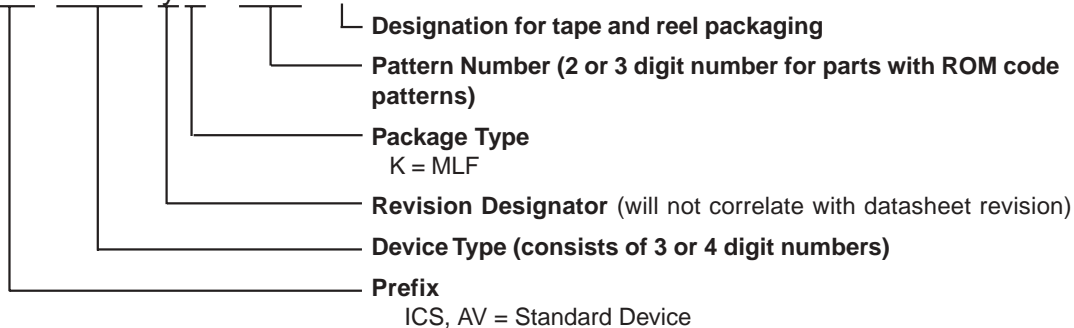
Symbol	Common Dimensions		
A	-	0.85	0.90
A1	0.00	0.01	0.05
A2	-	0.65	0.80
A3	0.20 REF		
D	6.00 BSC		
D1	5.75 BSC		
E	6.00 BSC		
E1	5.75 BSC		
Q			12
P	0.24	0.42	0.60
R	0.13	0.17	0.23
<b>Pitch Variation D</b>			
e	0.50 BSC		
N	40		
Nd	10		
Ne	10		
L	0.30	0.40	0.50
b	0.18	0.23	0.30
Q	0.00	0.20	0.45
D2	2.75	2.90	3.05
E2	2.75	2.90	3.05

## Ordering Information

### ICS95V857yKT

Example:

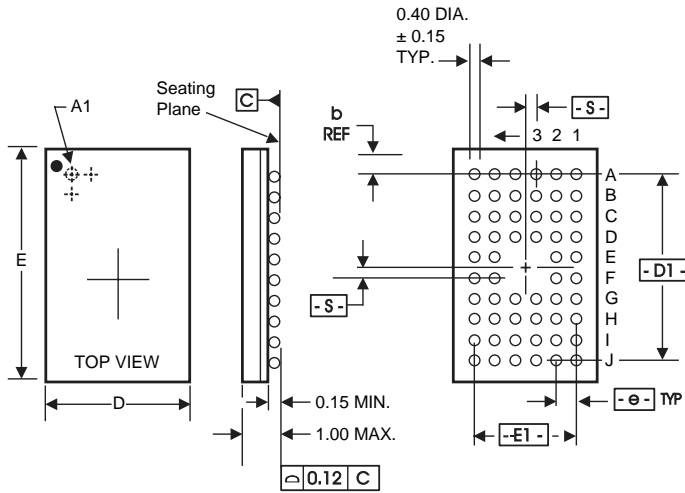
**ICS XXXX y K - PPP - T**





# ICS95V857-XXX

## Preliminary Product Preview



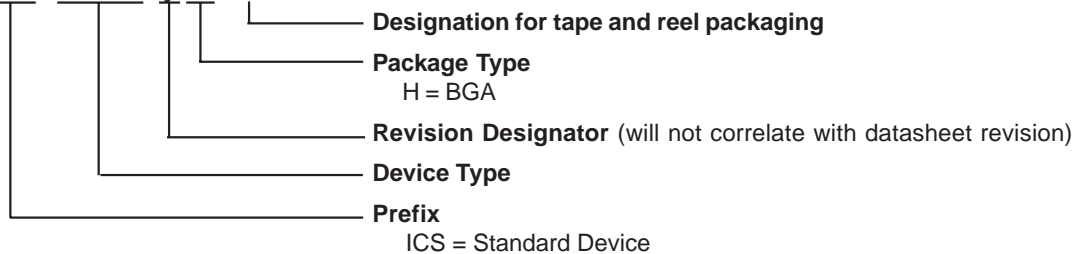
SYMBOL	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.15	0.18	0.21
A2	0.71	0.75	0.79
D	4.40	4.50	4.60
E	6.90	7.00	7.10
I	0.625 REF.		
J	0.575 REF.		
M	6X10		
aaa			0.10
bbb			0.10
ccc			0.10
b	0.35	0.40	0.45
e	0.65 TYP.		

## Ordering Information

ICS95V857yHT

Example:

ICS XXXX y H - T





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## 95V857C (DDR2 PLL)

Description

Market Group

DIMM

Additional Info



### Related Orderable Parts

Attributes	95V857CG	95V857CG8	95V857CGLF	95V857CGLF8	95V857CK	95V857CK8
Package	TSSOP 48 (PA48)	TSSOP 48 (PA48)	TSSOP 48 (PAG48)	TSSOP 48 (PAG48)	VFQFPN 40 (NL40)	VFQFPN 40 (NL40)
Speed	NA	NA	NA	NA	NA	NA
Temperature	C	C	C	C	C	C
Voltage	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V	1.8 V
Status	Active	Obsolete	Active	Obsolete	Active	Obsolete
Sample	No	No	No	No	No	No
Minimum Order Quantity	304	1000	304	1000	490	1000
Factory Order Increment	38	1000	38	1000	490	1000

1 2

1 2

### Related Documents

Type	Title	Size	Revision Date
Datasheet	95V857C Datasheet	136 KB	09/05/2006

