National Semiconductor

microCMOS

MM54HCT160/MM74HCT160
Synchronous Decade Counter with Asynchronous Clear
MM54HCT161/MM74HCT161
Synchronous Binary Counter with Asynchronous Clear
MM54HCT162/MM74HCT162
Synchronous Decade Counter with Synchronous Clear
MM54HCT163/MM74HCT163
Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HCT160/74HCT160, MM54HCT161/74HCT161, MM54HCT162/74HCT162, MM54HCT163/74HCT163 synchronous presettable counters utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HCT160 and the 'HCT162 are 4-bit decade counters, and the 'HCT161 and the 'HCT163 are 4-bit binary counters. All flip-flops are clocked simultaneously on the low to high transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HCT162/MM74HCT162 and MM54HCT163/MM74HCT163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HCT160/MM74HCT160 and MM54HCT161/MM74HCT161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

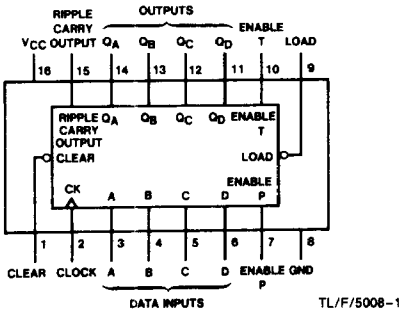
These circuits are TTL input and output compatible and are plug in replaceable for 'LS16X Series counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40 MHz
- Typical propagation delay: clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V
- TTL Input Compatible Inputs

Connection Diagram



TL/F/5008–1

54HCT160 (J) 74HCT160 (J,N)
54HCT161 (J) 74HCT161 (J,N)
54HCT162 (J) 74HCT162 (J,N)
54HCT163 (J) 74HCT163 (J,N)

Truth Tables

'HCT160/HCT161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HCT162/HCT163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	300	500			μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		43	30	MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		24	36	ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		20	30	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		29	34	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		21	28	ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		18	32	ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		15	26	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		29	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	ns
t_H	Minimum Hold Time, Data from Clock			5	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C		Units
			Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		40	27	21	18	MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		22	43	54	64	ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		18	35	44	52	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		21	41	52	61	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		17	34	43	51	ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		20	39	49	58	ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		16	32	40	48	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		32	44	55	66	ns
t_{REM}	Minimum Removal Time Clear to Clock			25	32	37	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	38	45	ns
t_H	Minimum Hold Time Data from Clock			10	13	15	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		8	15	19	22	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)	90				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.