CYPRESS

PRELIMINARY

CY2277A

Pentium™ Clock Synthesizer/Driver for Intel 82430TX Chipset

Features

- Mixed 2.5V and 3.3V operation
- Complete clock solution to meet requirements of Pentium™ motherboards
  - Four CPU clocks at 2.5V or 3.3V
  - Eight 3.3V SDRAM clocks
  - Seven 3.3V synchronous PCI clocks, one free running
  - Two 3.3V USB/IO clocks at 48 or 24 MHz, selectable by serial interface
  - One 2.5V IOAPIC clock at 14.318 MHz
  - Two 3.3V Ref. clocks at 14.318 MHz
- 1 ns–4 ns CPU-PCI delay (-1, -2, -3), factory-EPROM programmable, meets Intel and other core-logic chipset requirements. 500 ps CPU-PCI delay on -4.
- Factory-EPROM programmable output drive and slew rate for optimal EMI control. Improved output drivers are designed for low EMI.
- Factory-EPROM programmable CPU, PCI, and USB/IO clock frequencies for custom configurations
- Separate power management Mode Enable pin, enables CPU_STOP and PCI_STOP inputs
- Power management control input pins
- I²C™ serial configuration interface

- Available in space-saving 48-pin SSOP and TSSOP packages (see Ordering Information)

Functional Description

The CY2277A is a Clock Synthesizer/Driver for a Pentium-based PC.

The CY2277A outputs four CPU clocks at 2.5V or 3.3V and up to eight 3.3V SDRAM clocks. There are seven PCI clocks, running at one half the CPU clock frequency, one of which is free-running. Additionally, the part outputs two 3.3V USB/IO clocks at 48 MHz or 24 MHz, one 2.5V IOAPIC clock at 14.318 MHz, and two 3.3V reference clocks at 14.318 MHz. All output clocks meet Intel's drive strength, rise/fall time, jitter, accuracy, and skew requirements. The CPU, PCI, USB, and IO clock frequencies are factory-EPROM programmable for easy customization with fast turnaround times.

Dedicated power management pins, as well as a serial I²C programming interface enable the CY2277A to be optimized for mobile systems.

The CY2277A clock outputs are designed for low EMI emissions. Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2277A to have lower EMI than clock devices from other manufacturers. Additionally, factory-EPROM programmable output drive and slew-rate control enable optimal configurations for EMI control.

Logic Block Diagram

Pin Configuration

SSOP
Top View
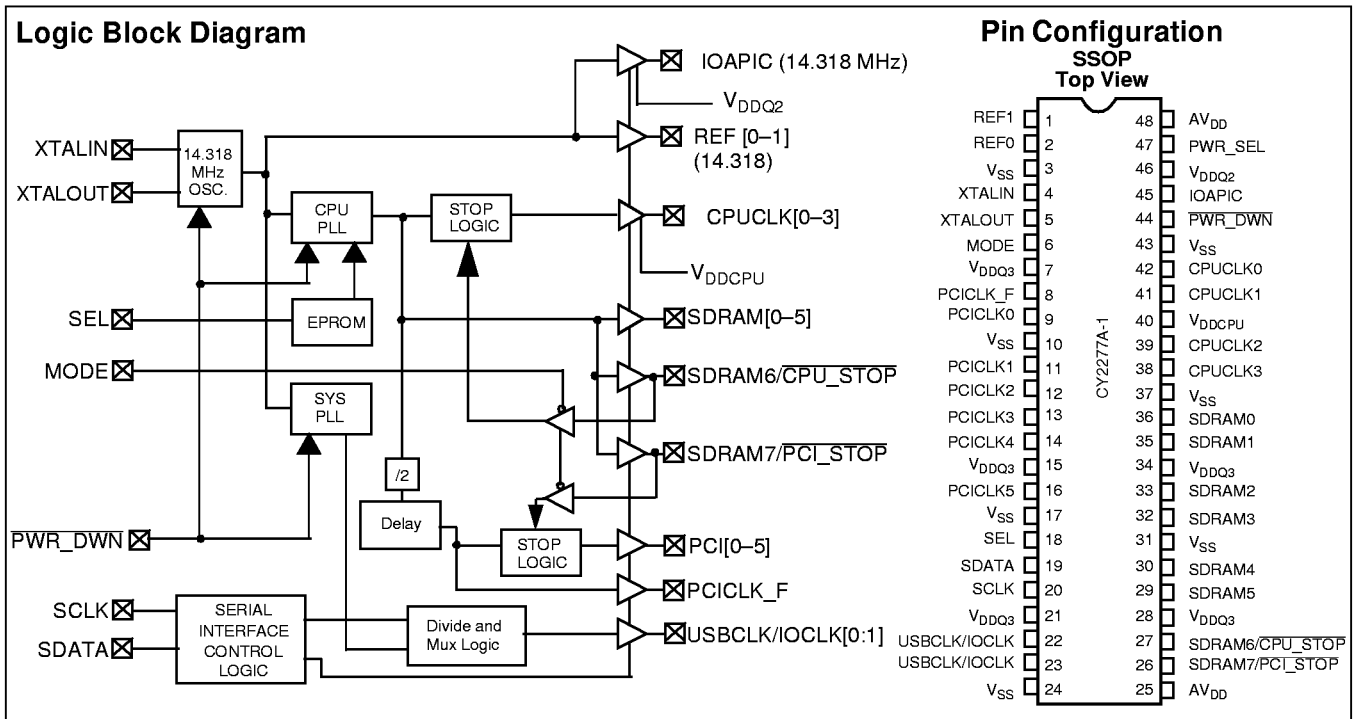
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Pin Summary

Name	Pins	Description
V_{DDQ3}	7, 15, 21, 28, 34	3.3V Digital voltage supply
V_{DDQ2}	46	IOAPIC Digital voltage supply, 2.5V or 3.3V
V_{DDCPU}	40	CPU Digital voltage supply, 2.5V or 3.3V
AV_{DD}	25, 48	3.3V Analog voltage supply
V_{SS}	3, 10, 17, 24, 31, 37, 43	Ground
XTALIN[1]	4	Reference crystal input
XTALOUT[1]	5	Reference crystal feedback
MODE	6	Mode select input, enables power management features
SEL	18	Select input to enable 66.66 MHz or 60 MHz CPU clock (See table below.)
SDATA	19	I^2C serial data input for serial configuration port
SCLK	20	I^2C serial clock input for serial configuration port
$\overline{PWR\_DWN}$	44	Active low control input to put osc., PLLs, and outputs in power down state
PWR_SEL	47	Power select input, indicates whether V_{DDCPU} is at 2.5V or 3.3V HIGH = 3.3V, LOW=2.5V (internal pull-up to V_{DD})
SDRAM7/$\overline{PCI\_STOP}$	26	SDRAM clock output. Also, active low control input to stop PCI clocks, enabled when MODE is low
SDRAM6/$\overline{CPU\_STOP}$	27	SDRAM clock output. Also, active low control input to stop CPU clocks, enabled when MODE is low
SDRAM[0:5]	36, 35, 33, 32, 30, 29	SDRAM clock outputs, have same frequency as CPU clocks
CPUCLK[0:3]	42, 41, 39, 38	CPU clock outputs
PCICLK[0:5]	9, 11, 12, 13, 14, 16	PCI clock outputs
PCICLK_F	8	PCI clock output, free-running
IOAPIC	45	IOAPIC clock output
REF[0:1]	1,2	Reference clock outputs, 14.318 MHz. REF0 drives 45 pF load
USBCLK/IOCLK	22,23	USB or IO clock outputs, frequency selected by serial word
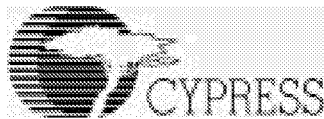
Function Table (-1, -4)

SEL	XTALIN	CPUCLK[0:3] SDRAM[0:7]	PCICLK[0:5] PCICLK_F	REF[0:1] IOAPIC	USBCLK / IOCLK[2]
0	14.318 MHz	60.0 MHz	30.0 MHz	14.318 MHz	48.0 MHz / 24.0 MHz
1	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz	48.0 MHz / 24.0 MHz

Function Table (-3)

SEL	XTALIN	CPUCLK[0:3] SDRAM[0:7]	PCICLK[0:5] PCICLK_F	REF[0:1] IOAPIC	USBCLK / IOCLK[2]
0	14.318 MHz	33.33 MHz	16.67 MHz	14.318 MHz	48.0 MHz / 24.0 MHz
1	14.318 MHz	66.67 MHz	33.33 MHz	14.318 MHz	48.0 MHz / 24.0 MHz

Function Table (-2)[3, 4]

Pin 18	I^{2}C Control - Byte 0[6]			Outputs (MHz)			
SEL[5]	Bit 6	Bit 5	Bit 4	CPU Freq (Target)	PCI Freq (CPU/2)	CPU Freq (Actual)	PPM
0	0	0	0	66.8	33.4	66.818	272
0	0	0	1	75.0	37.5	75.000	0
0	0	1	0	60.0	30.0	60.000	0
0	0	1	1	55.0	27.5	55.012	217
0	1	0	0	68.4	34.2	68.409	133
0	1	0	1	50.0	25.0	49.947	1057
0	1	1	0	83.3	41.65	83.306	69
0	1	1	1	33.3	16.67	33.298	1107
1	0	0	0	68.4	34.2	68.409	133
1	0	0	1	50.0	25.0	49.947	1057
1	0	1	0	83.3	41.65	83.306	69
1	0	1	1	33.3	16.67	33.298	1107
1	1	0	0	66.8	33.4	66.818	272
1	1	0	1	75.0	37.5	75.000	0
1	1	1	0	60.0	30.0	60.000	0
1	1	1	1	55.0	27.5	55.012	217

Actual Clock Frequency Values (-1, -3, -4)

Clock Output	Target Frequency (MHz)	Actual Frequency (MHz)	PPM
CPUCLK, SDRAM	66.67	66.654	−195
CPUCLK, SDRAM	60.0	60.0	0
USBCLK[7]	48.0	48.008	167
IOCLK	24.0	24.004	167

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V.

Notes:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.
2. On power-up, the default frequency on these outputs is 48 MHz.
3. All AC specs for duty cycle, skew, jitter, and rise/fall time remain the same.
4. The above frequencies support Intel Pentium and Pentium II, AMD K5™ and K6™, and Cyrix M1™ and M2™ processors.

5. SEL = 0 OR SEL = 1 gives all the same CPU frequencies on the outputs. In this case, the CPU and PCI frequencies are I^{2}C controllable. Therefore, the user can have jumperless frequency changes.
6. The above I^{2}C bits will NOT affect the other clocks in the system.
7. Meets Intel USB clock requirements

Power Management Logic

CPU_STOP	PCI_STOP	PWR_DWN	CPUCLK	PCICLK	PCICLK_F	Other Clocks	Osc.	PLLs
X	X	0	Low	Low	Stopped	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running	Running
0	1	1	Low	33/30 MHz	Running	Running	Running	Running
1	0	1	66/60 MHz	Low	Running	Running	Running	Running
1	1	1	66/60 MHz	33/30 MHz	Running	Running	Running	Running

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  .

  .

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0".
- I^2C Address for the CY2277A is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

Byte 0: Functional and Frequency Select Clock Register (1 = Enable, 0 = Disable)

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	--	(Reserved) drive to '0' on -1, -3, -4
Bit 6	--	Freq. Sel. Bit on -2
Bit 5	--	(Reserved) drive to '0' on -1, -3, -4
Bit 5	--	Freq. Sel. Bit on -2
Bit 4	--	(Reserved) drive to '0' on -1, -3, -4
Bit 4	--	Freq. Sel. Bit on -2
Bit 3	23	48/24 MHz (Frequency Select) 1 = 48 MHz (default), 0 = 24 MHz
Bit 2	22	48/24 MHz (Frequency Select) 1 = 48 MHz (default), 0 = 24 MHz
Bit 1 Bit 0	--	Bit 1 — Bit 0 1 — 1 - Three-State (see table below) 1 — 0 - N/A 0 — 1 - Test Mode (see table below) 0 — 0 - Normal Operation

Select Functions

Functional Description	Outputs						
	CPU	PCI, PCI_F	SDRAM	Ref	IOAPIC	IOCLK	USBCLK
Three-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2[8]	TCLK/4	TCLK/2	TCLK	TCLK	TCLK/4	TCLK/2

Note:
8. TCLK supplied on the XTALIN, PIN 4.

**Byte 1: CPU, 24/48 MHz Active/Inactive
Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	23	48/24 MHz (Active/Inactive)
Bit 6	22	48/24 MHz (Active/Inactive)
Bit 5	--	(Reserved) drive to '0'
Bit 4	N/A	Not Used, drive 0
Bit 3	38	CPUCLK3 (Active/Inactive)
Bit 2	39	CPUCLK2 (Active/Inactive)
Bit 1	41	CPUCLK1 (Active/Inactive)
Bit 0	42	CPUCLK0 (Active/Inactive)

**Byte 2: PCI Active/Inactive
Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	8	PCICLK_F (Active/Inactive)
Bit 5	16	PCICLK5 (Active/Inactive)
Bit 4	14	PCICLK4 (Active/Inactive)
Bit 3	13	PCICLK3 (Active/Inactive)
Bit 2	12	PCICLK2 (Active/Inactive)
Bit 1	11	PCICLK1 (Active/Inactive)
Bit 0	9	PCICLK0 (Active/Inactive)

**Byte 3: SDRAM Active/Inactive
Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	26	SDRAM7 (Active/Inactive)
Bit 6	27	SDRAM6 (Active/Inactive)
Bit 5	29	SDRAM5 (Active/Inactive)
Bit 4	30	SDRAM4 (Active/Inactive)
Bit 3	32	SDRAM3 (Active/Inactive)
Bit 2	33	SDRAM2 (Active/Inactive)
Bit 1	35	SDRAM1 (Active/Inactive)
Bit 0	36	SDRAM0 (Active/Inactive)

**Byte 4: SDRAM Active/Inactive
Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	N/A	Not used, drive to '0'
Bit 6	N/A	Not used, drive to '0'
Bit 5	N/A	Not used, drive to '0'
Bit 4	N/A	Not used, drive to '0'
Bit 3	N/A	Not used, drive to '0'
Bit 2	N/A	Not used, drive to '0'
Bit 1	N/A	Not used, drive to '0'
Bit 0	N/A	Not used, drive to '0'

**Byte 5: Peripheral Active/Inactive
Register(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description
Bit 7	--	(Reserved) drive to '0'
Bit 6	--	(Reserved) drive to '0'
Bit 5	--	(Reserved) drive to '0'
Bit 4	45	IOAPIC (Active/Inactive)
Bit 3	--	(Reserved) drive to '0'
Bit 2	--	(Reserved) drive to '0'
Bit 1	1	REF1 (Active/Inactive)
Bit 0	2	REF0 (Active/Inactive)

Byte 6: Reserved, for future use
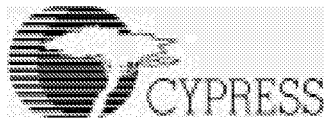
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ....–0.5 to +7.0V

Input Voltage ....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing) ... –65°C to +150°C

Max. Soldering Temperature (10 sec) .... +260°C

Junction Temperature .... +150°C

Package Power Dissipation.. 1W

Static Discharge Voltage ....>2000V
(per MIL-STD-883, Method 3015)

Operating Conditions[9]

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DDQ3}	Analog and Digital Supply Voltage	3.135	3.465	V
V_{DDCPU}	CPU Supply Voltage	2.375 3.135	2.9 3.465	V
V_{DDQ2}	IOAPIC Supply Voltage	2.375	2.9	V
T_A	Operating Temperature, Ambient	0	70	°C

C_L	Max. Capacitive Load on
	    CPUCLK, USBCLK/IOCLK, REF1, IOAPIC
	    PCICLK, SDRAM
	    REF0
		
		10
		30, 20
		20
			
			20
			30
			45
				pF

$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DDQ2} = V_{DDCPU} = 2.375V	I_{OH} = 18 mA	CPUCLK	2.0		V
			I_{OH} = 18 mA	IOAPIC			
V_{OL}	Low-level Output Voltage	V_{DDQ2} = V_{DDCPU} = 2.375V	I_{OL} = 29 mA	CPUCLK		0.4	V
			I_{OL} = 29 mA	IOAPIC			
V_{OH}	High-level Output Voltage	V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V	I_{OH} = 18 mA	CPUCLK	2.4		V
			I_{OH} = 36 mA	SDRAM			
			I_{OH} = 32 mA	PCICLK			
			I_{OH} = 26 mA	USBCLK			
			I_{OH} = 26 mA	IOCLK			
			I_{OH} = 36 mA	REF0			
			I_{OH} = 26 mA	REF1			
V_{OL}	Low-level Output Voltage	V_{DDQ3}, AV_{DD}, V_{DDCPU} = 3.135V	I_{OL} = 29 mA	CPUCLK		0.4V	V
			I_{OL} = 29 mA	SDRAM			
			I_{OL} = 26 mA	PCICLK			
			I_{OL} = 21 mA	USBCLK			
			I_{OL} = 21 mA	IOCLK			
			I_{OL} = 29 mA	REF0			
			I_{OL} = 21 mA	REF1			
I_{IH}	Input High Current	V_{IH} = V_{DD}			–5	+5	µA
I_{IL}	Input Low Current	V_{IL} = 0V				5	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current[10]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Loaded Outputs, CPU clocks = 66.67 MHz				250	mA
I_{DD}	Power Supply Current[10]	V_{DD} = 3.465V, V_{IN} = 0 or V_{DD}, Unloaded Outputs				120	mA
I_{DDS}	Power-down Current	Current draw in power-down state				50	µA

Notes:
9. Electrical parameters are guaranteed with these operating conditions.
10. Power supply current will vary with number of outputs which are running. Therefore, power supply current can be calculated with the following formula: TBD
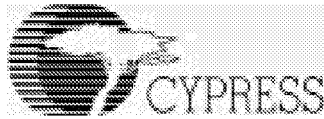
Switching Characteristics[11]

Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle[12]	$t_1 = t_{1A} \div t_{1B}$	45	50	55	%
t_{1C}	CPUCLK	CPU Clock HIGH Time	Above 2.0V, 66.6 MHz, V_{DDCPU} = 2.5V Above 2.4V, 66.6 MHz, V_{DDCPU} = 3.3V Above 2.0V, 60.0 MHz, V_{DDCPU} = 2.5V Above 2.4V, 60.0 MHz, V_{DDCPU} = 3.3V	5.2 TBD 6.0 TBD			ns
t_{1C}	PCICLK	PCI Clock HIGH Time	Above 2.4V, 33.3 MHz Above 2.4V, 30.0 MHz	12.0 13.3			ns
t_{1D}	CPUCLK	CPU Clock LOW Time	Below 0.4V, 66.6 MHz, V_{DDCPU} = 2.5V Below 0.4V, 66.6 MHz, V_{DDCPU} = 3.3V Below 0.4V, 60.0 MHz, V_{DDCPU} = 2.5V Below 0.4V, 60.0 MHz, V_{DDCPU} = 3.3V	5.0 5.0 5.8 5.8			ns
t_{1D}	PCICLK	PCI Clock LOW Time	Below 0.4V, 33.3 MHz Below 0.4V, 30.0 MHz	12.0 13.3			ns
t_2	CPUCLK, IOAPIC	CPU and IOAPIC Clock Rising and Falling Edge Rate	Between 0.4V and 2.0V, V_{DDCPU} = 2.5V Between 0.4V and 2.4V, V_{DDCPU} = 3.3V	1.0		4.0	V/ns
t_2	PCICLK, USBCLK, IOCLK, REF0	PCI, USB, I/O, REF0 Clock Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.0		4.0	V/ns
t_2	SDRAM	SDRAM Rising and Falling Edge Rate	Between 0.4V and 2.4V	1.5		4.0	V/ns
t_2	REF1	REF1 Rising and Falling Edge Rate	Between 0.4V and 2.4V	0.5		2.0	V/ns
t_3	CPUCLK	CPU Clock Rise Time	Between 0.4V and 2.0V, V_{DDCPU} = 2.5V Between 0.4V and 2.4V, V_{DDCPU} = 3.3V	0.4 0.5		1.6 2.0	ns
t_3	USBCLK, IOCLK	USB Clock and I/O Clock Rise Time	Between 0.4V and 2.4V			2.0	ns
t_4	CPUCLK	CPU Clock Fall Time	Between 2.0V and 0.4V, V_{DDCPU} = 2.5V Between 2.4V and 0.4V, V_{DDCPU} = 3.3V	0.4 0.5		1.6 2.0	ns
t_4	USBCLK, IOCLK	USB Clock and I/O Clock Fall Time	Between 2.4V and 0.4V			2.0	ns
t_5	CPUCLK	CPU-CPU Clock Skew	Measured at 1.25V, V_{DDCPU} = 2.5V Measured at 1.5V, V_{DDCPU} = 3.3V		100	250	ps
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew (-1, -2, -3)	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks	1.0	2.0	4.0	ns
t_6	CPUCLK, PCICLK	CPU-PCI Clock Skew (-4)	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			500	ps
t_7	CPUCLK, SDRAM	CPU-SDRAM Clock Skew	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			500	ps
t_8	CPUCLK, SDRAM	Cycle-Cycle Clock Jitter	Measured at 1.25V for 2.5V clocks, and at 1.5V for 3.3V clocks			±250	ps
t_8	USBCLK, IOCLK, PCICLK	Cycle-Cycle Clock Jitter	Measured at 1.5V			±500	ps
t_9	CPUCLK, PCICLK, SDRAM	Power-up Time	CPU, PCI, and SDRAM clock stabilization from power-up			3	ms
t_{10}	CPU, PCI, SDRAM	Frequency Slew Rate	Rate of change of frequency		2		MHz/ms

Notes:
11. All parameters specified with loaded outputs.
12. Duty cycle is measured at 1.5V when V_{DD} = 3.3V. When V_{DDCPU} = 2.5V, CPUCLK duty cycle is measured at 1.25V.

Timing Requirement for the I²C Bus

Parameter	Description	Min.	Max.	Unit
t_{10}	SCLK Clock Frequency	0	100	kHz
t_{11}	Time the bus must be free before a new transmission can start	4.7		μs
t_{12}	Hold time start condition. After this period the first clock pulse is generated.	4		μs
t_{13}	The LOW period of the clock.	4.7		μs
t_{14}	The HIGH period of the clock.	4		μs
t_{15}	Setup time for start condition. (Only relevant for a repeated start condition.)	4.7		μs

t_{16}	Hold time DATA
	    for CBUS compatible masters.
	    for I²C devices
		
		5
		0
				μs

t_{17}	DATA input set-up time	250		ns
t_{18}	Rise time of both SDATA and SCLK inputs		1	μs
t_{19}	Fall time of both SDATA and SCLK inputs		300	ns
t_{20}	Set-up time for stop condition	4.0		μs

Switching Waveforms

Duty Cycle Timing
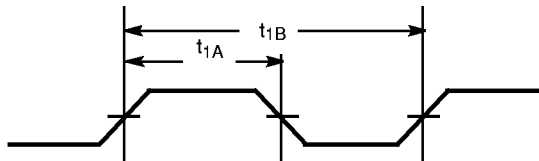
CPUCLK Outputs HIGH/LOW Time
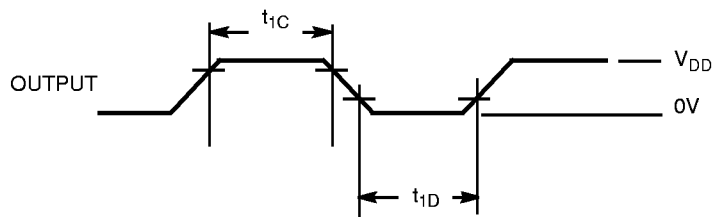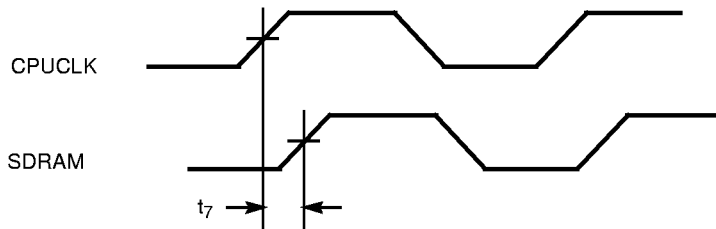

All Outputs Rise/Fall Time
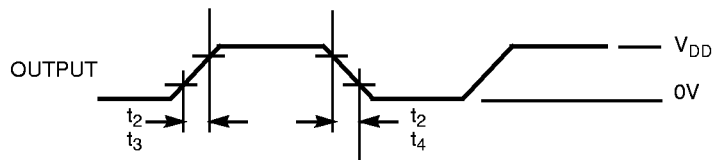
Switching Waveforms (continued)

CPU-CPU Clock Skew

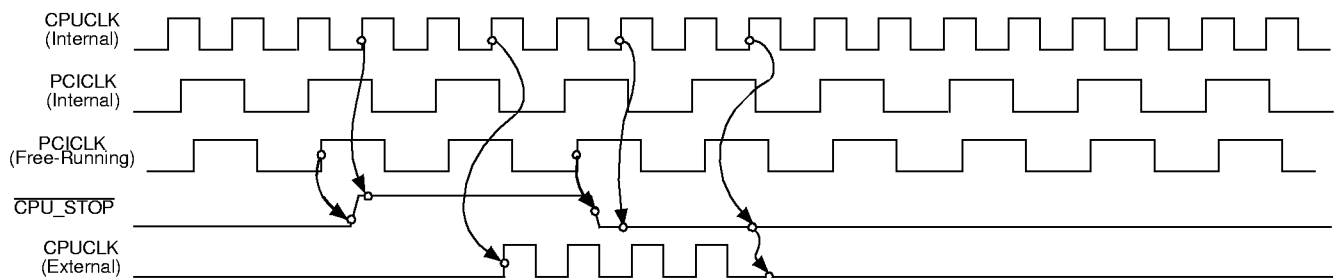CPUCLK

CPUCLK

t_5

CPU-SDRAM Clock Skew

CPUCLK

SDRAM

t_7
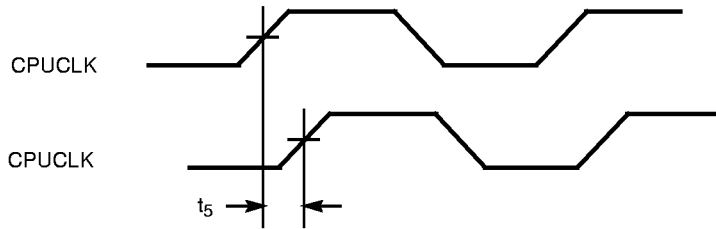
CPU-PCI and CPU/SDRAM Clock Skew

CPUCLK

PCICLK

t_6

$\overline{\text{CPU\_STOP}}$ [13, 14]

CPUCLK
(Internal)

PCICLK
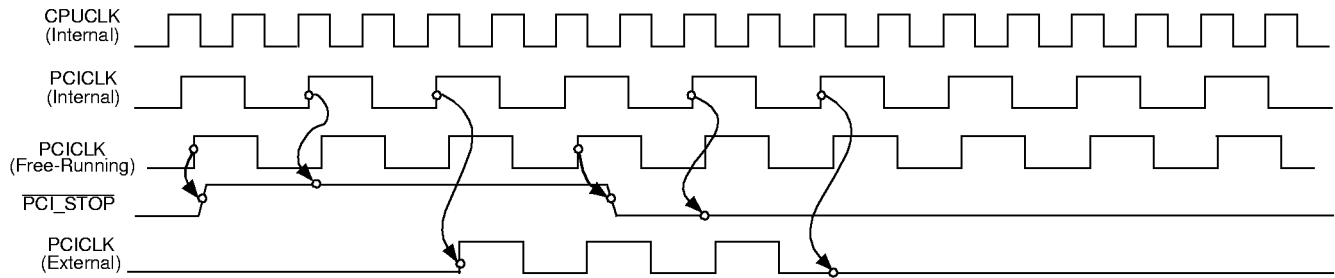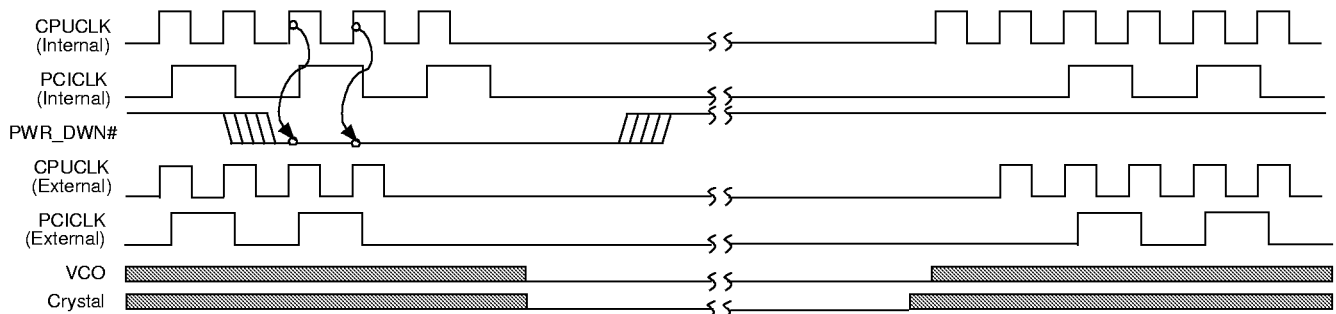(Internal)

PCICLK
(Free-Running)
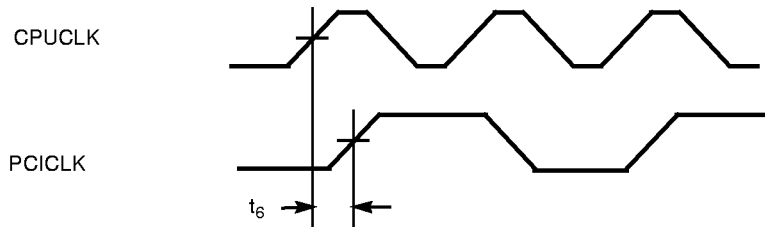
$\overline{\text{CPU\_STOP}}$

CPUCLK
(External)

Notes:
13. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
14. CPU_STOP may be applied asynchronously. It is synchronized internally.

Switching Waveforms (continued)

PCI_STOP [15, 16]

CPUCLK
(Internal)

PCICLK
(Internal)

PCICLK
(Free-Running)

PCI_STOP

PCICLK
(External)

PWR_DOWN

CPUCLK
(Internal)

PCICLK
(Internal)
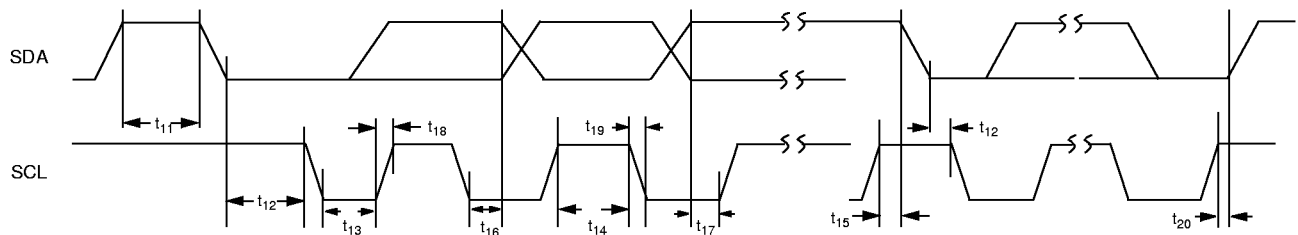
PWR_DWN#

CPUCLK
(External)

PCICLK
(External)

VCO

Crystal

Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Timing Requirements for the I^{2}C Bus

SDA

SCL

t_{11} t_{18} t_{19} t_{12}

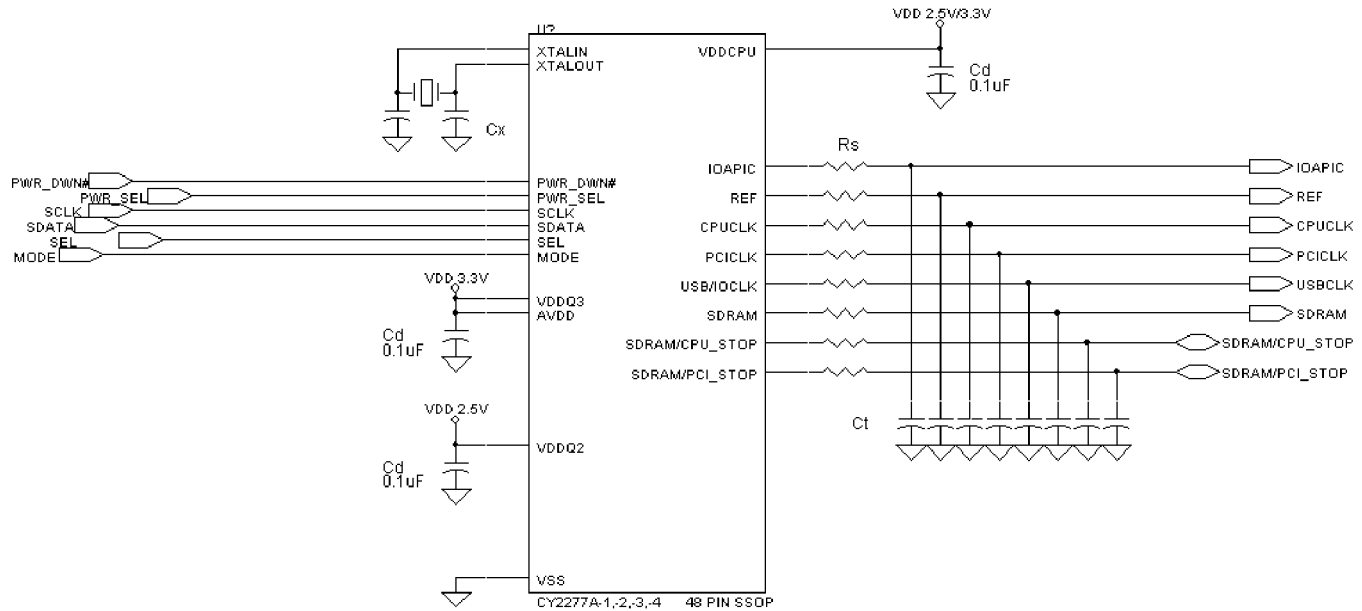t_{12} t_{13} t_{16} t_{14} t_{17} t_{15} t_{20}

Notes:
15. PCICLK on and PCICLK off latency is 1 rising edge of the external PCICLK.
16. PCI_STOP may be applied asynchronously. It is synchronized internally.

Application Information

Clock traces must be terminated with either series or parallel termination, as they are normally done.

Application Circuit

Cd = DECOUPLING CAPACITORS

Ct = OPTIONAL EMI-REDUCING CAPACITORS

Cx = OPTIONAL LOAD MATCHING CAPACITOR

Rs = SERIES TERMINATING RESISTORS

Summary

- A parallel-resonant crystal should be used as the reference to the clock generator. The operating frequency and C_{LOAD} of this crystal should be as specified in the data sheet. Optional trimming capacitors may be needed if a crystal with a different C_{LOAD} is used. Footprints must be laid out for flexibility.

- Surface mount, low-ESR, ceramic capacitors should be used for filtering. Typically, these capacitors have a value of 0.1 μF. In some cases, smaller value capacitors may be required.

- The value of the series terminating resistor satisfies the following equation, where R_{trace} is the loaded characteristic impedance of the trace, R_{out} is the output impedance of the clock generator (specified in the data sheet), and R_{series} is the series terminating resistor.

$$R_{series} \geq R_{trace} - R_{out}$$

- Footprints must be laid out for optional EMI-reducing capacitors, which should be placed as close to the terminating resistor as is physically possible. Typical values of these capacitors range from 4.7 pF to 22 pF.

- A Ferrite Bead **may** be used to isolate the Board V_{DD} from the clock generator V_{DD} island. Ensure that the Ferrite Bead offers greater than 50Ω impedance at the clock frequency, under loaded DC conditions. Please refer to the application note "Layout and Termination Techniques for Cypress Clock Generators" for more details.

- If a Ferrite Bead is used, a 10 μF– 22 μF tantalum bypass capacitor should be placed close to the Ferrite Bead. This capacitor prevents power supply droop during current surges.

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Test Circuit
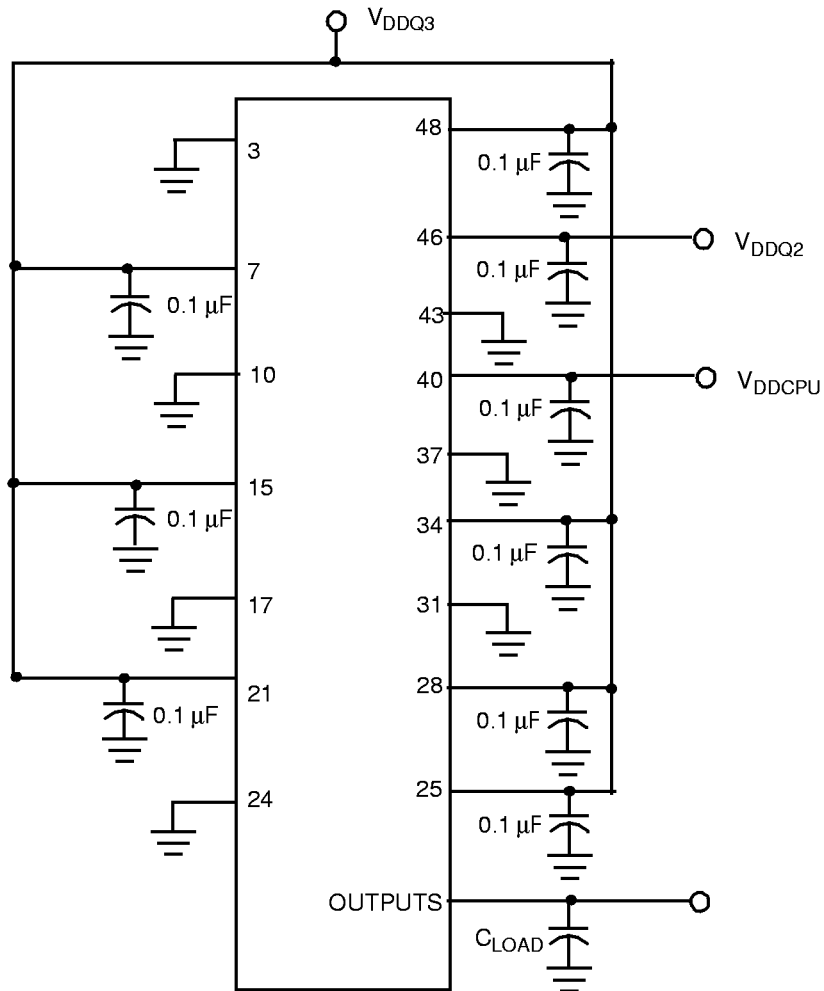
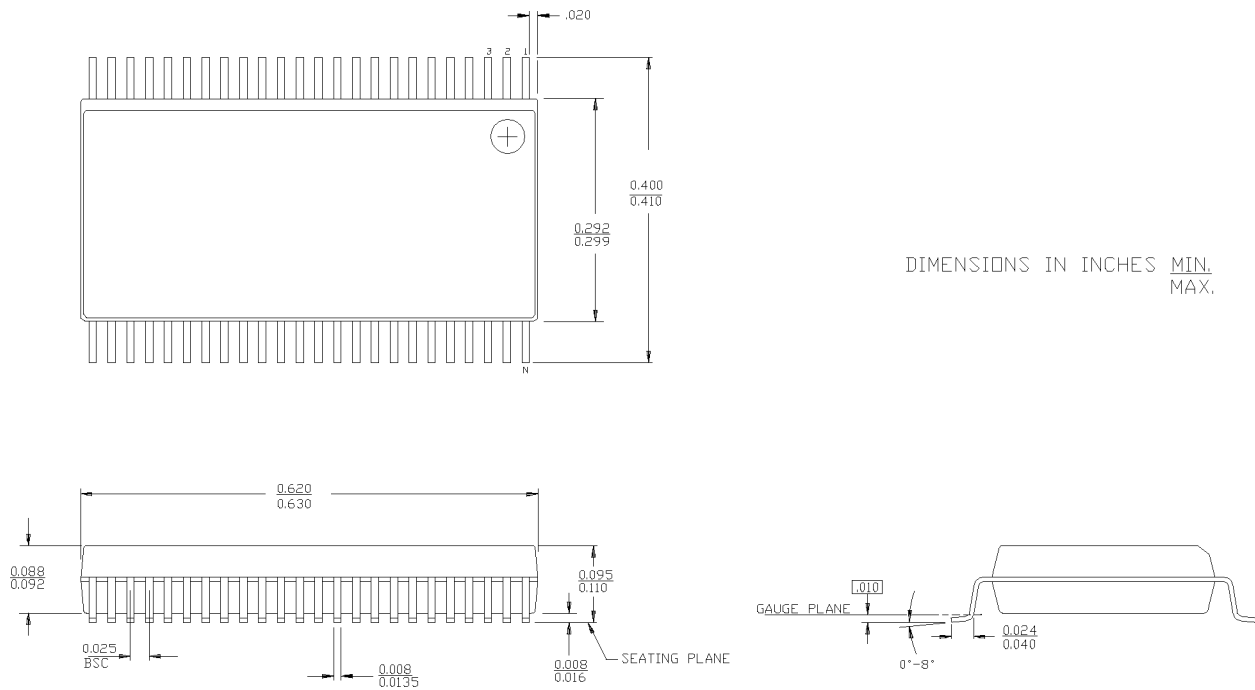Note: All capacitors should be placed as close to each pin as possible.

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2277APAC-1	Z48	48-Pin TSSOP	Commercial
CY2277APVC-1	O48	48-Pin SSOP	Commercial
CY2277APVC-2	O48	48-Pin SSOP	Commercial
CY2277APVC-3	O48	48-Pin SSOP	Commercial
CY2277APAC-4	Z48	48-Pin TSSOP	Commercial
CY2277APVC-4	O48	48-Pin SSOP	Commercial

Document #: 38–00612

Package Diagram

48-Lead Shrunk Small Outline Package O48

DIMENSIONS IN INCHES MIN.
MAX.

48-Lead Thin Shrunk Small Outline Package Z48

DIMENSIONS IN INCHES MIN.
MAX.