

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74LS161A

## Synchronous 4-bit Binary Counter (direct clear)

REJ03D0445-0200

Rev.2.00

Feb.18.2005

This synchronous 4-bit binary counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs changes coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the output may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the  $Q_A$  output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

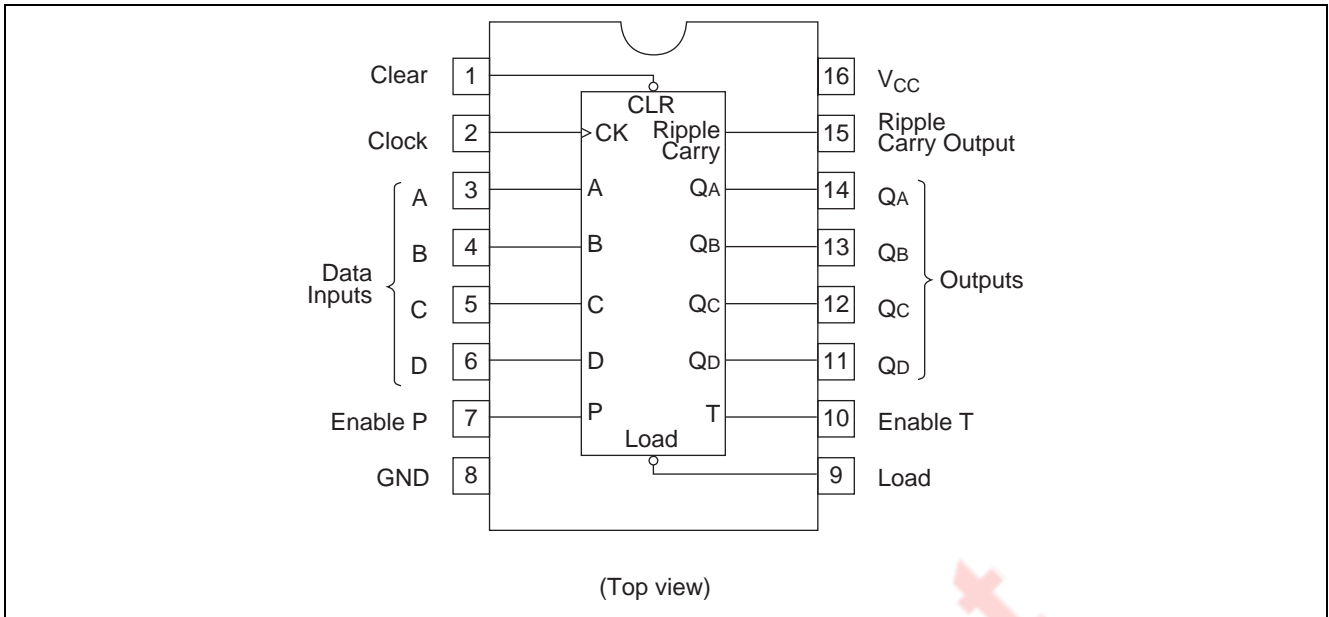
### Features

- Ordering Information

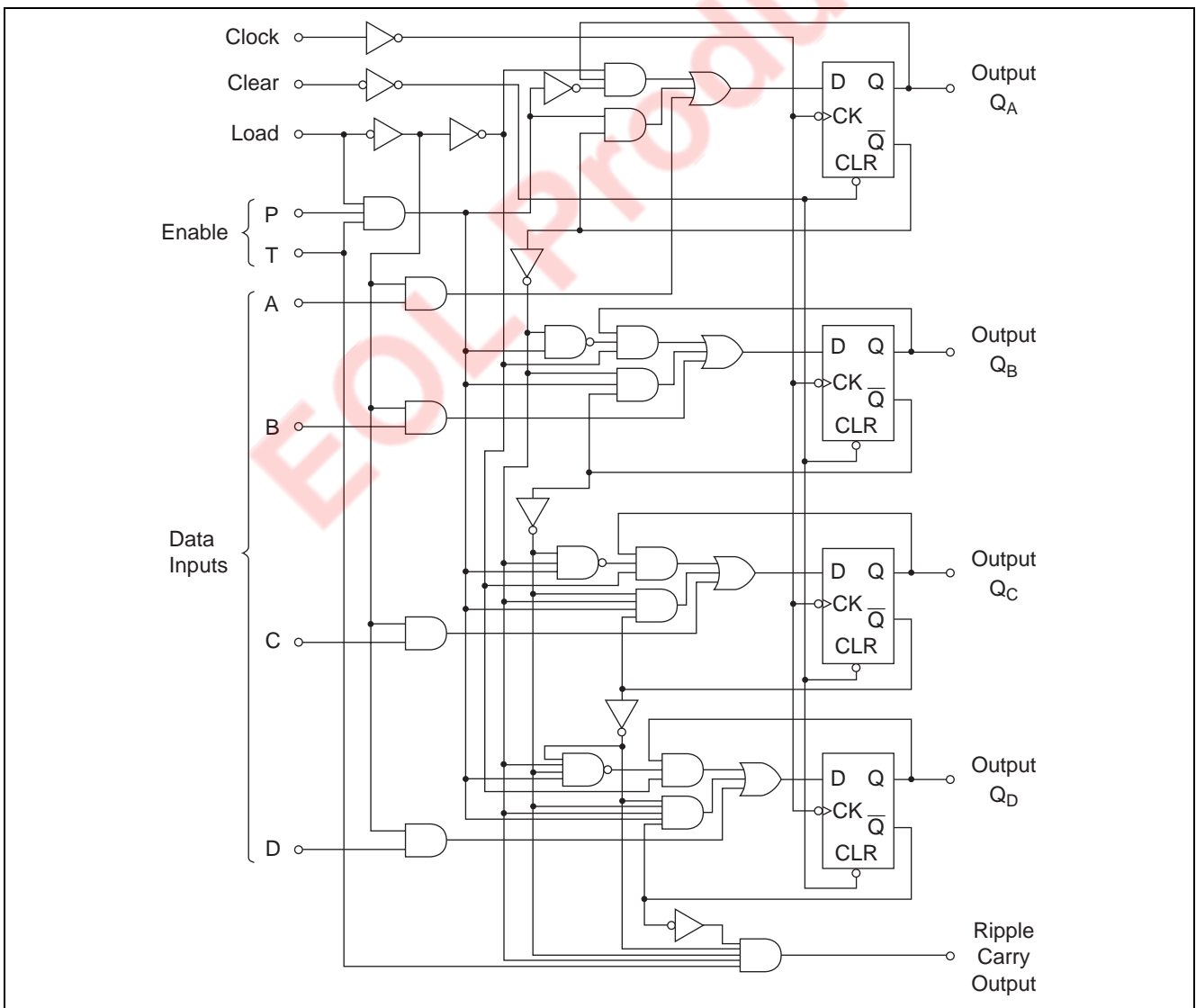
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS161AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS161AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS161ARPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Block Diagram



### Absolute Maximum Ratings

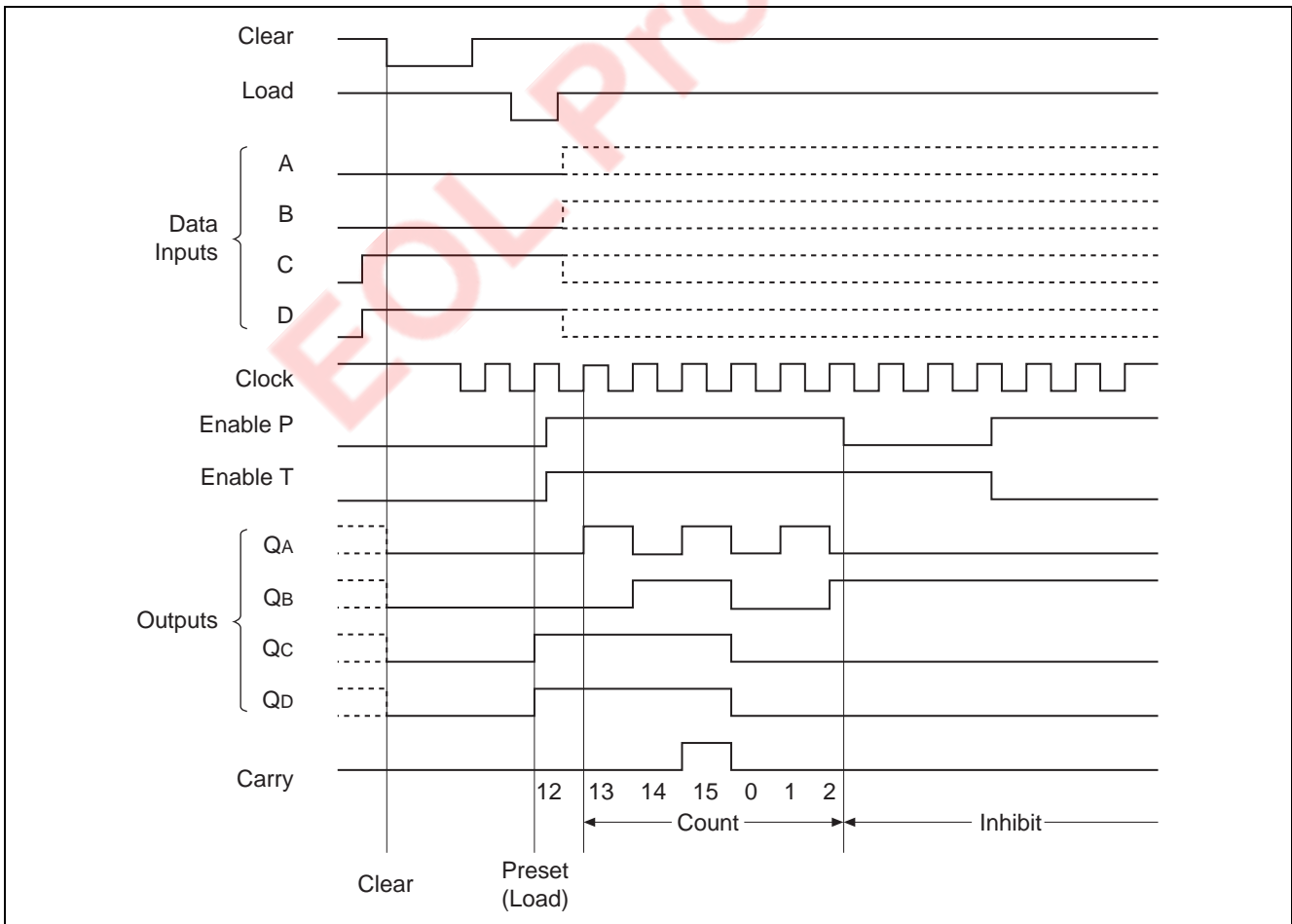
Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	$V_{IN}$	7	V
Power dissipation	$P_T$	400	mW
Storage temperature	Tstg	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

### Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	$\mu A$
	$I_{OL}$	—	—	8	mA
Operating temperature	Topr	-20	25	75	°C
Clock frequency	$f_{clock}$	0	—	25	MHz
Clock pulse width	$t_w (clock)$	25	—	—	ns
Clear pulse width	$t_w (clear)$	20	—	—	ns
Setup time	A, B, C, D	$t_{su}$	—	—	ns
	Enable P, T		—	—	ns
	Load		—	—	ns
Hold time	$t_h$	3	—	—	ns

### Typical Clear, Preset, and Inhibit Sequence



**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V <sub>IH</sub>	2.0	—	—	V	
		V <sub>IL</sub>	—	—	0.8	V	
Output voltage		V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA
		V <sub>OL</sub>	—	—	0.4	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V
—	—		0.5				
Input current	Data, Enable P	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	Load, Clock, Enable T		—	—	40		
	Clear		—	—	20		
	Data, Enable P	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	Load, Clock, Enable T		—	—	-0.8		
	Clear		—	—	-0.4		
	Data, Enable P	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
	Load, Clock, Enable T		—	—	0.2		
	Clear		—	—	0.1		
Short-circuit output current		I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V
Supply current**		I <sub>CCH</sub>	—	18	31	mA	V <sub>CC</sub> = 5.25 V
		I <sub>CCL</sub>	—	19	32	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage		V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C

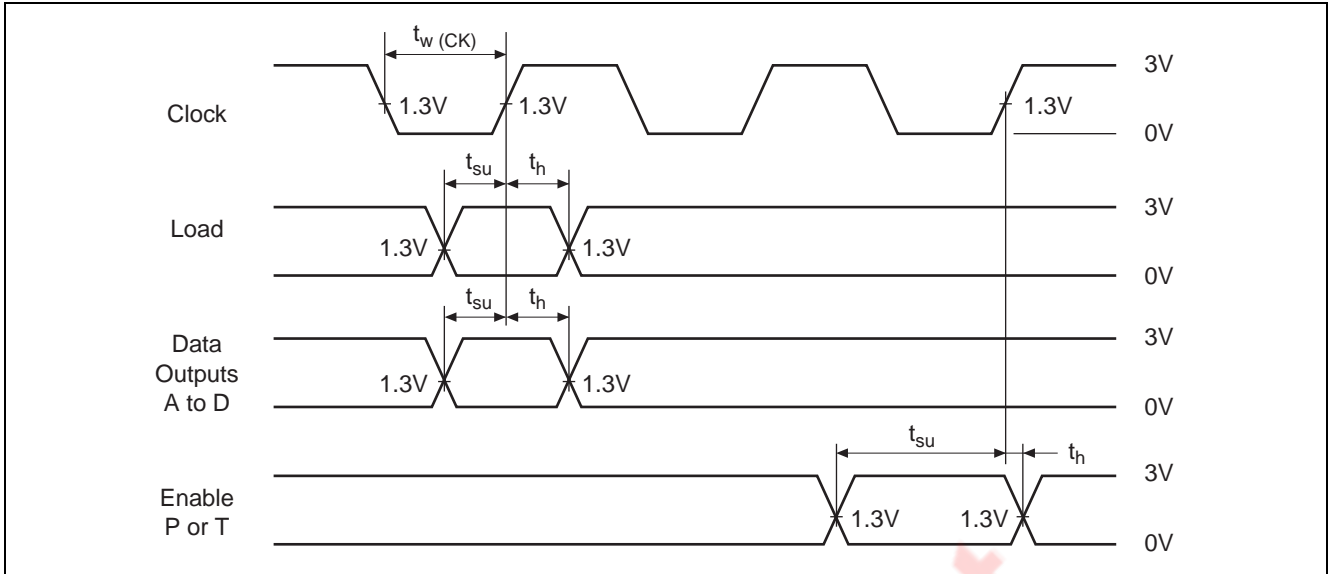
\*\* I<sub>CCH</sub> is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. I<sub>CCL</sub> is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

**Switching Characteristics**

(V<sub>CC</sub> = 5 V, Ta = 25°C)

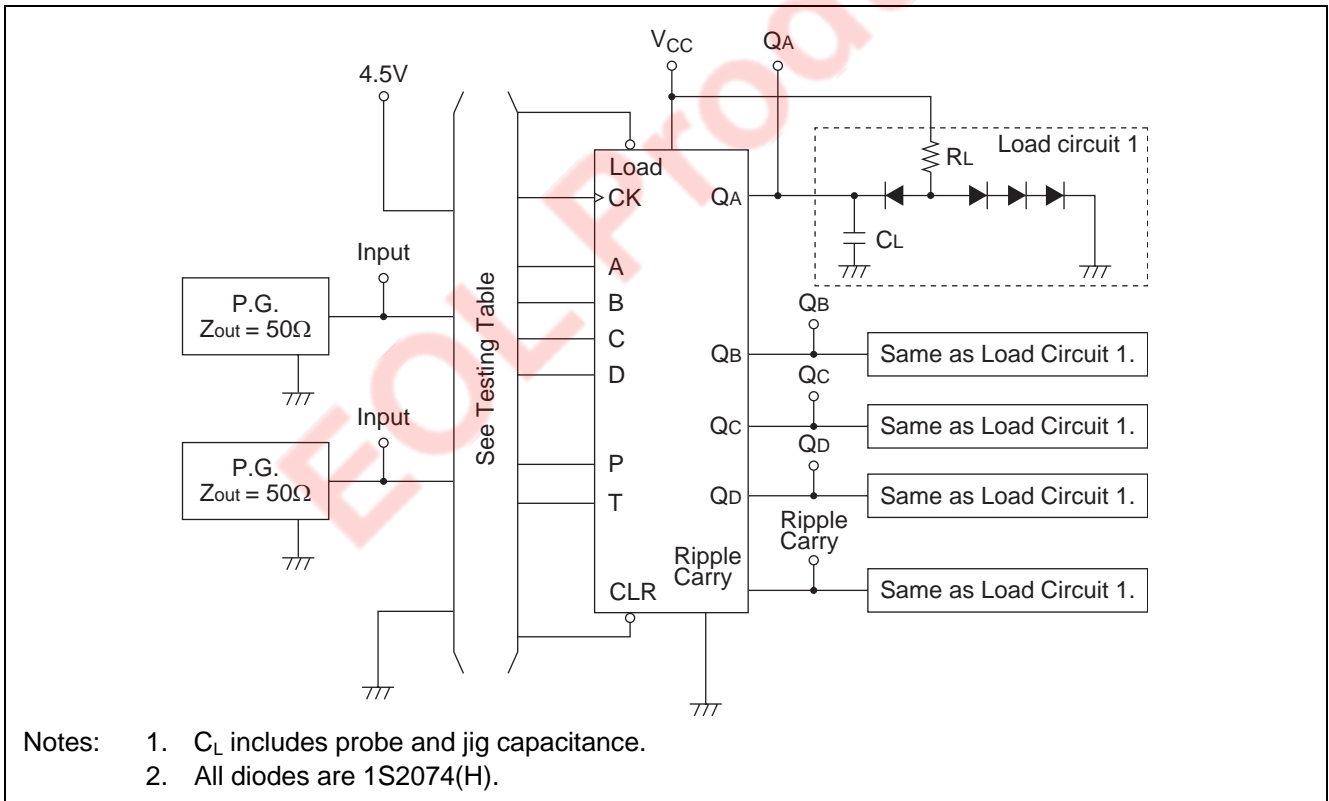
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f <sub>max</sub>	Clock	Q <sub>A</sub> to Q <sub>D</sub>	25	32	—	MHz	
Propagation delay time	t <sub>PLH</sub>	Clock	Ripple	—	20	35	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
	t <sub>PHL</sub>		Carry	—	18	35	ns	
	t <sub>PLH</sub>	Clock (Load = "H")	Q <sub>A</sub> to Q <sub>D</sub>	—	13	24	ns	
	t <sub>PHL</sub>			—	18	27	ns	
	t <sub>PLH</sub>	Clock (Load = "L")	Q <sub>A</sub> to Q <sub>D</sub>	—	13	24	ns	
	t <sub>PHL</sub>			—	18	27	ns	
	t <sub>PLH</sub>	Enable T	Ripple Carry	—	9	14	ns	
	t <sub>PHL</sub>			—	9	14	ns	
	t <sub>PHL</sub>	Clear	Q <sub>A</sub> to Q <sub>D</sub>	—	20	28	ns	

### Timing Method



### Testing Method

#### Test Circuit



- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2. All diodes are 1S2074(H).

Testing Table

Item	From input to output	Inputs								
		Clear	Load	Enable		Clock	Data			
				P	T		A	B	C	D
$f_{max}$		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
$t_{PLH}$ $t_{PHL}$	CK Ripply → Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*
	Enable T → Ripple Carry	4.5V	GND	4.5V	IN	IN*	4.5V	4.5V	4.5V	4.5V
	CLR → Q	IN	GND	GND	GND	IN*	4.5V	4.5V	4.5V	4.5V

Notes: \*. For initialized

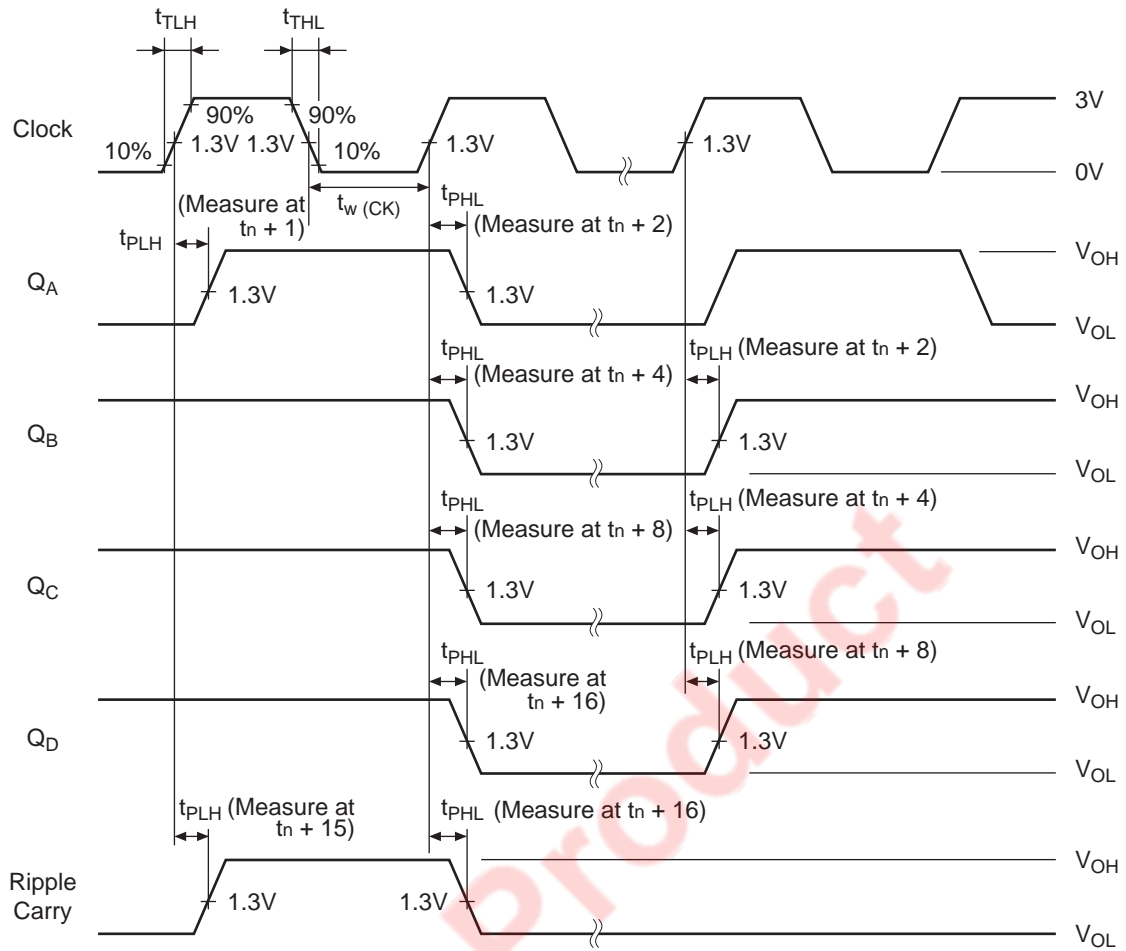
Item	From input to output	Outputs				
		Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>	Ripple Carry
$f_{max}$		OUT	OUT	OUT	OUT	OUT
$t_{PLH}$ $t_{PHL}$	CK→Ripple Carry	—	—	—	—	OUT
	CK→Q	OUT	OUT	OUT	OUT	—
	CK→Q	OUT	OUT	OUT	OUT	—
	Enable T→Ripple Carry	—	—	—	—	OUT
	CLR→Q	OUT	OUT	OUT	OUT	—

EOL Product



Waveforms 1

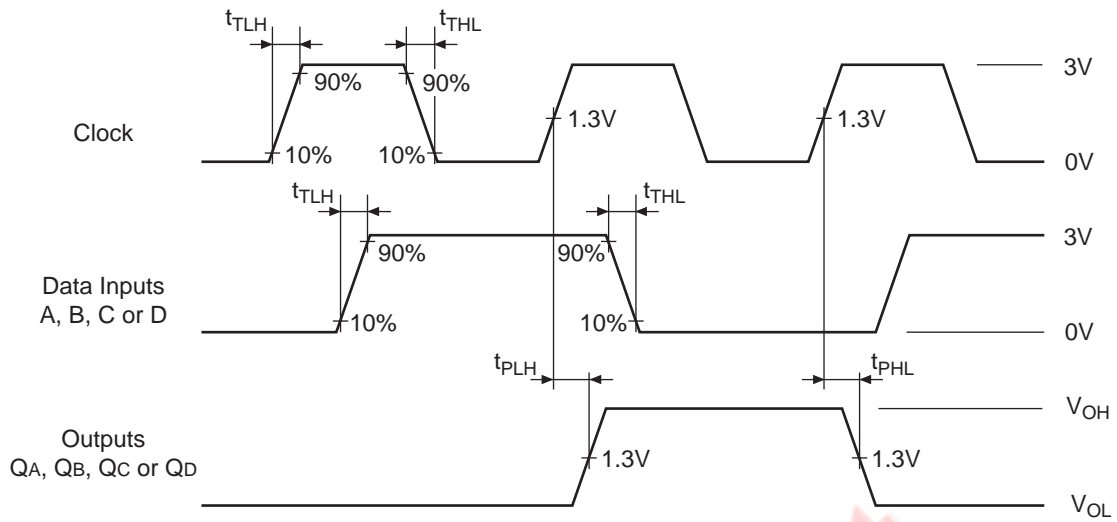
$f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Clock→Q, Ripple Carry)



Note: Clock input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz, duty cycle 50% and :  $f_{max} t_{TLH} = t_{THL} \leq 2.5$  ns.  
 $t_n$  is reference bit time when all outputs are low.

Waveforms 2

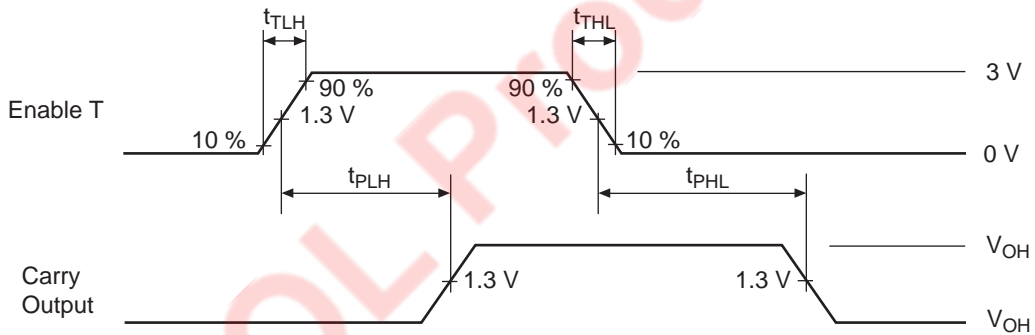
$t_{PLH}$ ,  $t_{PHL}$ , (Clock→Q)



Note: Input pulse:  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, Clock input: PRR = 1 MHz, duty cycle 50%, Data input: PRR = 500 kHz, duty cycle 50%

Waveforms 3

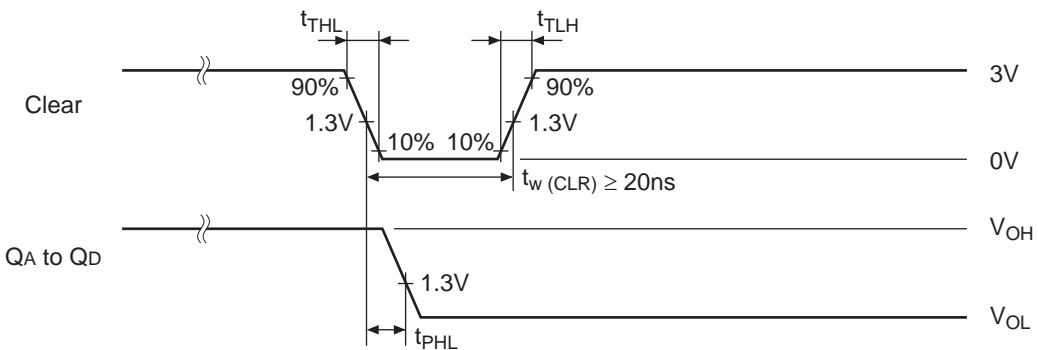
$t_{PLH}$ ,  $t_{PHL}$ , (Enable T→Ripple Carry)



Note: Input pulse:  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz

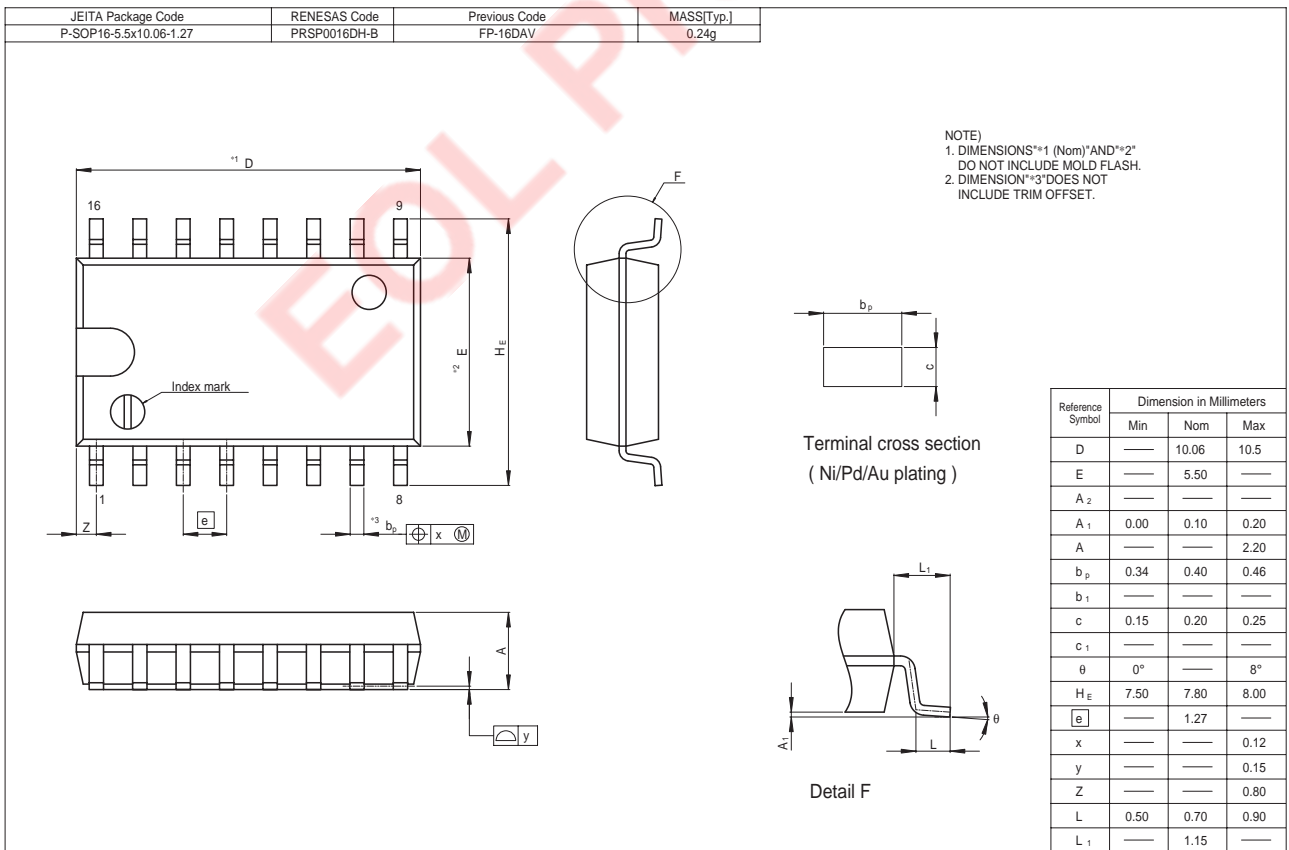
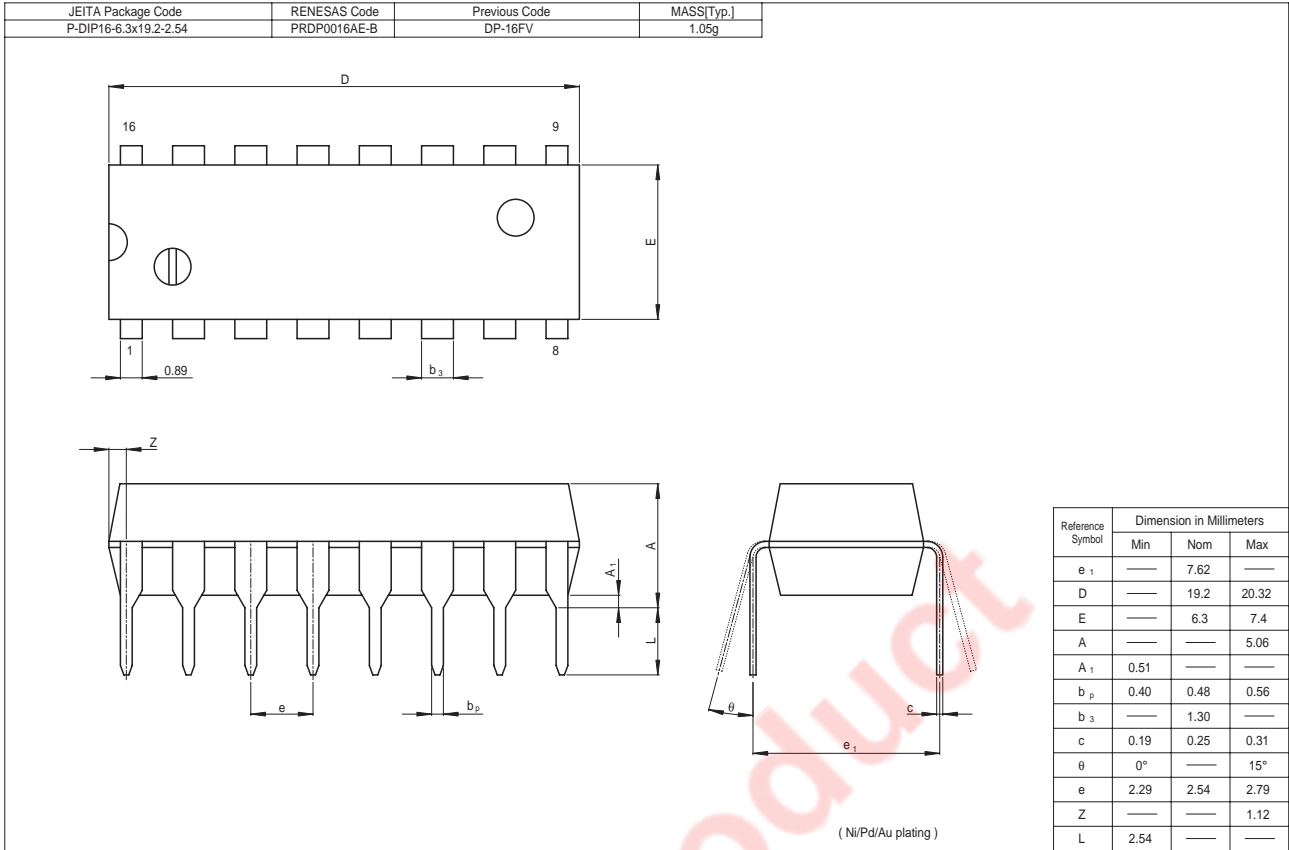
Waveforms 4

$t_{PHL}$ , (Clear→Q)

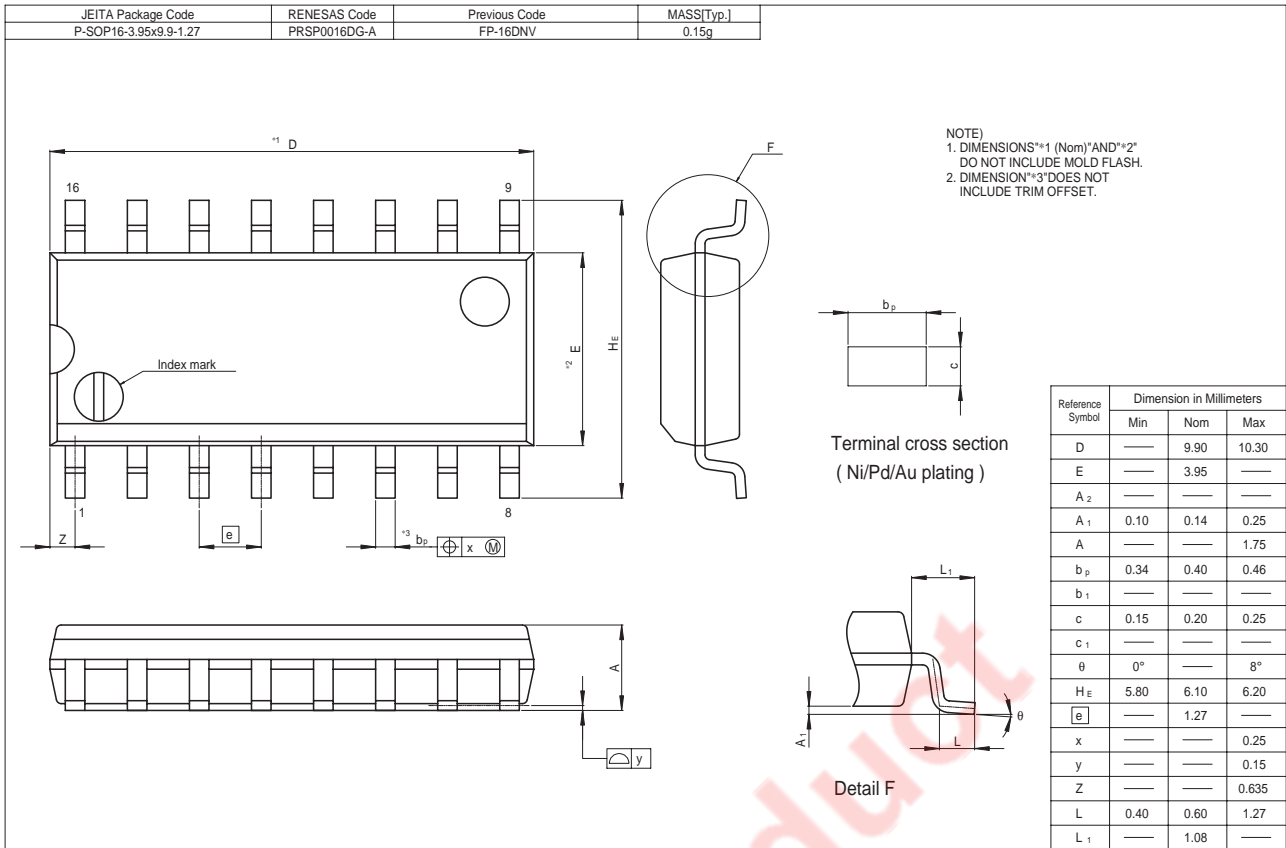


Note: Input pulse:  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns

Package Dimensions



# HD74LS161A



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