

HM658512 Series

524288-Word × 8-Bit High Speed Pseudo Static RAM

Features

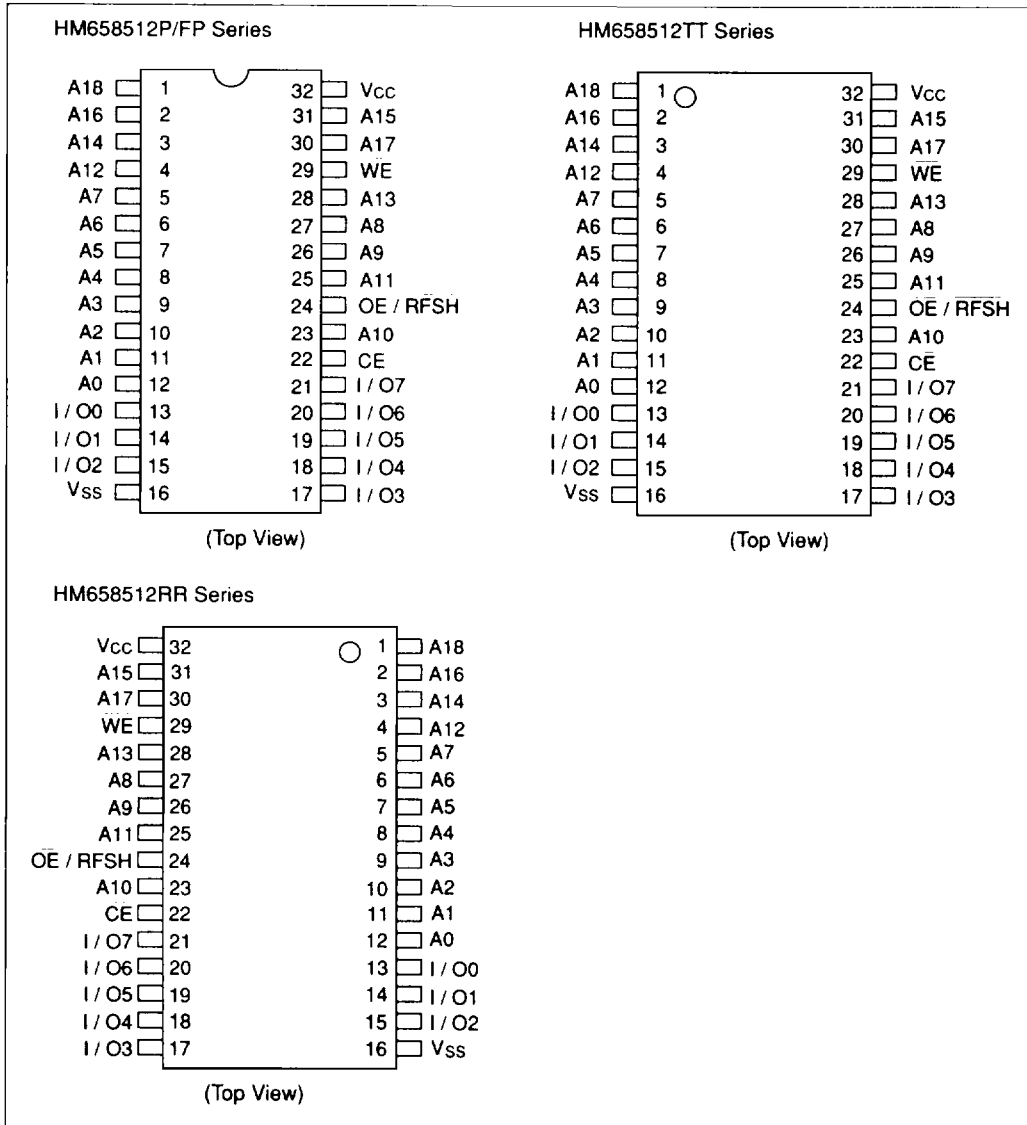
- Single 5 V ($\pm 10\%$)
- High speed
 - Access time
CE access time: 80/85/100/120 ns
 - Cycle time
Random read/write cycle time:
130/160/190 ns
- Low power
 - 250 mW typ active
 - 350 μ W typ standby (L-version)
 - 200 μ W typ standby (LV-version)
- All inputs and outputs TTL compatible
- Package
 - 32-pin dual-in-line plastic package
 - 32-pin SOP package
 - 32-pin TSOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
 - L-version: Address refresh
LV-version Automatic refresh
Self refresh
 - D-version: Address refresh
Automatic refresh

Ordering Information

Type No.	Access	Package
HM658512LP-8	80 ns	600 mil 32-pin plastic DIP (DP-32)
HM658512LP-10	100 ns	
HM658512LP-12	120 ns	
HM658512LP-8V	80 ns	
HM658512LP-10V	100 ns	
HM658512LP-12V	120 ns	
HM658512DP-8	80 ns	
HM658512DP-10	100 ns	
HM658512DP-12	120 ns	
HM658512LFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658512LFP-85	85 ns	
HM658512LFP-10	100 ns	
HM658512LFP-12	120 ns	
HM658512LFP-8V	80 ns	
HM658512LFP-85V	85 ns	
HM658512LFP-10V	100 ns	
HM658512LFP-12V	120 ns	
HM658512DFP-8	80 ns	
HM658512DFP-10	100 ns	
HM658512DFP-12	120 ns	
HM658512DTT-8	80 ns	400 mil 32-pin plastic TSOP (TTP-32D)
HM658512DTT-10	100 ns	
HM658512DTT-12	120 ns	
HM658512LTT-8	80 ns	
HM658512LTT-85	85 ns	
HM658512LTT-10	100 ns	
HM658512LTT-12	120 ns	
HM658512LTT-8V	80 ns	
HM658512LTT-85V	85 ns	
HM658512LTT-10V	100 ns	
HM658512LTT-12V	120 ns	
HM658512DRR-8	80 ns	400 mil 32-pin plastic TSOP reverse type (TTP-32DR)
HM658512DRR-10	100 ns	
HM658512DRR-12	120 ns	
HM658512LRR-8	80 ns	
HM658512LRR-10	100 ns	
HM658512LRR-12	120 ns	
HM658512LRR-8V	80 ns	
HM658512LRR-10V	100 ns	
HM658512LRR-12V	120 ns	

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Pin Arrangement



Pin Description

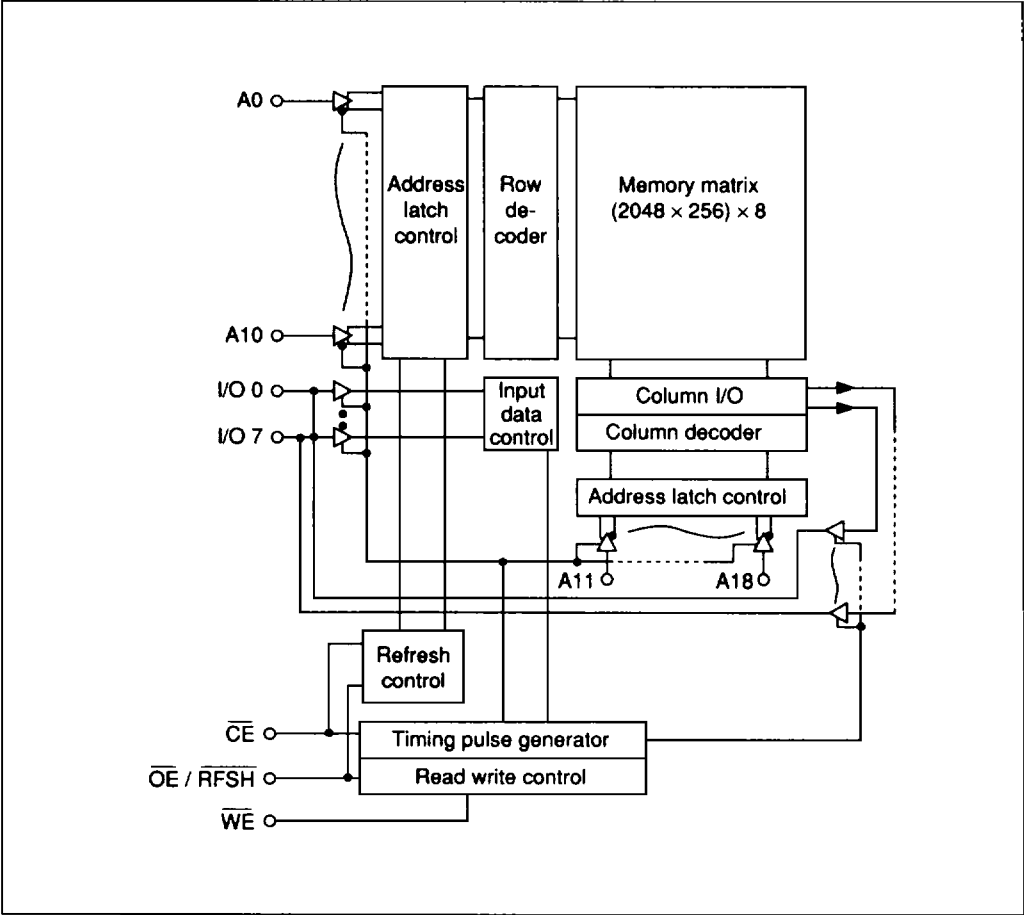
Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
CE	Chip enable
OE/RFSH	Output enable/refresh

Pin name	Function
WE	Write enable
Vcc	Power supply
Vss	Ground

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Block Diagram



Function Table

\overline{CE}	$\overline{OE/RFSH}$	\overline{WE}	I/O pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh *2
H	H	X	High-Z	Standby

Notes: 1. X means don't care
 2. Self refresh is guaranteed only for L-version and LV-version.

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	-1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	-1.0 *1	—	0.8	V

Note: 1. V_{IL} min = -3.0 V for pulse width 30 ns

DC Characteristics ($T_a = 0$ to +70°C, $V_{CC} = 5$ V \pm 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	—	75	mA	$I_{I/O} = 0$ $t_{cyc} = \text{min}$
Standby power supply current	I_{SB1}	—	1	2	mA	$CE = V_{IH}$, $V_{in} \geq 0$ V $OE/RFSH = V_{IH}$
	I_{SB2}	—	20 *1	200 *1	μ A	$CE \geq V_{CC} - 0.2$ V, $V_{in} \geq 0$ V $OE/RFSH \geq V_{CC} - 0.2$ V
Operating power supply current in self refresh mode	I_{CC2}	—	1 *1,2	2 *1,2	mA	$CE = V_{IH}$ $OE/RFSH = V_{IL}$, $V_{in} \geq 0$ V
	I_{CC3}	—	70 *1	200 *1	μ A	$CE \geq V_{CC} - 0.2$ V $OE/RFSH \leq 0.2$ V $V_{in} \geq 0$ V
Input leakage current	I_{LI}	-10	—	10	μ A	$V_{CC} = 5.5$ V $V_{in} = V_{SS}$ to V_{CC}

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LV-version.

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output leakage current	I _{LO}	-10	—	10	μA	OE/RFSH = V _{IH} V _{I/O} = V _{SS} to V _{CC}
Output voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
	V _{OH}	2.4	—	—	V	I _{OH} = -1 mA

Capacitance

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance	C _{I/O}	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

Input pulse levels: 2.4 V, 0.4 V

Input rise and fall times: 5 ns

Timing measurement level: 2.2 V, 0.8 V

Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V

Output load: 1 TTL and 100 pF

Parameter	Symbol	HM658512-8		HM658512-85		HM658512-10		HM658512-12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	130	—	135	—	160	—	190	—	ns	
Chip enable access time	t _{CEA}	—	80	—	85	—	100	—	120	ns	
Read-modify-write cycle time	t _{RWC}	180	—	190	—	220	—	260	—	ns	
Output enable access time	t _{OEA}	—	30	—	30	—	40	—	50	ns	
Chip disable to output in high-Z	t _{CHZ}	0	25	0	25	0	25	0	30	ns	1, 2

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$) (cont)

Parameter	Symbol	HM658512-8		HM658512-85		HM658512-10		HM658512-12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Chip enable to output in low-Z	tCLZ	20	—	20	—	20	—	20	—	ns	2
Output disable to output in high-Z	tOHZ	—	25	—	25	—	25	—	30	ns	1
Output enable to output in low-Z	tOLZ	0	—	0	—	0	—	0	—	ns	2
Chip enable pulse width	tCE	80ns	10 μ s	85ns	10 μ s	100ns	10 μ s	120ns	10 μ s		
Chip enable precharge time	tP	40	—	40	—	50	—	60	—	ns	
Address setup time	tAS	0	—	0	—	0	—	0	—	ns	
Address hold time	tAH	20	—	20	—	25	—	30	—	ns	
Read command setup time	tRCS	0	—	0	—	0	—	0	—	ns	
Read command hold time	tRCH	0	—	0	—	0	—	0	—	ns	
Write command pulse width	tWP	25	—	25	—	30	—	35	—	ns	
Chip enable to end of write	tCW	80	—	85	—	100	—	120	—	ns	
Chip enable to output delay time	tOCD	0	—	0	—	0	—	0	—	ns	
Output enable hold time	tOHC	15	—	15	—	15	—	15	—	ns	
Data in to end of write	tDW	20	—	20	—	25	—	30	—	ns	
Data in hold time for write	tDH	0	—	0	—	0	—	0	—	ns	
Output active from end of write	tOW	5	—	5	—	5	—	5	—	ns	2
Write to output in high-Z	tWHZ	—	20	—	20	—	25	—	30	ns	1
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	

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AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

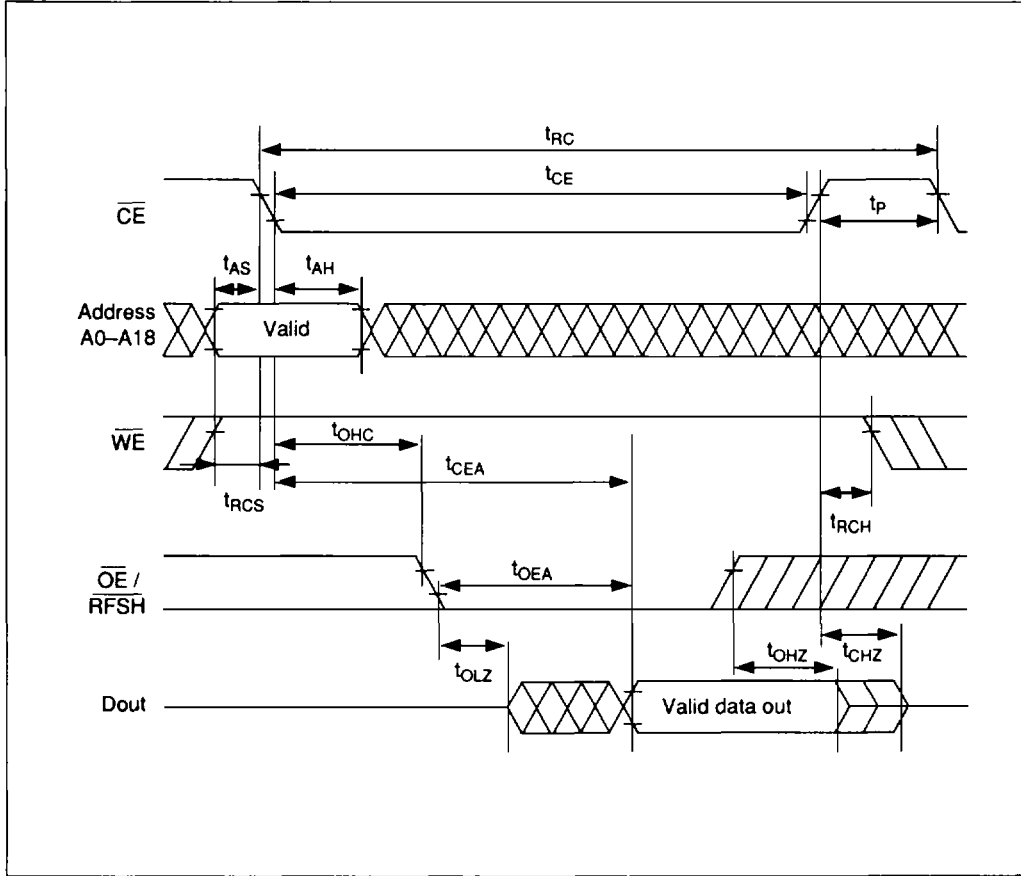
Parameter	Symbol	HM658512-8		HM658512-85		HM658512-10		HM658512-12		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Refresh command delay time	t _{RFD}	40	—	40	—	50	—	60	—	ns	
Refresh precharge time	t _{FP}	40	—	40	—	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t _{FAP}	80ns	8μs	80ns	8μs	80ns	8μs	80ns	8μs		
Automatic refresh cycle time	t _{FC}	130	—	135	—	160	—	190	—	ns	
Refresh command pulse width for self refresh	t _{FAS}	8	—	8	—	8	—	8	—	μs	
Refresh reset time from self refresh	t _{RFS}	600	—	600	—	600	—	600	—	ns	
Refresh period	t _{REF}	—	32	—	32	—	32	—	32	ms	2048 cycle

- Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
 2. t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5 ns and not 100% tested.
 3. A write occurs during the overlap of low CE and low WE.
 4. If the CE low transition occurs simultaneously with or later from the WE low transition, the output buffers remain in high impedance state.
 5. In write cycle, OE or WE must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to OE or WE turning on output buffers.
 6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
 7. After power-up, pause for more than 100 μs and execute at least 8 initialization cycles.
 8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15μs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
 9. This characteristics is guaranteed only for L-version and LL-version.
 10. At the end of self refresh, refresh reset time (t_{RFS}) is required to reset the internal self refresh operation of the RAM. During t_{RFS}, CE and OE/RFSH must be kept high. If auto refresh follows self refresh, low transition of OE/RFSH at the beginning of auto refresh must not occur during t_{RFS} period.

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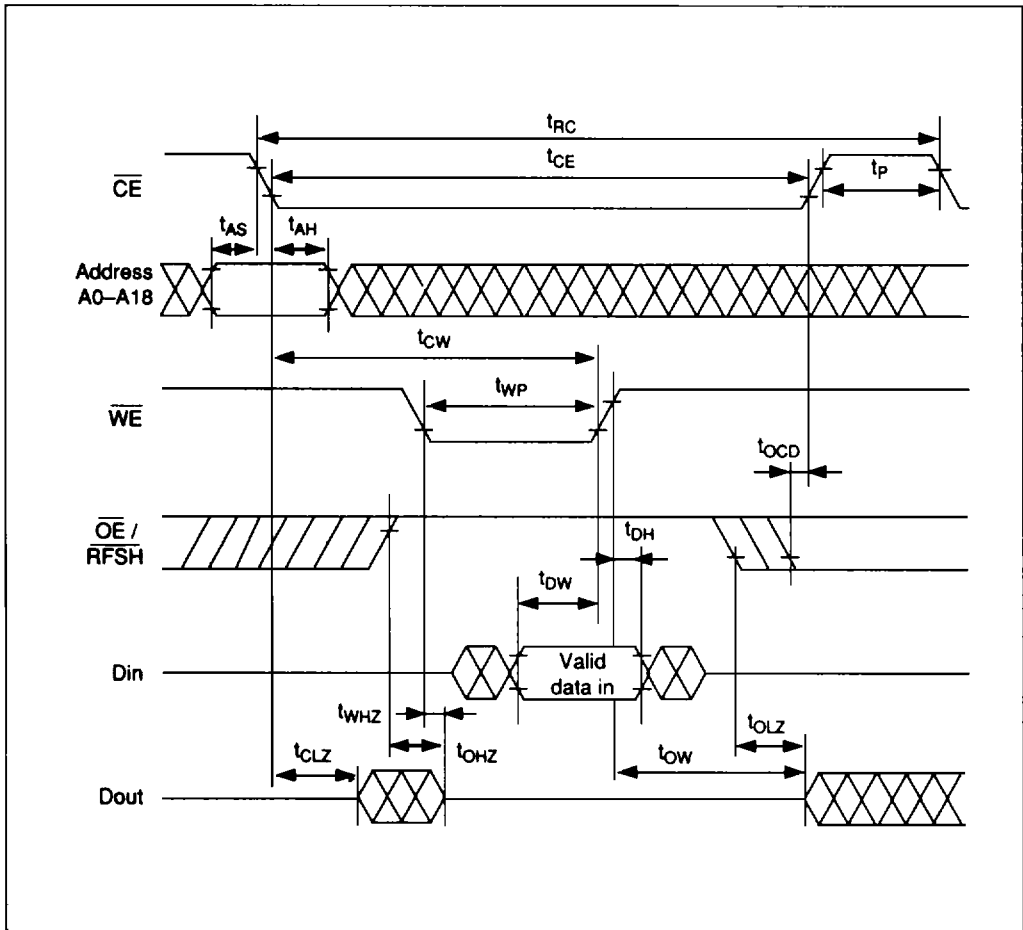
Timing Waveforms

Read Cycle



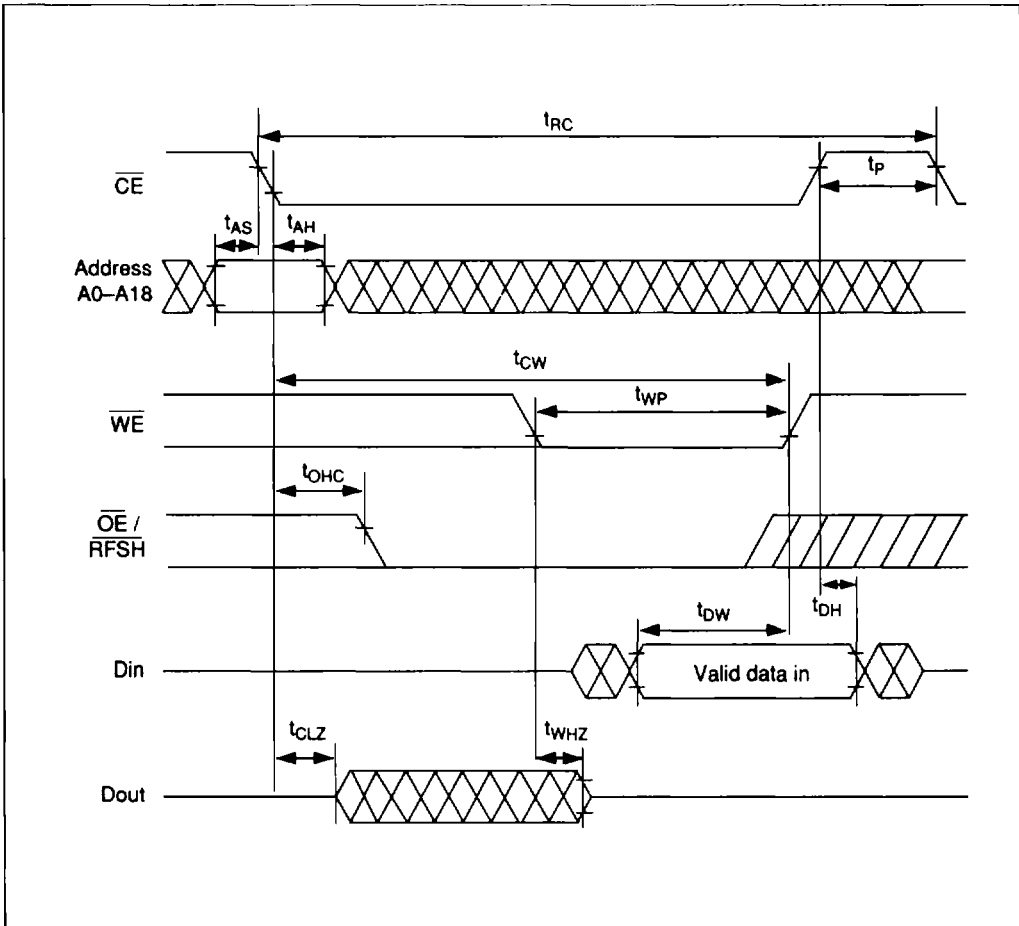
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Write Cycle (1) (\overline{OE} High)

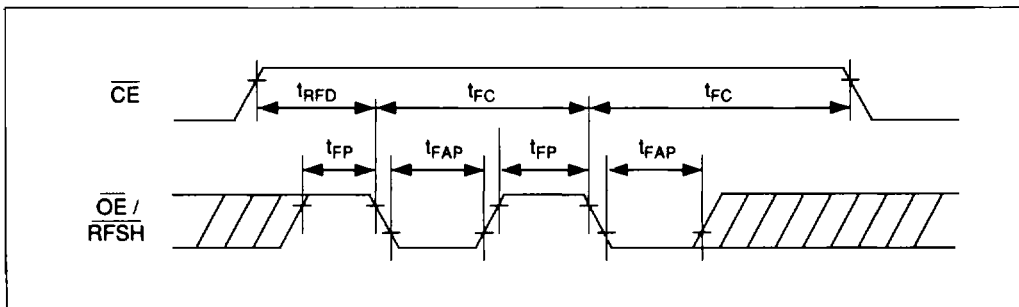


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Write Cycle (2) (\overline{OE} Low)



Automatic Refresh Cycle

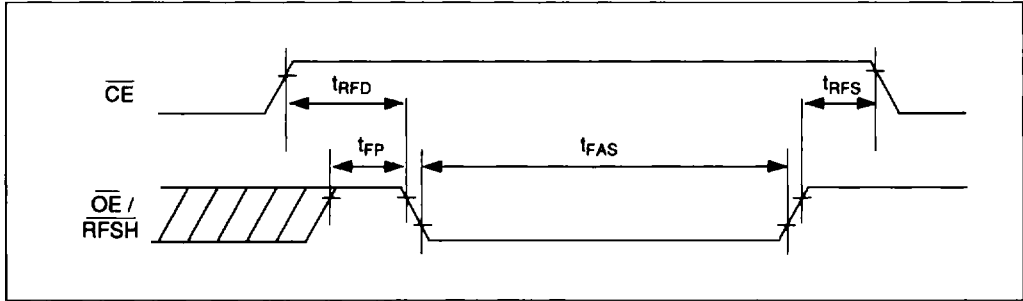


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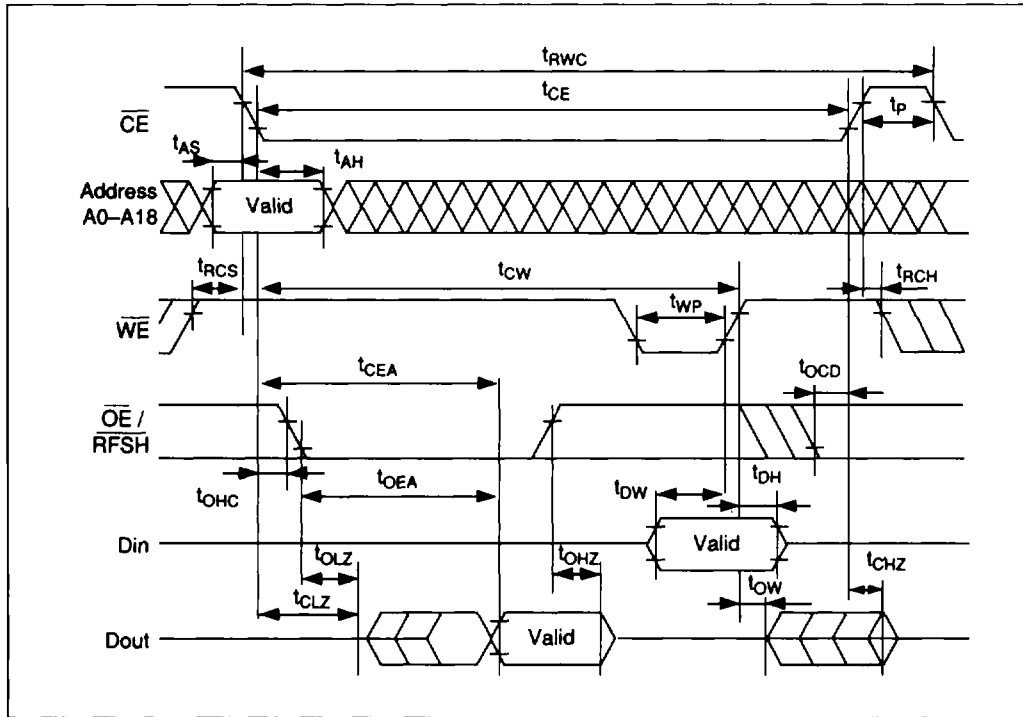
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Self Refresh Cycle



Read-Modify-Write Cycle



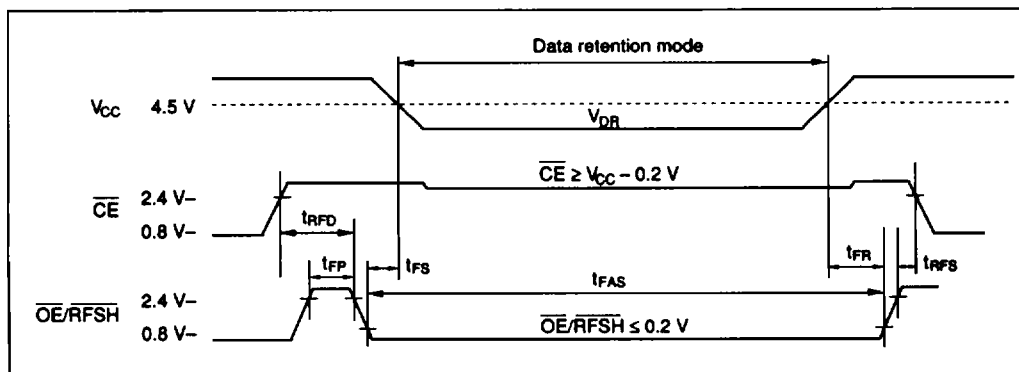
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Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for LV-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	3.0	—	5.5	V	
Self refresh current	I_{CCDR}	—	—	50	μA	$V_{CC} = 3.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ $\overline{OE}/\overline{RFSH} \leq 0.2$ $V_{in} \geq 0\text{ V}$
		—	—	100	μA	$V_{CC} = 5.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ $\overline{OE}/\overline{RFSH} \leq 0.2$ $V_{in} \geq 0\text{ V}$
Refresh setup time	t_{FS}	0	—	—	ns	
Operation recovery time	t_{FR}	5	—	—	ms	

Low V_{CC} Data Retention Timing Waveform



- Notes:
1. Rise time and fall time of power supply voltage must be smaller than 0.05 V/ms.
 2. Keep $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ during data retention mode.
 3. Regarding t_{RFD} , t_{FP} , t_{FAS} and t_{RFS} , refer to AC characteristics.
 4. Input voltage should be lower than $V_{CC} + 1.5\text{ V}$ in data retention mode.