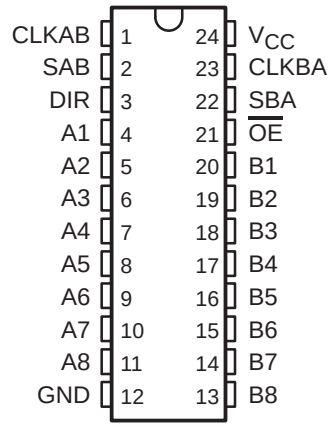
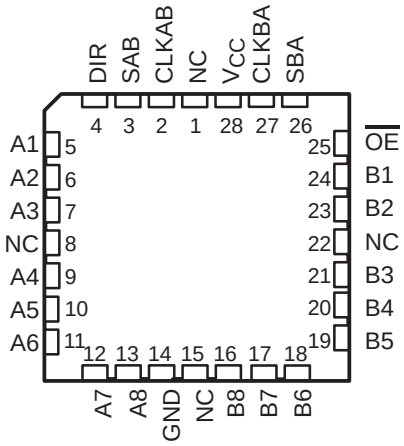
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs**

SN54ABT646 . . . JT PACKAGE
SN74ABT646 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ′ABT646.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

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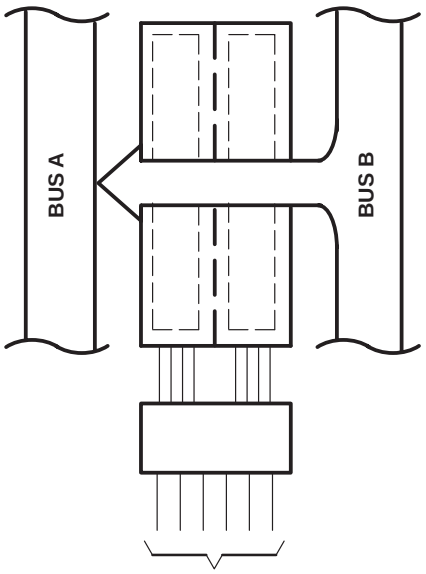
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

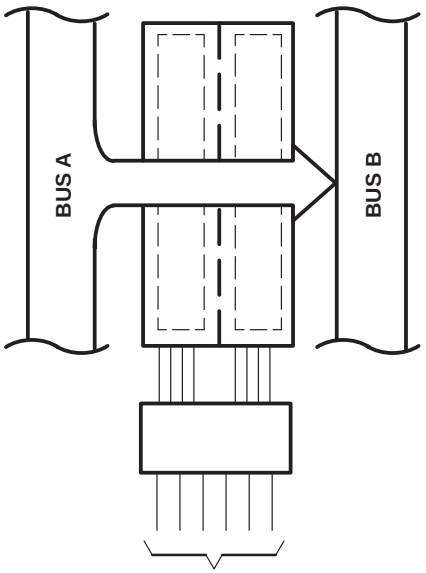
The SN54ABT646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT646 is characterized for operation from –40°C to 85°C.

EPIC-IIB is a trademark of Texas Instruments Incorporated.



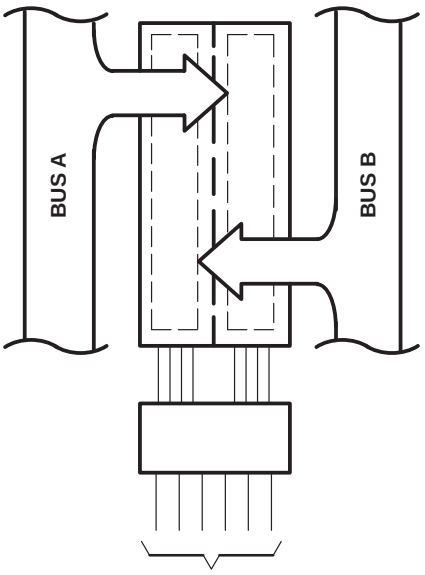
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



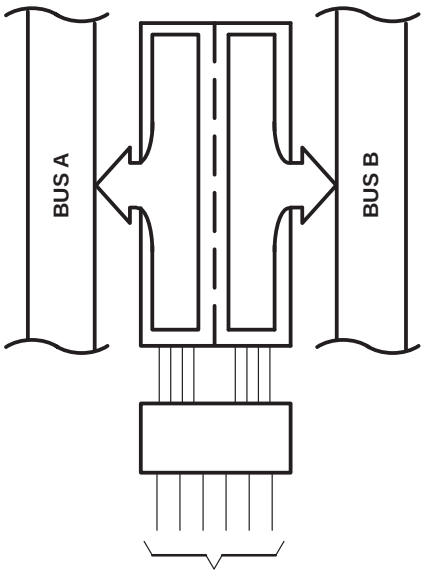
21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



21	3	1	23	2	22
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	L	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

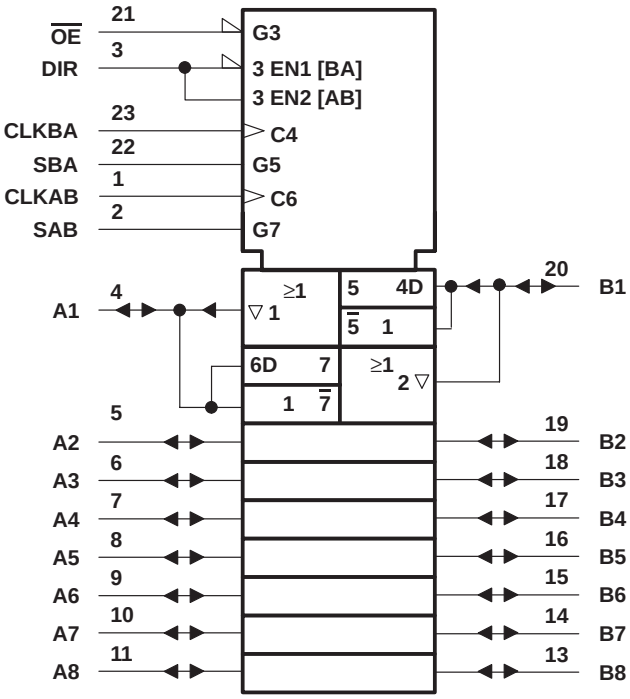
Pin numbers shown are for DB, DW, JT, NT, and PW packages.

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

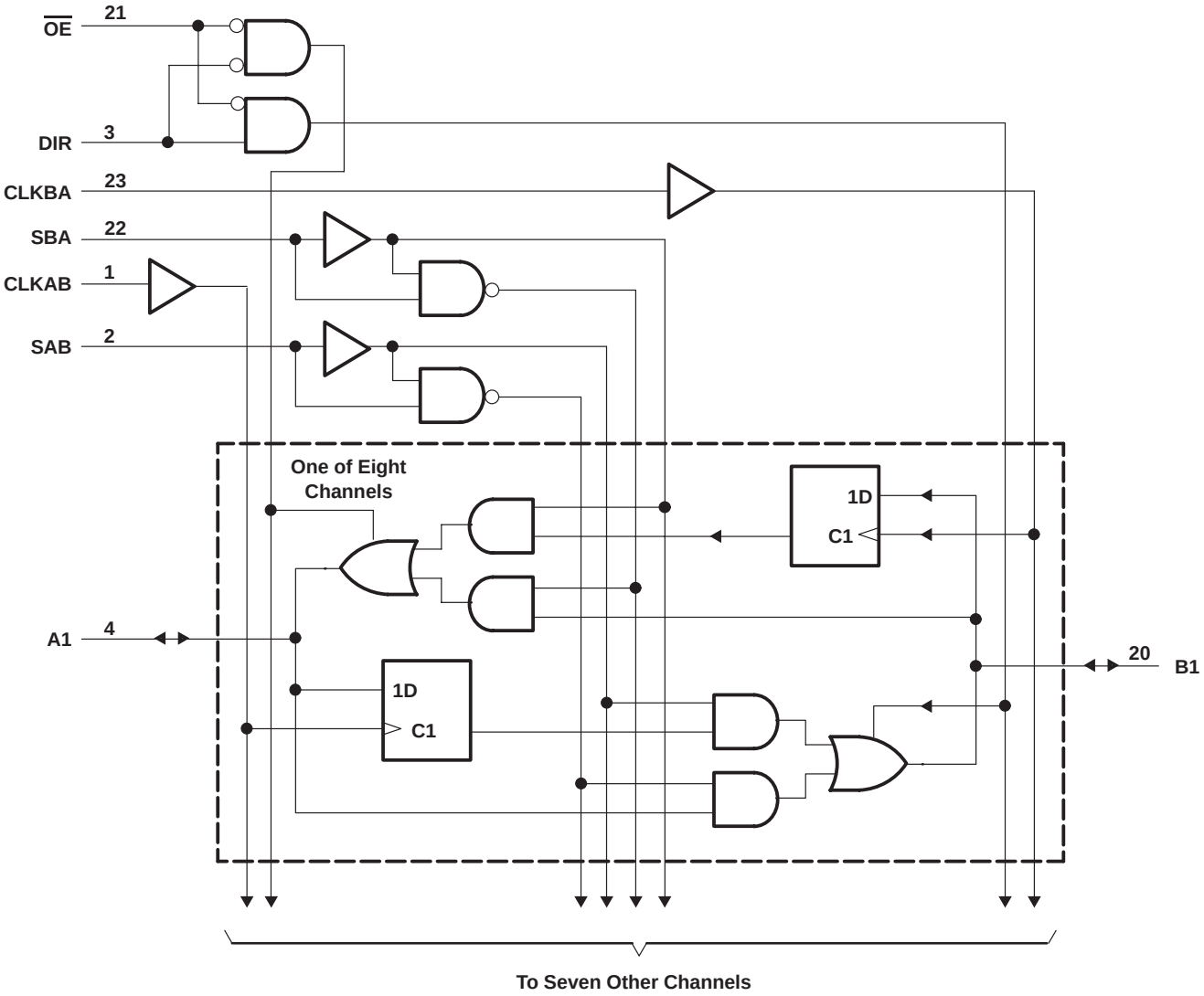
† The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT646 . . . . . 96 mA
SN74ABT646 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . . 0.65 W
DW package . . . . . 1.7 W
NT package . . . . . 1.3 W
PW package . . . . . 0.7 W
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

		SN54ABT646		SN74ABT646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT646		SN74ABT646		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = –3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = –24 mA		2			2				
		I_{OH} = –32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		Control inputs			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				10§		50		10§	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–10§		–50		–10§	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–100	–180	–50	–180	–50	–180	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			250		250		250	µA
			Outputs low			30		30		30	mA
			Outputs disabled			250		250		250	µA
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		7						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		12						pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ This data sheet limit may vary among suppliers.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

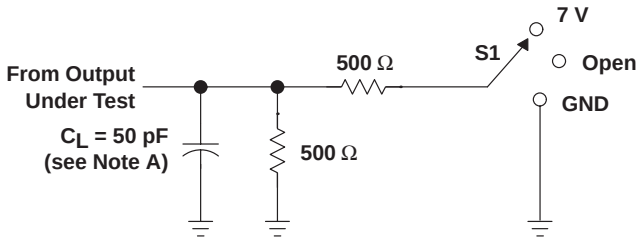
			V_{CC} = 5 V, T_A = 25°C		SN54ABT646		SN74ABT646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	125	0	125	0	125	MHz
t_w	Pulse duration, CLK high or low		4		4		4		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	High	3.5		3.5		3.5		ns
		Low	3		3		3		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑		0		0		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT646		SN74ABT646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			125					125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	6.8			2.2	7.8	ns
t_{PHL}			1.7	4	7.4			1.7	8.4	
t_{PLH}	A or B	B or A	1.5	3	5.9			1.5	6.9	ns
t_{PHL}			1.5	3.3	5.9			1.5	6.9	
t_{PLH}	SAB or SBA†	B or A	1.5	4	6.1			1.5	7.1	ns
t_{PHL}			1.5	3.6	6.9			1.5	7.9	
t_{PZH}	$\overline{OE}$	A or B	1	4.3	5.3			1	6.3	ns
t_{PZL}			2.1	5.8	7.4			2.1	8.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	3.5	7.3			1.5	8.3	ns
t_{PLZ}			1.5	3	7			1.5	7.5	
t_{PZH}	DIR	A or B	1.2	4.5	5.7			1.2	6.7	ns
t_{PZL}			2.5	6.5	9			2.5	9.5	
t_{PHZ}	DIR	A or B	1.5	3.8	6.7			1.5	7.7	ns
t_{PLZ}			1.5	3.8	7.2			1.5	8.2	

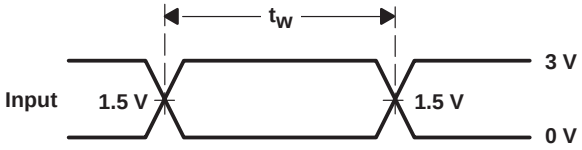
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

PARAMETER MEASUREMENT INFORMATION

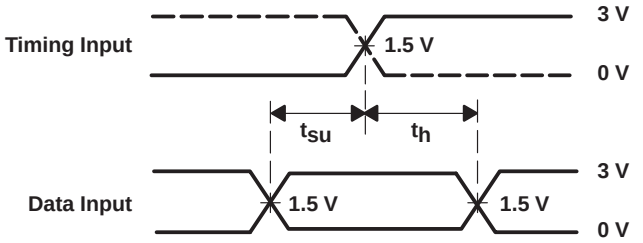


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

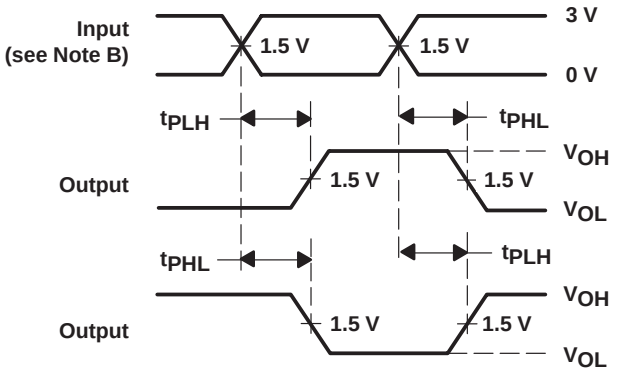
LOAD CIRCUIT FOR OUTPUTS



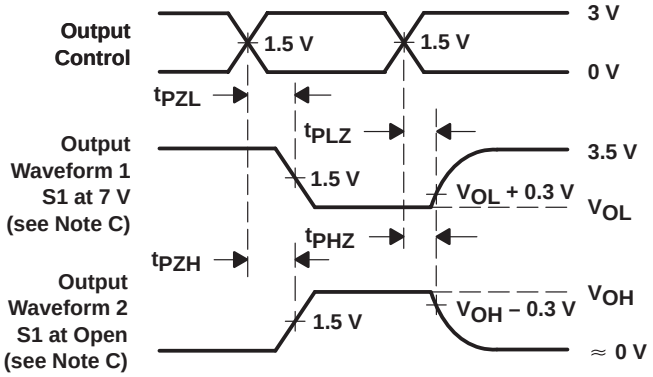
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

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SN74ABT646, Octal Bus Transceivers And Registers With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74ABT646
Voltage Nodes (V)	5

FEATURES

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DESCRIPTION

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These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the ´ABT646.

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Product Folder: SN74ABT646, Octal Bus Transceivers And Registers With 3-State Outputs

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74abt646.pdf (156 KB,Rev.E) (Updated: 07/01/1994)

APPLICATION NOTES

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View Application Notes for Digital Logic

- Advanced BiCMOS Technology (ABT) Logic Characterization Information (Rev. B) (SCBA008B - Updated: 06/01/1997)
- Advanced BiCMOS Technology (ABT) Logic Enables Optimal System Design (Rev. A) (SCBA001A - Updated: 03/01/1997)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices (Rev. A) (SCBA006A - Updated: 12/01/1996)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. C) (SCBA017C - Updated: 11/22/2002)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74ABT646DBR	SSOP (DB)	24	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT646DGVR	TVSOP (DGV)	24	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT646DW	SOIC (DW)	24	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT646NT	PDIP (NT)	24	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74ABT646PWR	TSSOP (PW)	24	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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Product Folder: SN74ABT646, Octal Bus Transceivers And Registers With 3-State Outputs

DEVICE INFORMATION (Updated Daily)							TI INVENTORY STATUS (As Of 09:00 AM GMT, 17 Apr 2003)			REPORTED DISTRIBUTOR INVENTORY (As Of 09:00 AM GMT, 17 Apr 2003)		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME	DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
SN74ABT646DBLE	OBSOLETE	SSOP (DB) | 24	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors		
SN74ABT646DBR	ACTIVE	SSOP (DB) | 24	-40 TO 85	View Contents	1KU | 3.30	2000	0*	>10k | 12 May	4 WKS	DigiKey | Americas	>1k	BUY NOW
SN74ABT646DGVR	ACTIVE	TVSOP (DGV) | 24	-40 TO 85	View Contents	1KU | 3.30	2000	0*	3606 | 01 May	4 WKS	DigiKey | Americas	>1k	BUY NOW
								>10k | 08 May				
SN74ABT646DW	ACTIVE	SOIC (DW) | 24	-40 TO 85	View Contents	1KU | 3.30	25	2975*	11 | 21 Apr	4 WKS	DigiKey | Americas	286	BUY NOW
								>10k | 12 May		Insight | Americas	125	BUY NOW
SN74ABT646DWR	ACTIVE	SOIC (DW) | 24	-40 TO 85	View Contents	1KU | 3.34	2000	0*	>10k | 12 May	4 WKS	None Reported View Distributors		
SN74ABT646NT	ACTIVE	PDIP (NT) | 24	-40 TO 85	View Contents	1KU | 3.30	15	0*	660 | 30 Apr	4 WKS	DigiKey | Americas	219	BUY NOW
								3733 | 02 May		Arrow | Americas	126	BUY NOW
								>10k | 12 May		Newark Electronics | Americas	25	BUY NOW
										Avnet | Americas	5	BUY NOW
SN74ABT646PW	ACTIVE	TSSOP (PW) | 24	-40 TO 85	View Contents	1KU | 2.10	60	0*	3847 | 01 May	4 WKS	None Reported View Distributors		
								>10k | 08 May				
SN74ABT646PWLE	OBSOLETE	TSSOP (PW) | 24	-40 TO 85	View Contents	1KU |		0*		Call**	None Reported View Distributors		
SN74ABT646PWR	ACTIVE	TSSOP (PW) | 24	-40 TO 85	View Contents	1KU | 3.30	2000	0*	>10k | 08 May	4 WKS	DigiKey | Americas	>1k	BUY NOW

Table Data Updated on: 4/17/2003