THIS SPEC IS OBSOLETE

Spec No: 38-07333

Spec Title: CY22K7 133-MHz Spread Spectrum Clock Generator For Use With the AMD-K7® Processor and AMD-750 Chipset

Sunset Owner: Rose Galindez (RGL)

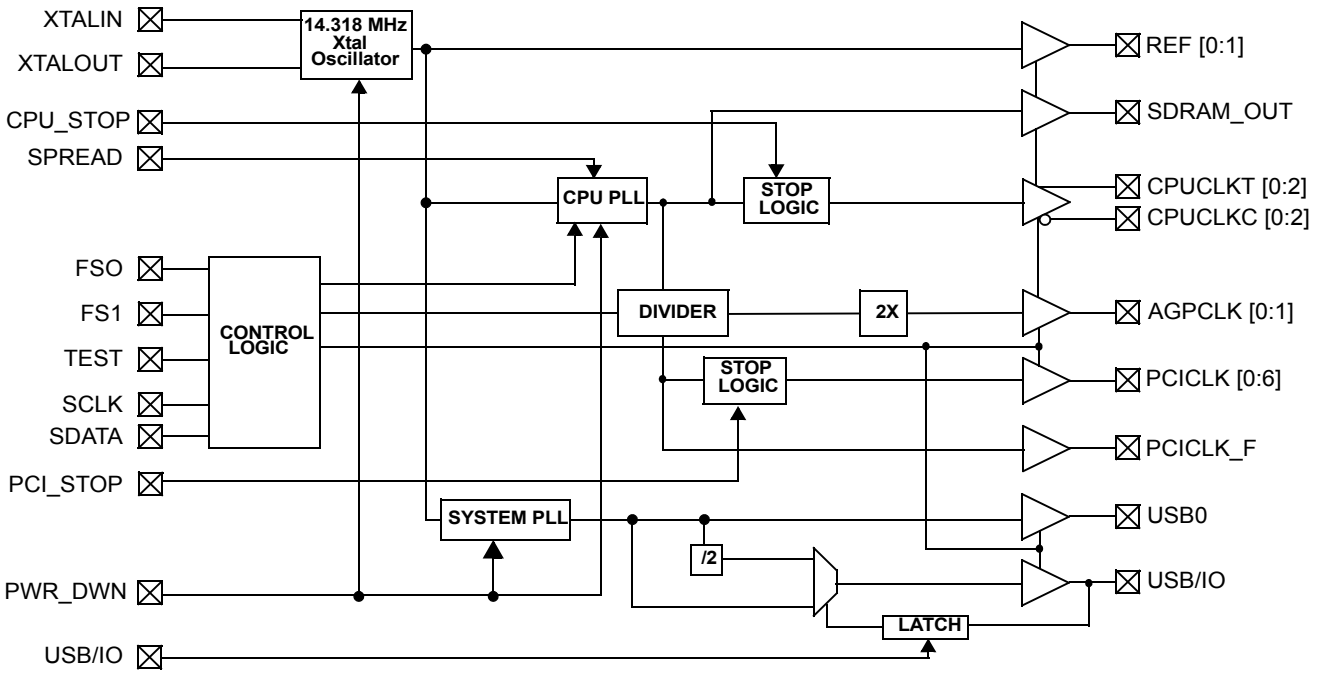
Replaced by: None

CY22K7

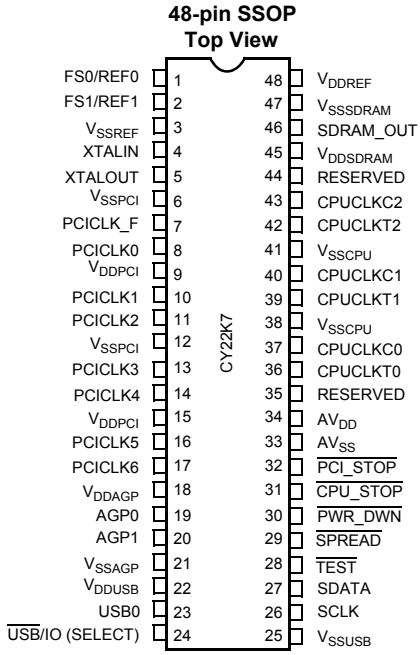
133-MHz Spread Spectrum Clock Generator For Use With the AMD-K7® Processor and AMD-750 Chipset

Features	Benefits
• **Multiple output clocks running at different frequencies** — **Three open-drain differential CPU outputs running up to 133 MHz** — **Eight 3.3V synchronous PCI clocks (one free running)** — **Two 3.3V AGP clocks at 2xPCI** — **One dedicated 3.3V USB clock at 48 MHz** — **One 3.3V USB/IO clock at 48 MHz or 24 MHz, selectable via power-on latch input** — **One 3.3V SDRAM clock output running at the CPU frequency** — **Two 3.3V Reference clocks at 14.318 MHz**	Main clock generator for PC motherboard designs using the AMD-K7® processor and AMD-750 Chipset — Supports up to two CPUs and chipset — Support for 4 PCI slots and chipset — Supports designs using AGP — Supports designs using USB — Allows for one additional USB output or support for I/O chip from various vendors — Supports SDRAM memory architecture with external PLL buffer — Supports ISA slots and I/O chip
• **Spread Spectrum clocking** — **33 kHz modulation frequency** — **–0.6% downspread margin**	EMI reduction
• **Dedicated inputs for various functions** — **$\overline{\text{PCI\_STOP}}$** — **$\overline{\text{CPU\_STOP}}$** — **$\overline{\text{PWR\_DWN}}$** — **SPREAD** — **$\overline{\text{TEST}}$** — **USB/IO** — **FS [0:1]**	Provides system design flexibility and power management — Stops all PCI clocks (except PCICLK_F0) when LOW — Stops all CPU clocks when LOW — Power is removed from internal logic when LOW — Activates Spread Spectrum for lower EMI — Used to enter Test Mode — Selects USB or SuperIO Clock — Power-on latched inputs for frequency select options
• **Serial Programming Interface**	Dynamic control of output clock signals via SMBus
• **48-Pin SSOP package**	Industry-standard package provides cost and space savings

Logic Block Diagram



Pin Configuration



Pin Summary[1]

Pin Number	Pin Name	Type	Description
34	AV_{DD}	PWR	Isolated power for core
33	AV_{SS}	PWR	Isolated ground for core
48	V_{DDREF}	PWR	Power for REF[0:1], XTALIN, XTALOUT
3	V_{SSREF}	PWR	Ground for REF[0:1] outputs
1, 2	FS[0:1]/REF[0:1]	IN/OUT	Frequency select input at power-on/14.318-MHz output
4	XTALIN[2]	IN	14.318-MHz reference crystal input
5	XTALOUT	OUT	14.318-MHz reference crystal feedback
9, 15	V_{DDPCI}	PWR	Power for PCICLK outputs
6, 12	V_{SSPCI}	PWR	Ground for PCICLK outputs
7	PCICLK_F	OUT	Free running PCI output
8, 10, 11, 13, 14, 16, 17	PCICLK[0:6]	OUT	PCI clock outputs, TTL compatible 3.3V
18	V_{DDAGP}	PWR	Power for AGP outputs
21	V_{SSAGP}	PWR	Ground for AGP outputs
19, 20	AGP[0:1]	OUT	AGP clock outputs
22	V_{DDUSB}	PWR	Power for USB outputs
25	V_{SSUSB}	PWR	Ground for USB outputs
23	USB0	OUT	USB clock output
24	$\overline{USB}$/IO (SELECT)	IN/OUT	USB or Super I/O output selected at power-on by latched input resistor: LOW = 48 MHz, HIGH = 24 MHz
26	SCLK	IN/OUT	SMBus Clock
27	SDATA	IN/OUT	SMBus Data
28	$\overline{TEST}$	IN	Three-state or Test Mode when LOW

Pin Summary[1] (continued)

Pin Number	Pin Name	Type	Description
29	$\overline{\text{SPREAD}}$	IN	Enables spread spectrum when LOW
30	$\overline{\text{PWR\_DWN}}$[3]	IN	Power-down when LOW, removes power from internal logic
31	$\overline{\text{CPU\_STOP}}$	IN	Stops CPU clocks when LOW
32	$\overline{\text{PCI\_STOP}}$[2]	IN	Stops PCI clocks when LOW
45	$V_{DDSDRAM}$	PWR	Power for SDRAM_OUT
47	$V_{SSSDRAM}$	PWR	Ground for SDRAM_OUT
46	SDRAM_OUT	OUT	CPU reference clock for SDRAM zero delay buffer
38, 41	V_{SSCPU}	PWR	Ground for CPU outputs shorted to SDRAM ground
36, 39, 42	CPUCLKT[0:2]	OUT	“True” clocks of differential pair for CPU and host clock outputs
37, 40, 43	CPUCLKC[0:2]	OUT	“Complementary” clocks of differential pair for CPU and host clock outputs
35, 44	RESERVED	–	Reserved for future CPU power rail

Function Table

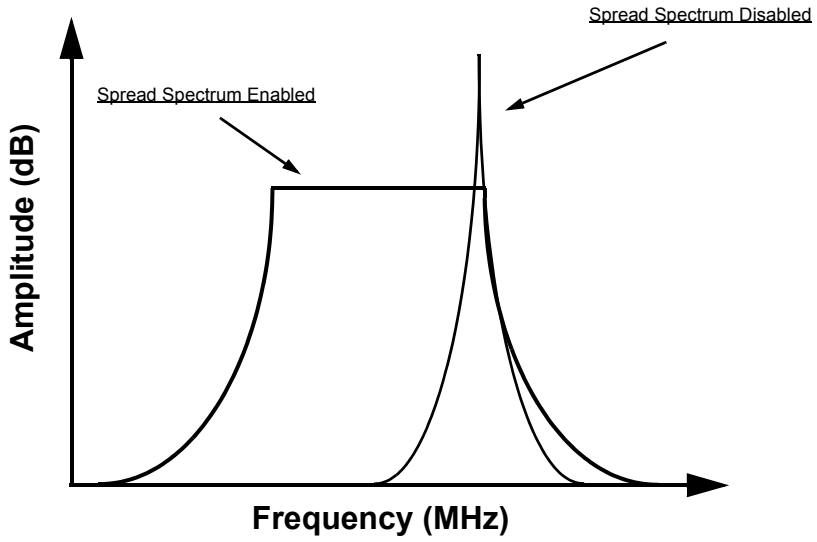
$\overline{\text{TEST}}$	FS1	FS0	CPUCLK SDRAM_OUT	PCICLK PCICLK_F	AGP	USB/IO	REF
0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	0	1	50	25	50	48/24	14.318
0	1	0	66	33	66	48/24	14.318
0	1	1	TCLK/2	TCLK/6	TCLK/3	TCLK/4[4]	TCLK
1	0	0	90	30	60	48/24	14.318
1	0	1	133	33.3	66.6	48/24	14.318
1	1	0	120	30	60	48/24	14.318
1	1	1	100	33.3	66.6	48/24	14.318

Power Management Modes

$\overline{\text{PWR\_DWN}}$	$\overline{\text{CPU\_STOP}}$	$\overline{\text{PCI\_STOP}}$	CPU+	CPU-	PCICLK	PCICLK_F	Other Clocks	Oscillator	PLLs
0	X	X	Low	High	Low	Low	Low	Off	Off
1	0	0	Low	High	Low	Running	Running	Running	Running
1	0	1	Low	High	Running	Running	Running	Running	Running
1	1	0	Running	Running	Low	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running	Running	Running

Notes:
1. All control pins have internal pull-ups of 56K including: USB/IO, TEST, SPREAD, PWR_DWN, CPU_STOP, PCI_STOP.
2. Part will go into test mode if three rising edges come on PCI_STOP while XTALIN is held LOW.
3. Part will consume more shutdown current if external pull-ups are connected on latched input/outputs during power-down.
4. TCLK/4 if Select = 0; TCLK/8 if Select = 1.

Spread Spectrum Clocking



Description	Output	Min	Max	Unit
Modulation Frequency	CPUCLK, PCICLK, SDRAM_OUT, AGPCLK	30.0	33.0	kHz
Downspread margin at the fundamental frequency	CPUCLK, PCICLK, SDRAM_OUT, AGPCLK	0.0	–0.6	%

Serial Configuration Map

- The Serial bits will be read by the clock driver in the following order:

  Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

  Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- SPI Address for the CY22K7 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	–

Bytes 0 to 3 will be ignored.

Byte 4: Clock Control Register (1 = Active, 0 = Inactive)

Bit	Pin #	Default	Description
7	1	Active	REF0
6	24	Active	$\overline{\text{USB}}$/IO
5	23	Active	USB0
4	20	Active	AGP1
3	19	Active	AGP0
2	42, 43	Active	CPUCLK2 (both of differential pair, “True” and “Complementary”)
1	39, 40	Active	CPUCLK1 (both of differential pair, “True” and “Complementary”)
0	36, 37	Active	CPUCLK0 (both of differential pair, “True” and “Complementary”)

Byte 5: PCI/REF Clock Control Register (1 = Active, 0 = Inactive)

Bit	Pin #	Default	Description
7	2	Active	REF1
6	17	Active	PCICLK6
5	16	Active	PCICLK5
4	14	Active	PCICLK4
3	13	Active	PCICLK3
2	11	Active	PCICLK2
1	10	Active	PCICLK1
0	8	Active	PCICLK0

Byte 6: SDRAM Clock & Generator Mode Control Register (1 = Active, 0 = Inactive)

Bit	Pin #	Default	Description
7	–	Inactive	Spread Spectrum
6	–	Active	Bits[6:4] correspond to the Function Table on page 3 Bit 6 = $\overline{\text{TEST}}$, Bit 5 = FS1, Bit 4 = FS0 example: Bits[6:4] = ‘111’ -- 100-MHz CPUCLK and SDRAM_OUT clocks
5	–	Active	
4	–	Active	
3	–	Active	Reserved
2	–	Active	Reserved
1	–	Inactive	SPI (directs the generator to utilize either SPI feature selection if bit is enabled or pin-based feature if bit is disabled)
0	46	Active	SDRAM_OUT

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... – 0.5 to +4.0V

Input Voltage ..... – 0.5V to V_{DD} + 0.5

Storage Temperature (Non-Condensing) .. – 65°C to +150°C

Junction Temperature ..... +150°C

Package Power Dissipation 0.7W

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2000V

CY22K7 DC Operating Conditions Over which the DC Characteristics are Guaranteed

Parameter	Description	Min.	Max.	Unit
V_{DD}	3.3V Power Supply Voltages	3.135	3.465	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Maximum Capacitive Load on SDRAM_OUT PCICLK PCICLK_F AGPCLK USB, REF		 30 30 30 30 20	pF
f_{REF}	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Pads. Threshold voltage for crystal pads = $V_{DD}/2$		2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Pads			0.8	V
I_{IH}	Input High Current	$0 \le V_{IN} \le V_{DD}$			10	µA
I_{IL}	Input Low Current	$0 \le V_{IN} \le V_{DD}$			50	µA
I_{OH}	High-level Output Current	SDRAM_OUT	V_{OUT} = 2.0V		–19	mA
		PCICLK	V_{OUT} = 2.0V		–26	
		PCICLK_F	V_{OUT} = 2.0V		–19	
		AGPCLK	V_{OUT} = 2.0V		–26	
		USB, USB/IO, REF	V_{OUT} = 2.0V		–22	
I_{OL}	Low-level Output Current	CPUCLK	V_{OUT} = 0.3V	16		mA
		SDRAM_OUT	V_{OUT} = 0.8V	12		
		PCICLK	V_{OUT} = 0.8V	19		
		PCICLK_F	V_{OUT} = 0.8V	12		
		AGPCLK	V_{OUT} = 0.8V	19		
		USB, $\overline{USB}$/IO, REF	V_{OUT} = 0.8V	16		
I_{OZ}	Output Leakage Current	Three-state			10	µA
I_{DD}	3.3V Power Supply Current	V_{DD} = 3.465V, F_{CPU} = 133 MHz			175	mA
I_{DDPD}	3.3V Shutdown Current	V_{DD} = 3.465V			200	µA
VIHS	SMBus Input High Level			0.7		V
VILS	SMBus Input Low Level				0.3	V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit

CY22K7 CPUCLK Driver Characteristics (Open Drain)[7]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DIF}	Differential Voltage	See Note 5	0.4		V_{pullup} (External) + 0.6	V
Vx	Differential Crossover Voltage	V_{pullup} is to 1.5V	550	750	950	mV
V_X	Differential Crossover Voltage	V_{pullup} (External) = 1.4 to 1.9V Min. = (V_{pullup} (External)/2) – 150 mV Max. = (V_{pullup} (External)/2) + 150 mV	550	750	1100	mV

CY22K7 Switching Characteristics[6, 7] Over the Operating Range @ 100 MHz

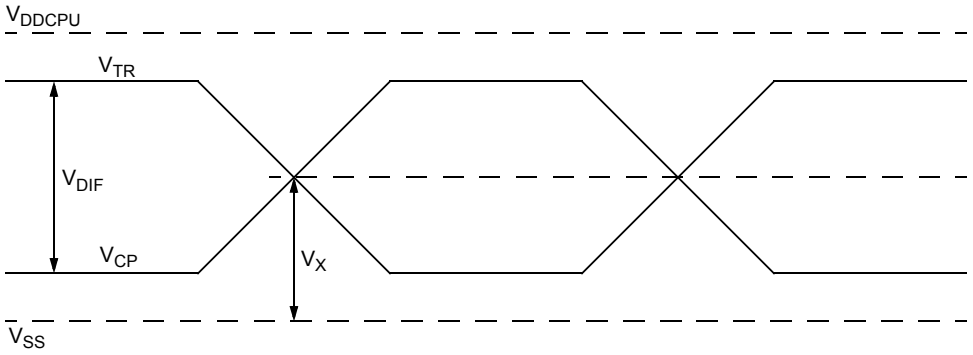
Parameter	Output	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_1	All	Output Duty Cycle	t_{1A}/t_{1B}[8]	45		55	%
t_2	CPU	Rising Edge Rate	At Output of CY22K7 CPU±		1.0		V/ns
t_2	CPU	Rising Edge Rate	As measured at Observation Point in *Figure 1*		0.4		V/ns
t_2	PCI	Rise Time	Between 0.4V and 2.4V			2.0	ns
t_2	SDRAM_OUT	Rise Time	Between 0.4V and 2.4V			2.0	ns
t_2	AGP	Rise Time	Between 0.4V and 2.4V	0.4		2.0	ns
t_2	USB, REF	Rise Time	Between 0.4V and 2.4V			4.0	ns
t_3	CPU	Falling Edge Rate	At Output of CY22K7 CPU±		1.0		V/ns
t_3	CPU	Falling Edge Rate	As measured at Observation Point in *Figure 1*		0.4		V/ns
t_3	PCI	Fall Time	Between 2.4V and 0.4V			2.0	ns
t_3	SDRAM_OUT	Fall Time	Between 2.4V and 0.4V			2.0	ns
t_3	AGP	Fall Time	Between 2.4V and 0.4V	0.4		2.0	ns
t_3	USB, REF	Fall Time	Between 2.4V and 0.4V			4.0	ns
t_4	CPU, PCI	CPU-PCI Offset	Load shown in *Figure 1 & Figure 2*		500	700	ps
t_4	CPU, SDRAM	CPU-SDRAM Skew	Load shown in *Figure 1 & Figure 2*		500	700	ps
t_4	CPU, AGP	CPU-AGP Skew	Load shown in *Figure 1 & Figure 2*			1000	ps
t_4	CPU, CPU	CPU-CPU Skew	Load shown in *Figure 1*			250	ps
t_4	PCI, PCI	PCI-PCI Skew	Load shown in *Figure 2*			500	ps
t_5	CPU	Cycle-Cycle Clock Jitter	Measured at V_X, t_{5A}–t_{5B}			250	ps

Notes:

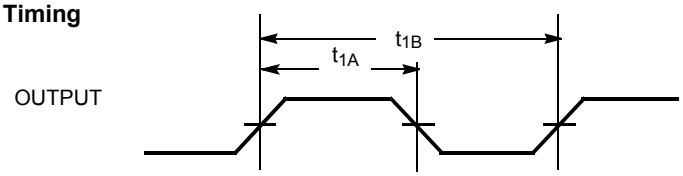
5. V_{DIF} specifies the minimum input differential voltages ($V_{TR} – V_{CP}$) required for switching, where V_{TR} is the 'true' input level and V_{CP} is the 'complement' input level.
6. All parameters specified with loaded outputs.
7. All parameters for CPU are measured at observation point shown in *Figure 1* on page 10 and parameters for PCI, SDRAM & AGP are measured at observation point shown in *Figure 2* on page 11 unless otherwise mentioned.
8. For 133-MHz Output Duty Cycle will be guaranteed at 40% Min., 60% Max.

Switching Waveforms

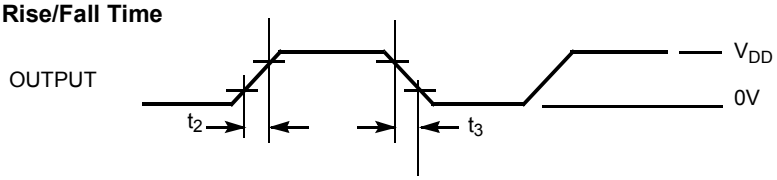
Differential Clock Parameters



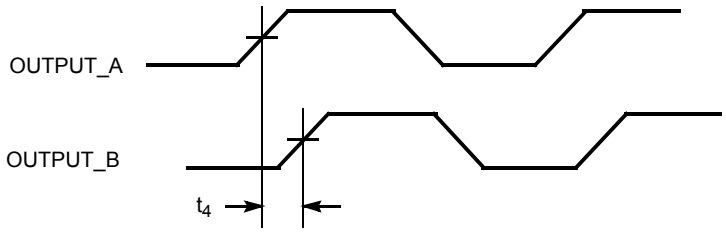
Duty Cycle Timing



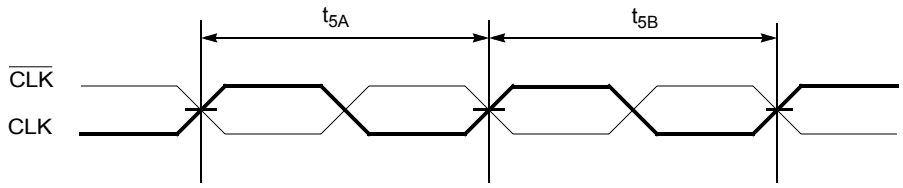
All Outputs Rise/Fall Time



Output_A-Output_B Clock Skew

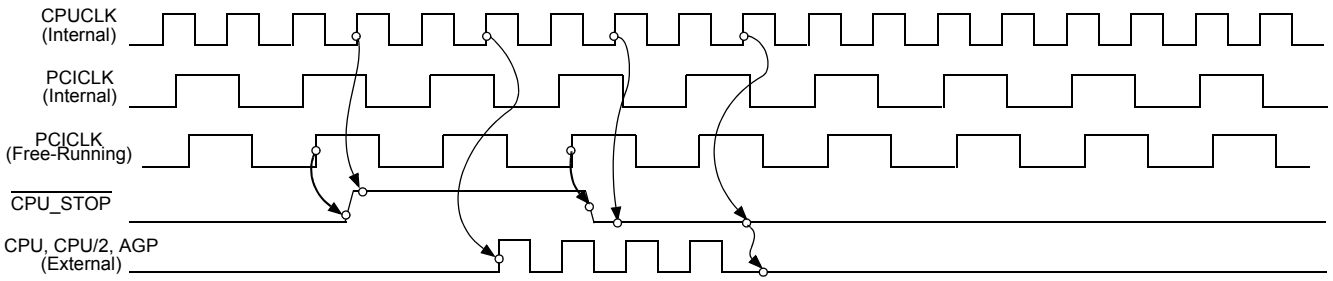


Cycle-Cycle Clock Jitter

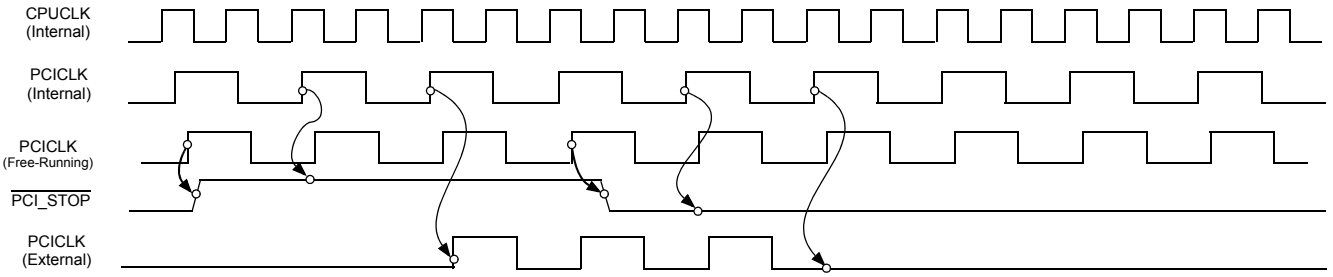


Switching Waveforms (continued)

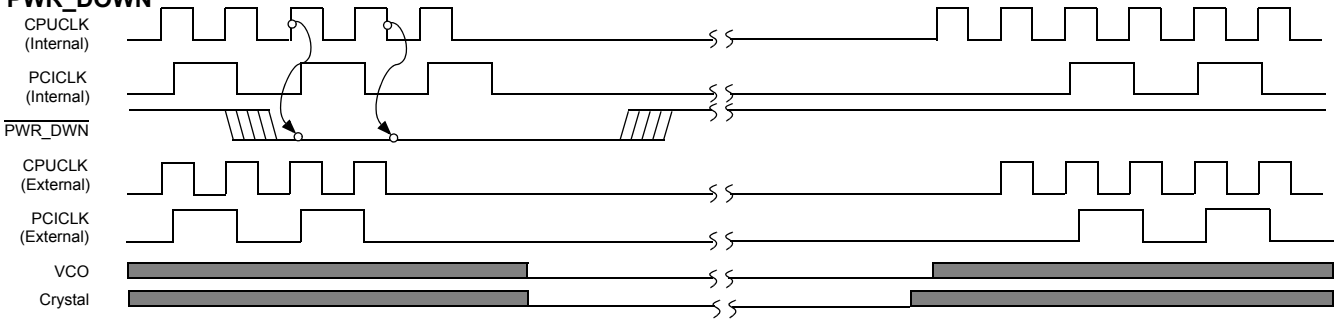
CPU_STOP Timing[9,10]



PCI_STOP



PWR_DOWN [11]



Shaded section on the VCO and Crystal waveforms indicates that the VCO and crystal oscillator are active, and there is a valid clock.

Notes:

9. CPUCLK on and CPUCLK off latency is 2 or 3 CPUCLK cycles.
10. CPU_STOP may be applied asynchronously. It is synchronized internally.
11. USB, USB/IO, REF are not synchronized when entering/leaving power-down.

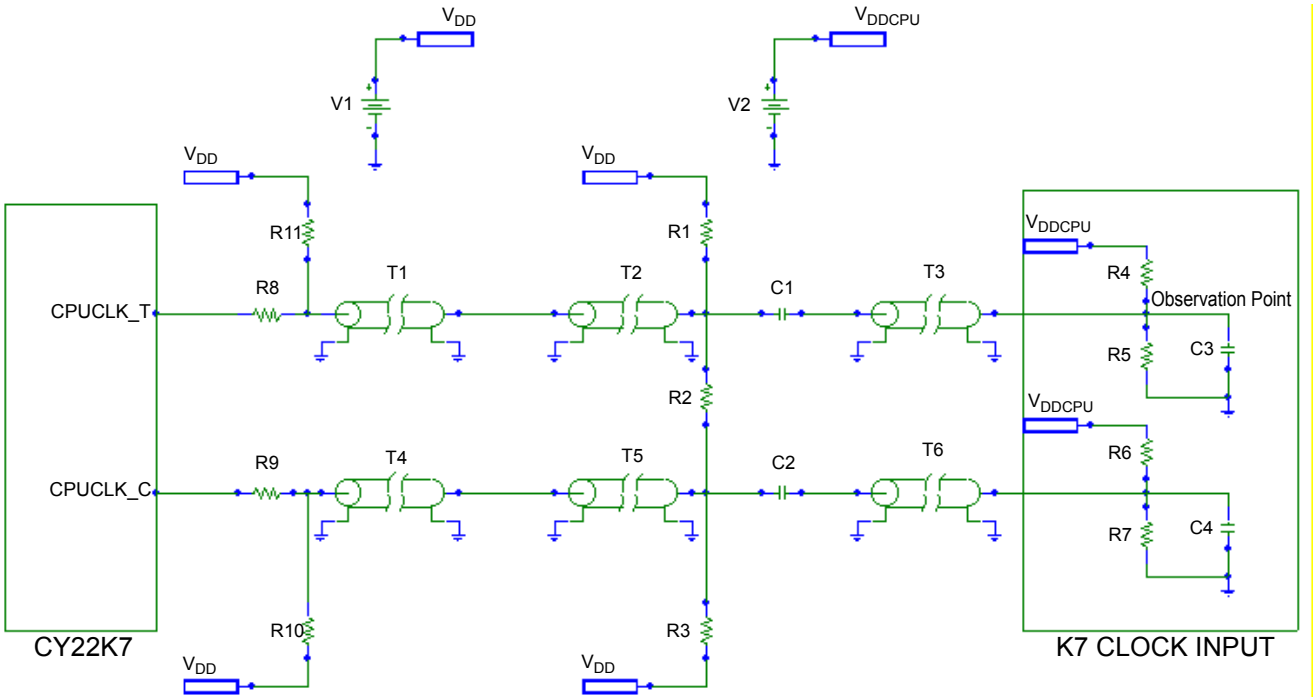


Figure 1. AMD CPU Load Circuit

Component Values

Symbol	Value
V1	3.3V
V2	1.5V
R1,3	95Ω
R2	360Ω
R4,5,6,7	500Ω
R8,9	50Ω
R10,11	150Ω
C1,2	680 pF
C3,4	20 pF
T1,4	Z_0 = 50Ω
	length = 5”
T2,5	Z_0 = 50Ω
	length = 3”
T3,6	Z_0 = 50Ω
	length = 1”

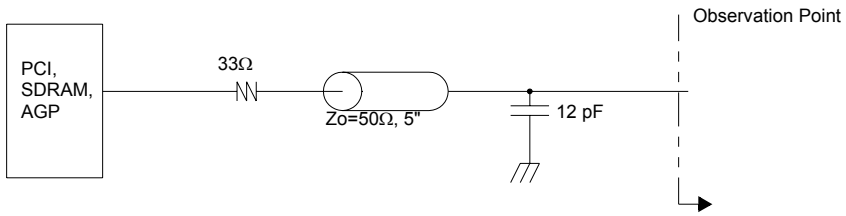


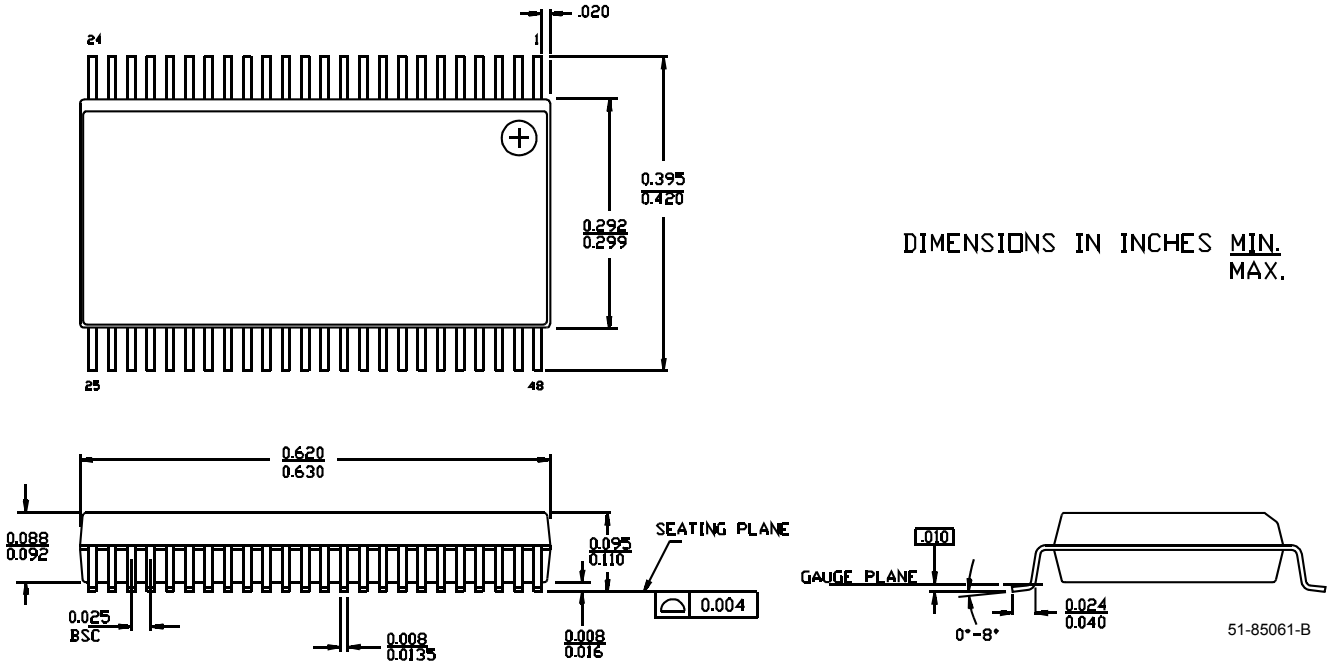
Figure 2. Test Circuit for PCI/SDRAM/AGP

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY22K7PVC-1	O48	48-pin SSOP	Commercial

Package Diagram

48-Lead Shrunk Small Outline Package O48



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Revision History

Document Title: CY22K7 133-MHz Spread Spectrum Clock Generator For Use With the AMD-K7® Processor and AMD-750 Chipset Document Number: 38-07333				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111732	12/16/01	DSG	Change from Spec number: 38-00745 to 38-07333
*A	121856	12/14/02	RBI	Power up requirements added to Operating Conditions Information
OBS	294235	See ECN	RGL	To Obsolete the DS