FAIRCHILD
SEMICONDUCTOR™

October 1998
PRELIMINARY

FDS8433A

Single P-Channel 2.5V Specified MOSFET

General Description

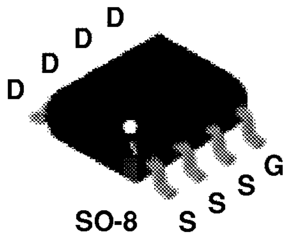
This P-Channel enhancement mode power field effect transistors is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density processis especially tailored to minimize on-state resistance and provide superior switching performance.

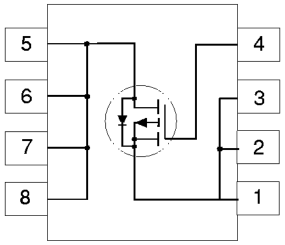
Applications

- Load switch
- DC/DC converter
- Battery protection

Features

- -5 A, -20 V. $R_{DS(on)} = 0.045\ \Omega$ @ $V_{GS} = -4.5$ V
  $R_{DS(on)} = 0.070\ \Omega$ @ $V_{GS} = -2.5$ V
- Fast switching speed.
- High density cell design for extremely low $R_{DS(on)}$.
- High power and current handling capability.





Absolute Maximum Ratings

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter		FDS8433A	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current - Continuous	(Note 1a)	-5	A
	- Pulsed		-50	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS8433A	FDS8433A	13"	12mm	2500 units

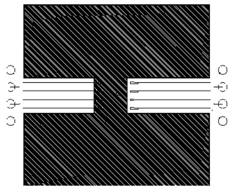
DMOS Electrical Characteristics

T_A = 25°C unless otherwise noted

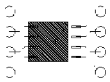
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-20			V
$\frac{BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		-25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -5 A V_{GS} = -4.5 V, I_D = -5 A, T_J=125°C V_{GS} = -2.5 V, I_D = -4.3 A		0.036 0.050 0.047	0.045 0.085 0.070	Ω Ω Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-25			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -5 A		16		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1130		pF
C_{oss}	Output Capacitance			480		pF
C_{rss}	Reverse Transfer Capacitance			120		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		8	16	ns
t_r	Turn-On Rise Time			23	37	ns
$t_{d(off)}$	Turn-Off Delay Time			260	360	ns
t_f	Turn-Off Fall Time			90	125	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -5 A, V_{GS} = -5 V,		20	28	nC
Q_{gs}	Gate-Source Charge			2.8		nC
Q_{gd}	Gate-Drain Charge			3.2		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		-0.8	-1.2	V

Notes:

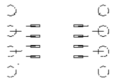
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 50° C/W when mounted on a 1 in^2 pad of 2 oz. copper.



b) 105° C/W when mounted on a 0.04 in^2 pad of 2 oz. copper.



c) 125° C/W when mounted on a 0.006 in^2 pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

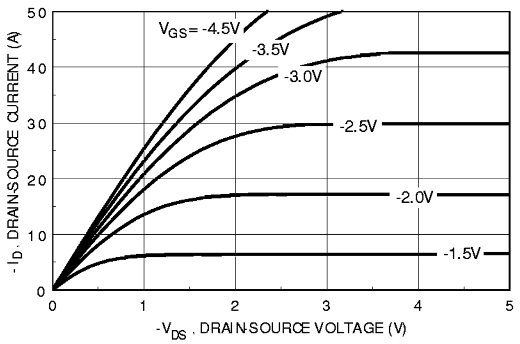


Figure 1. On-Region Characteristics.

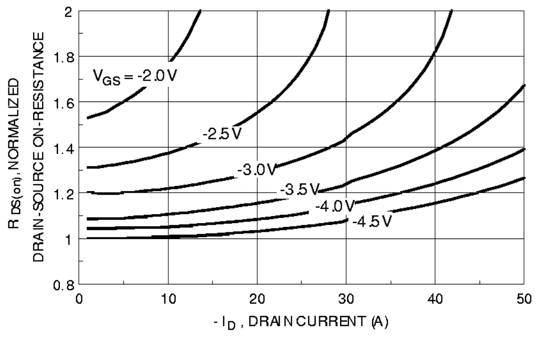


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

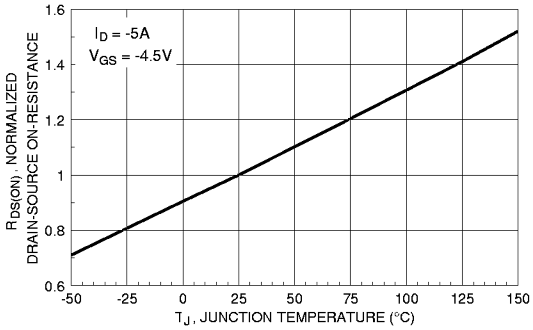


Figure 3. On-Resistance Variation with Temperature.

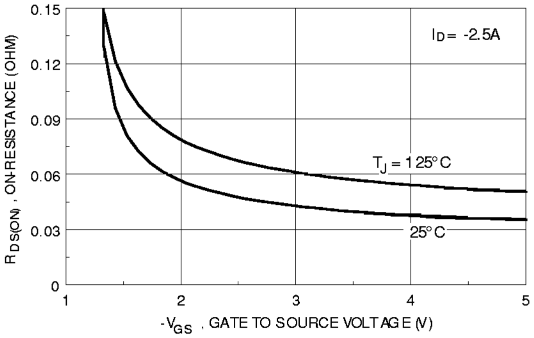


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

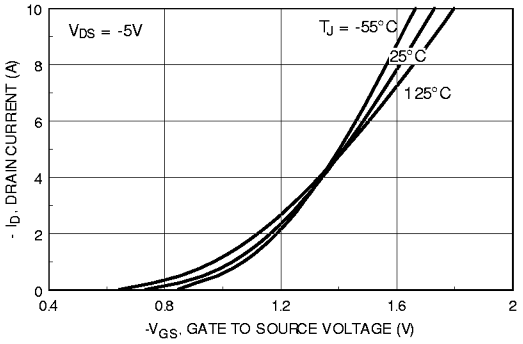


Figure 5. Transfer Characteristics.

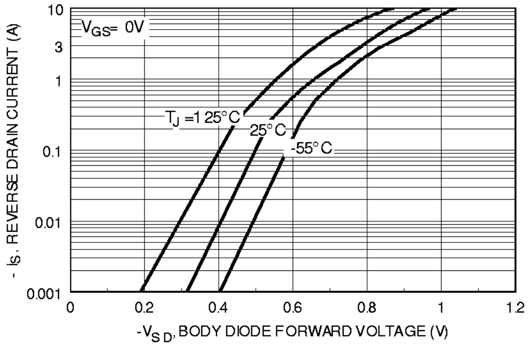


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

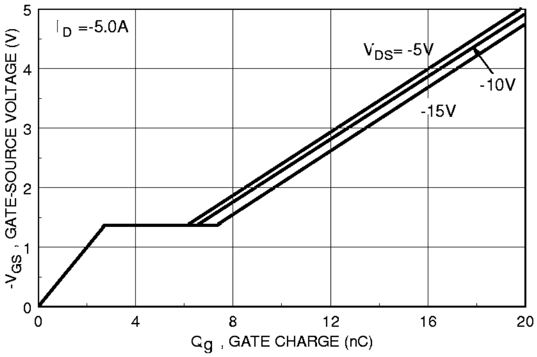


Figure 7. Gate-Charge Characteristics.

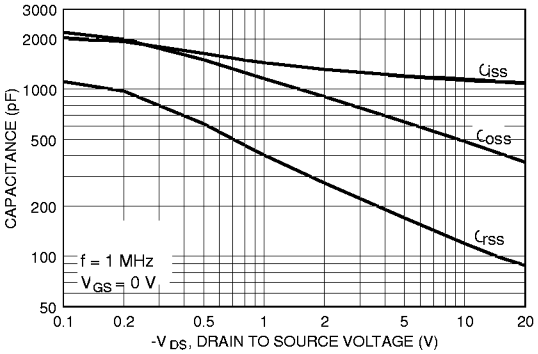


Figure 8. Capacitance Characteristics.

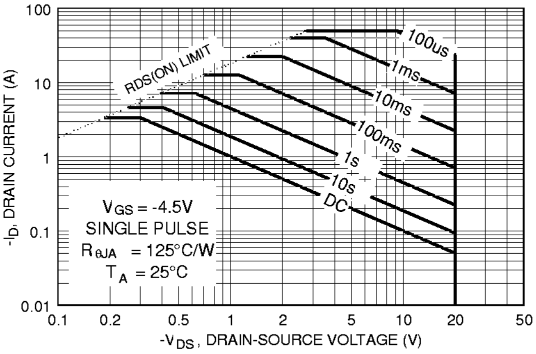


Figure 9. Maximum Safe Operating Area.

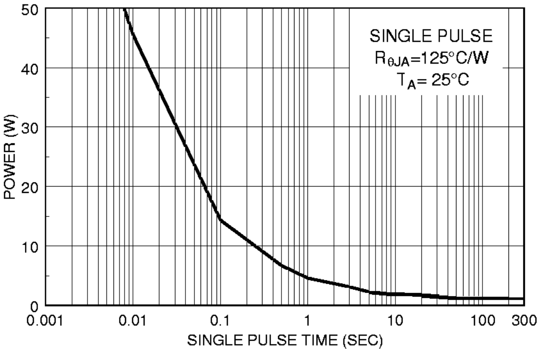


Figure 10. Single Pulse Maximum Power Dissipation.

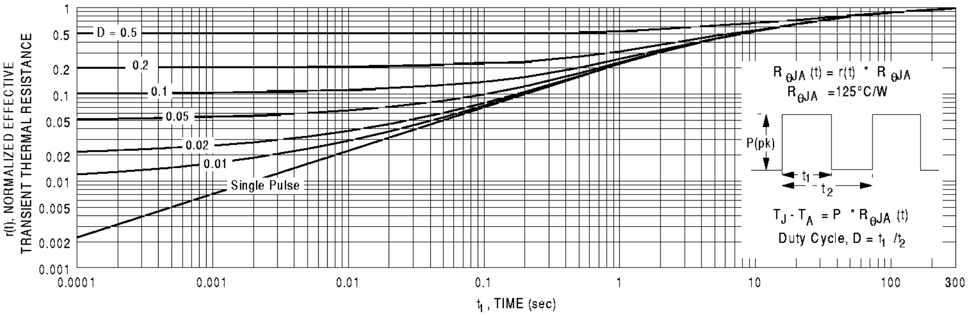


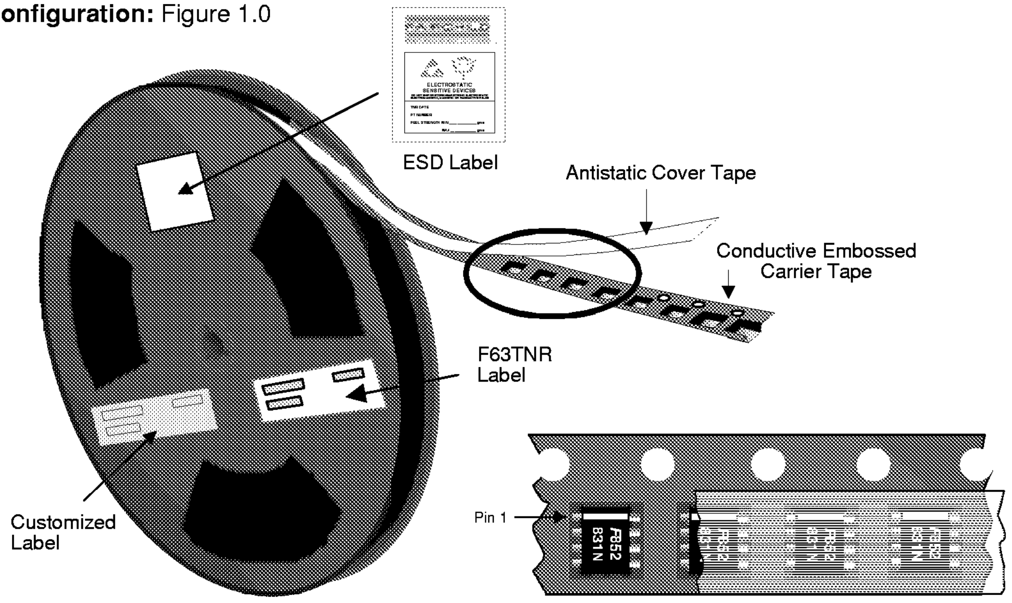
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1.
Transient themal response will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions

SOIC(8lds) Packaging

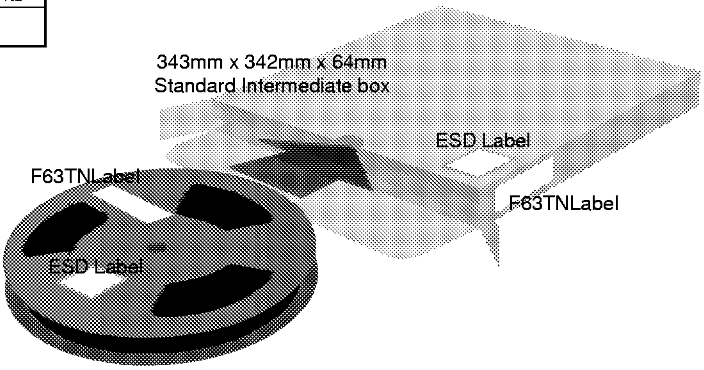
Configuration: Figure 1.0



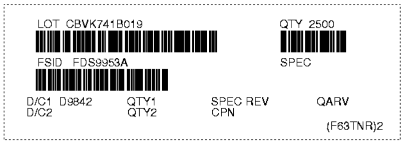
SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information

Packaging Option	Standard (no flow code)	L86Z	S62Z	D84Z
Packaging type	TNR	Rail/Tube	Bag	TNR
Qty per Reel/Tube/Bag	2,500	95	200	500
Reel Size	13" Dia	-	-	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	76x102x127	184x187x47
Max qty per Box	5,000	30,000	1,000	2,500
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	-	0.1182
Note/Comments			Bulk	



F63TNR Label sample



LOT CBVK741B019 QTY 2500

FSID FDS9953A SPEC

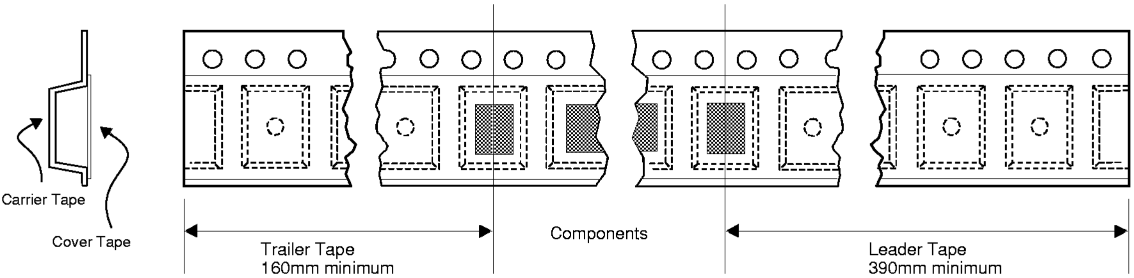
D/C1 D9842 QTY1 SPEC REV QARV

D/C2 QTY2 CPN

(F63TNR)2

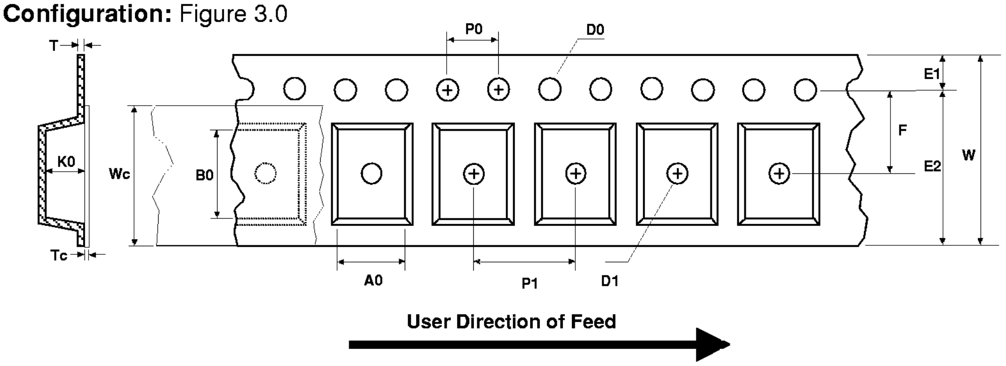
SOIC(8lds) Tape Leader and Trailer

Configuration: Figure 2.0



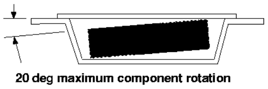
SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0

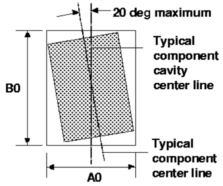


Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

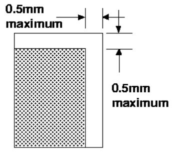
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

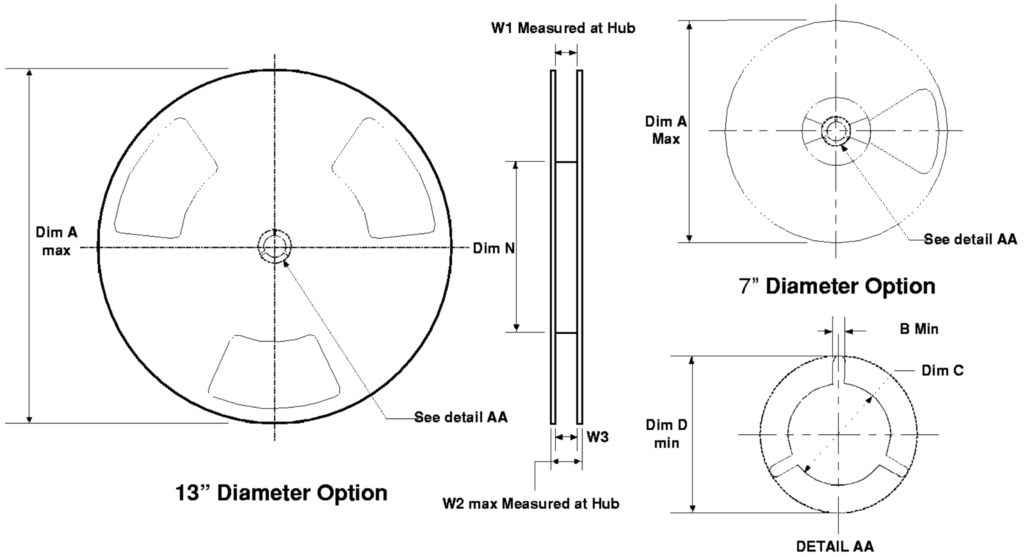


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

SOIC(8lds) Reel Configuration: Figure 4.0



13” Diameter Option

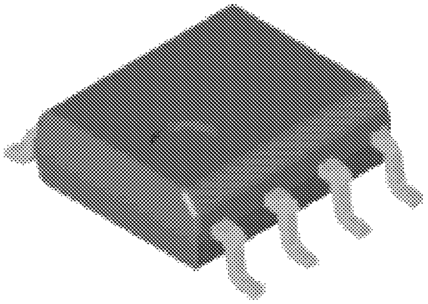
7” Diameter Option

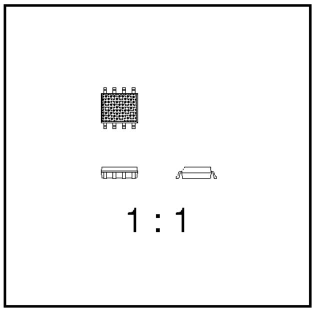
DETAIL AA

Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC-8 (FS PKG Code S1)

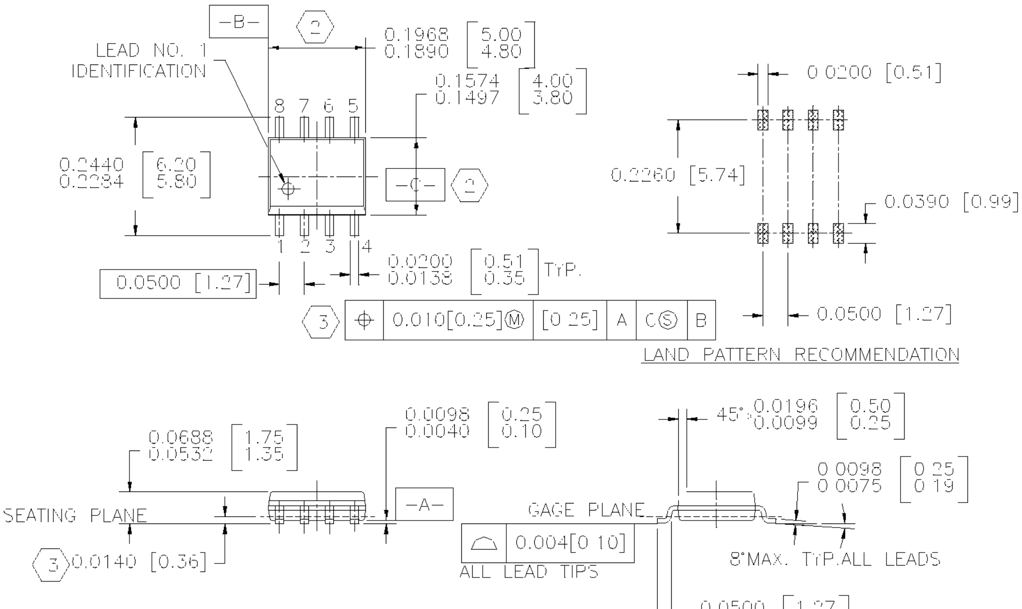




Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH.
200 MICROINCHES / 5.08 MICRONS MINIMUM
LEAD / TIN (SOLDER) ON COPPER.

⟨2⟩ THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

⟨3⟩ MAXIMUM LEAD 0.024 [0.609]

SO 0.150 WIDE 8 LEADS

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VCX™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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