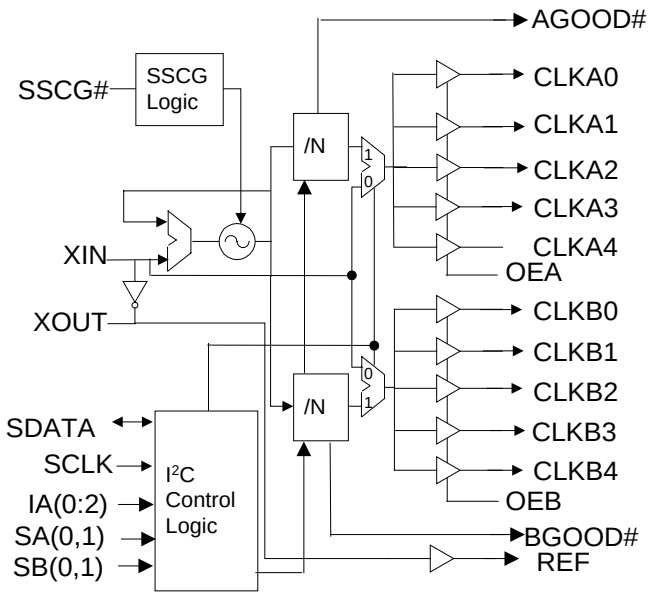
C9530

PCIX I/O System Clock Generator With EMI Control Features

Product Features

- Dedicated clock buffer power pins for reduced noise, crosstalk and jitter
- Buffer XIN Reference clock output
- Input clock frequency 33.3 MHz
- Reference may be a clock or a crystal
- Output frequencies of 33.3, 66.6, 100 and 133.3 MHz selectable (PCIX requirements)
- Output grouped in two banks of 5 clocks each.
- SMBus clock control interface for individual clock disabling, SSCG control and individual bank frequency selection
- Output clock duty cycle is 50% (± 5%)
- <250 pS skew between output clocks within a bank
- Output jitter <250 pSec. (175pSec with all outputs at the same frequency)
- Spread Spectrum feature for reduced EMI
- OE pins for separate output bank enable control and testability
- 48 Pin SSOP and TSSOP package

Block Diagram

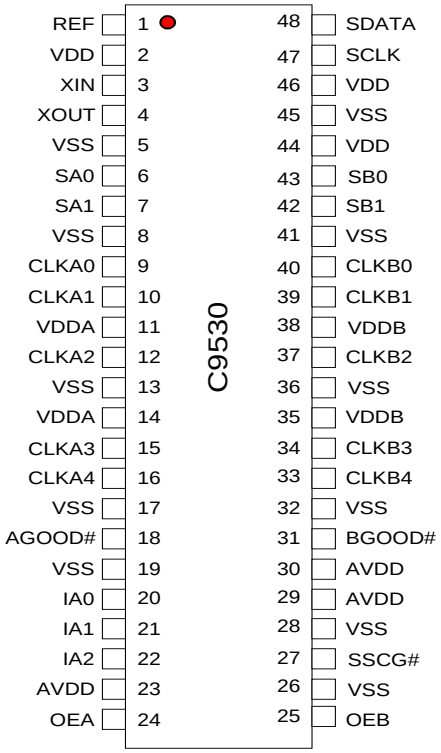


Test Mode Logic Table

INPUT PINS			OUTPUT PINS	
OEA	**SA1**	**SA0**	**CLKA(0:4)**	**REF**
OEB	**SB1**	**SB0**	**CLKB(0:4)**	
HIGH	LOW	LOW	XIN	XIN
HIGH	LOW	HIGH	2 * XIN	XIN
HIGH	HIGH	LOW	3 * XIN	XIN
HIGH	HIGH	HIGH	4 * XIN	XIN
LOW	X	X	Tri-State	Tri-State

Note: A and B banks have separate frequency select and output enable controls. XIN is the frequency of the clock on the device's XIN pin. OEA or OEB will tristate REF.

Pin Configuration



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Pin Description

Pin No.	Pin Name	PWR	I/O	Description
3	XIN	VDDA	I	Crystal Buffer input pin. Connects to a crystal, or an external clock source. Serves as input clock TCLK, in Test mode.
4	XOUT	VDDA	O	Crystal Buffer output pin. Connects to a crystal only. When a Can Oscillator is used or in Test mode, this pin is kept unconnected.
1	REF	VDD	O	Buffered inverted outputs of the signal applied at Xin, typically 33.33 MHz
24*	OEA	VDD	I	Output Enable for clock bank A. Causes the CLKA (0:4) output clocks to be in a Tri-state condition when driven to a logic low level.
25*	OEB	VDD	I	Output Enable for clock bank B. Causes the CLKB (0:4) output clocks to be in a Tri-state condition when driven to a logic low level.
18	AGOOD#	VDD	O	When this output signal is a logic low level, it indicates that the output clocks of the A bank are locked to the input reference clock. This output is latched.
31	BGOOD#	VDD	O	When this output signal is at a logic low level, it indicates that the output clocks of the B bank are locked to the input reference clock. This output is latched.
6*, 7*	SA(0,1)	VDD	I	Clock Bank A selection bits. These control the clock frequency that will be present on the outputs of the A bank of buffers. See table on page one for frequency codes and selection values.
43*, 42*	SB(0,1)	VDD	I	Clock Bank B selection bits. These control the clock frequency that will be present on the outputs of the B bank of buffers. See table on page one for frequency codes and selection values.
20*, 21*, 22*	IA(0:2)	VDD	I	SMBus address selection input pins. See SMBus Address table.
27*	SSCG#	VDD	I	Enables Spread Spectrum clock modulation when at a logic low level, see pg. 3.
48	SDATA	VDD	I/O	Data for the internal SMBus circuitry. See pg 4.
47	SCLK	VDD	I	Clock for the internal SMBus circuitry. See pg. 4
11, 14	VDDA	-	PWR	3.3V common power supply pin for Bank A PCI clocks CLKA (0:4).
38, 35	VDDB	-	PWR	3.3V common power supply pin for Bank B PCI clocks CLKB (0:4).
2, 44, 46	VDD	-	PWR	Power supply for internal Core logic.
23, 29, 30	AVDD	-	PWR	Power for internal analog circuitry. This supply should have a separately decoupled current source from VDD.
9, 10, 12, 15, 16	CLKA (0:4)	VDDA	O	A bank of Five 33.3, 66.6, 100.0 or 133.3 MHz output clocks (1x, 2x, 3x and 4x Xin clock).
40, 39, 37, 34, 33	CLKB (0:4)	VDDB	O	A bank of Five 33.3, 66.6, 100.0 or 133.3 MHz output clocks (1x, 2x, 3x, and 4x Xin clock).
5, 8, 13, 17, 19, 26, 28, 32, 36, 41, 45	VSS	-	PWR	Ground pins for the device

Notes: Pin numbers ending with a * indicate that they contain device internal pull-up resistors that will insure that they are sensed as a logic 1 if no external circuitry is connected to them.

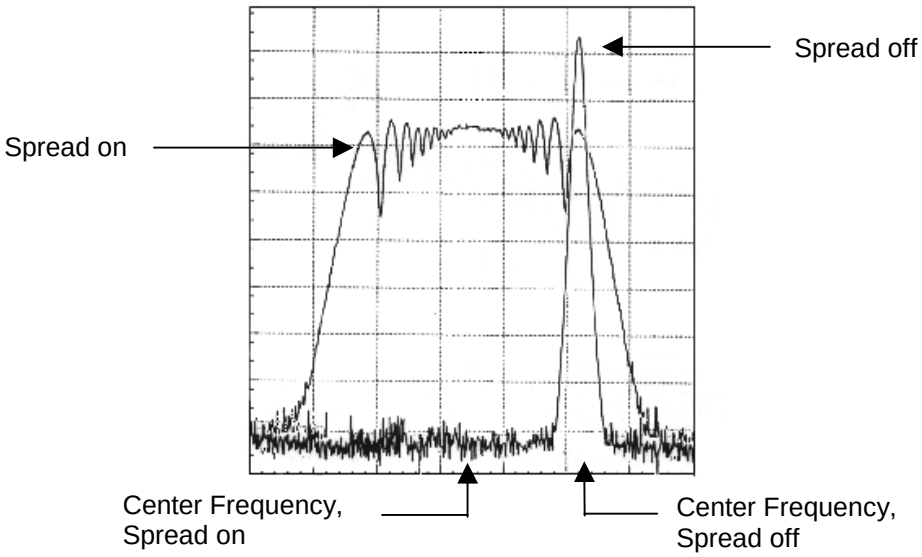
A bypass capacitor (0.1 µF) should be placed as close as possible to each VDD pin. If these bypass capacitors are not close to the pins, their high frequency filtering characteristic will be canceled by the lead inductance of the trace. PWR = Power connection, I = Input, O = Output and I/O = both input and output functionality of the pin(s).

Spectrum Spread Clocking

Down Spread Description

Spread Spectrum is a modulation technique for distributing clock period over a certain bandwidth (called Spread Bandwidth). This technique allows the distribution of the undesirable electromagnetic energy (EMI) over a wide range of frequencies therefore reducing the average radiated energy present at any frequency over a given time period. As the spread is specified as a percentage of the resting (non-spread) frequency value, it is effective at the fundamental and, to a greater extent, at all it's harmonics.

In this device, Spread Spectrum is enabled externally through pin 27 (SSCG#) or internally via SMBus Byte 0 Bit 0 and 6. Spread spectrum is enabled externally when the SSCG# pin is low. This pin has an internal device pull up resistor, which causes its state to default to a high (Spread Spectrum disabled) unless externally forced to a low. It may also be enabled by programming SMBus Byte 0 Bit 0 LOW (to enable SMBus control of the function) and then programming SMBus Byte 0 Bit 6 LOW to set the feature active.



Spectrum Spreading Selection Table

Output clock Frequency	% OF FREQUENCY SPREADING		MODE
	SMBus Byte 0 Bit 5 =0	SMBus Byte 0 Bit 5 =1	
33.3 MHz (XIN)	1.0% (-1.0% + 0%)	0.5% (-0.5% + 0%)	Down Spread
66.6 MHz (XIN*2)	1.0% (-1.0% + 0%)	0.5% (-0.5% + 0%)	Down Spread
100.0 MHz (XIN*3)	1.0% (-1.0% + 0%)	0.5% (-0.5% + 0%)	Down Spread
133.3 MHz (XIN*4)	1.0% (-1.0% + 0%)	0.5% (-0.5% + 0%)	Down Spread

When SSCG is enabled, the device will down spread the clock over a range that is 1% of its resting frequency. This means that for a 100 MHz output clock the frequency will sweep through a spectral range from 99 to 100 MHz.

2-Wire SMBus Control Interface

The 2-wire control interface implements a write slave only interface according to SMBus specification. The device can be read back. Sub addressing is not supported, thus all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled. 100 Kbits/second (standard mode) data transfer is supported.

Through the use of the IA0, IA1, and IA2 pins the SMBus address of the device may be changed so that multiple devices may reside on a single SMBus control signaling bus and not interfere with each other.

SMBus Address Selection Table

SMBus address of the device	IA0 BIT (Pin 20)	IA1 BIT (Pin 21)	IA2 BIT (Pin 22)
DE	0	0	0
DC	1	0	0
DA	0	1	0
D8	1	1	0
D6	0	0	1
D4	1	0	1
D0	0	1	1
D2	1	1	1

During normal data transfer, the SDATA signal only changes when the SCLK signal is low, and is stable when SCLK is high. There are two exceptions to this. A high to low transition on SDATA while SCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SCLK is high indicates the end of a data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledgement is generated. The first byte of a transfer cycle is a 7-bit address with a Read/Write bit (R/W#) as the LSB. R/W# = 1 in read mode.

The device will respond to writes to 10 bytes (max) of data to its selected address by generating the acknowledge (low) signal on the SDATA wire following reception of each byte.

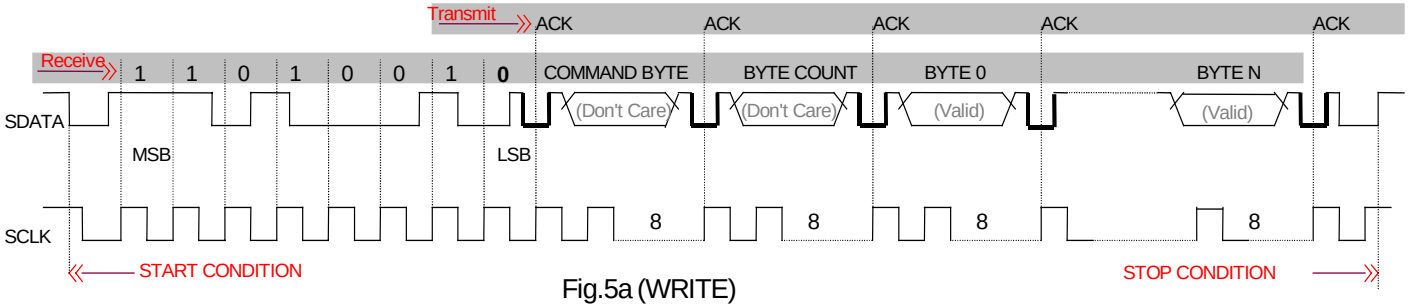


Fig.5a (WRITE)

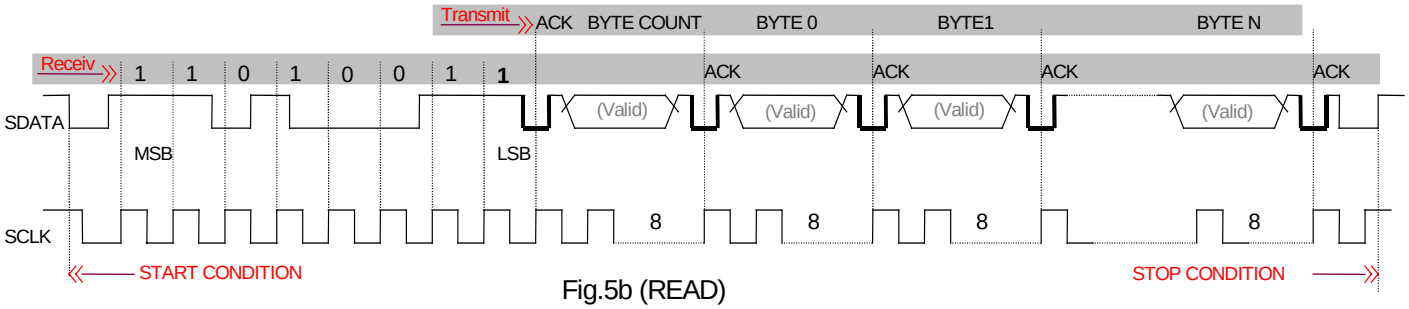


Fig.5b (READ)

Fig.5

Serial Control Registers

NOTE: The Pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown initially only after true power up condition occurs.
Following the acknowledge of the Address Byte , two additional bytes must be sent:

1) "**Command Code** " byte, and
2) "**Byte Count**" byte.
3)

Although the data (bits) in these two bytes are considered "don't care"; they must be sent and will be acknowledged.

Byte 0: Function Select Register

Bit	@Pup	Pin#	Description
7	1	-	Test Mode Enable. 1=normal operation, 0 = Test mode
6	0	27	Spread Spectrum modulation control bit (effective only when Bit 0 of this register is set to a 0) 0=OFF, 1 = ON
5	1	-	SSCG Spread width select. 1=0.5%, 0=1.0% See table below for clarification
4	0	42	SB1 Bank B MSB frequency control bit (effective only when Bit 0 of this register is set to a 0)
3	0	43	SB0 Bank B LSB frequency control bit (effective only when Bit 0 of this register is set to a 0)
2	0	7	SA1 Bank A MSB frequency control bit (effective only when Bit 0 of this register is set to a 0)
1	0	6	SA0 Bank A LSB frequency control bit (effective only when Bit 0 of this register is set to a 0)
0	1	-	Hardware/SMBus frequency control. 1=Hardware (pins 6, 7, 42, 43, and 27), 0=SMBus Byte 0 bits 1-4 and 6

Clarification Table for Byte0, bit5

Byte 0, bit6	Byte0, bit5	Description
0	0	Frequency generated from second PLL
0	1	Frequency generated from XIN
1	0	Spread @ -1.0%
1	1	Spread @ -0.5%

Test Table

These output frequencies will be present when SMBus byte 0 bit 7 has been set to a logic 0 state.

Test Function	Outputs		
Clock	CLKA(0:4)	CLKB(0:4)	REF
Frequency	XIN/6	XIN/4	XIN

Table 3

Notes:

1. XIN is the frequency of the clock that is present on the XIN input during test mode.

Byte 1: A Bank and REF Clock Control Register
(1 = Enable, 0 = Stopped at a low level)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	1	REF Enable/Stopped
4	1	16	CLKA4 Enable/Stopped
3	1	15	CLKA3 Enable/Stopped
2	1	12	CLKA2 Enable/Stopped
1	1	10	CLKA1 Enable/Stopped
0	1	9	CLKA0 Enable/Stopped

Byte 2: B Bank Clock Control Register
(1 = Enable, 0 = Stopped at a low level)

Bit	@Pup	Pin#	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	33	CLKB4 Enable/Stopped
3	1	34	CLKB3 Enable/Stopped
2	1	37	CLKB2 Enable/Stopped
1	1	39	CLKB1 Enable/Stopped
0	1	40	CLKB0 Enable/Stopped

Note: Stopping a clock indicated that the clock output is fixed in a logic low state. This effect will occur within 2 clock cycles from the time the bit is set and does so in a manner so as not to cause any short or runt clock cycles. When the stop is bit is changed from a stopped state to a running state the same (maximum 2 clock latency) delay occurs with the first cycle being full in period (for the frequency that is selected

Internal Crystal Oscillator

This device will operate in two input reference clock configurations. In its simplest mode a 33.33 MHz fundamental cut parallel resonant crystal is attached to the XIN and XOUT pins.

In the second mode a 33.33MHz input reference clock is driven in on the XIN clock from an external source. In this application the XOUT pin must be left disconnected.

Output Clock Frequency Control

All of the output clocks have their frequency selected by the logic state of the S0 and S1 control bits. The source of these control signals is determined by the SMBus register Byte 0 Bit 0. At initial power up this bit is set of a logic 1 state and thus the frequency selections are controlled by the logic levels present on the devices SA(0,1) and SB(0,1) pins. If the application does not use an SMBus interface then hardware frequency selection SA(0,1), (SB(0,1) that must be used. If it is desired to control the output clocks using an SMBus interface, then this bit (Byte 0 Bit 0) must first be set to a low state. After this is done the device will use the contents of the internal SMBus register Byte 0, Bits 1,2,3 and 4) to control the output clock's frequency.

Output Clock Tri-state Control

All of the clocks in Bank A (CLKA(0:4)) and bank B (CLKB(0:4)) may be placed in a tri-state condition by bringing their relevant OE pins (OEA and OEB) to a logic low state. This transition to and from a tristate and active condition is a totally asynchronous event and clock glitching may occur during the transitioning states. This function is intended as a board level testing feature. When output clocks are being enabled and disabled in active environments the SMBus control register bits are the preferred mechanism to control these signals in an orderly and predictable manner.

Both output enable pins contain internal pull-up resistors that will insure that a logic 1 (high) is maintained and sensed by the device if no external circuitry is connected to these pins.

Absolute Maximum Ratings

Maximum Power Supply:	5.5
Storage Temperature:	-65ºC to + 150ºC
Operating Temperature:	0ºC to +70ºC
Maximum ESD protection	2000V
Maximum Input Voltage Relative to VDD:	VDD + 0.3V
Maximum Input Voltage Relative to VSS:	VSS - 0.3V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD)

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL1	-	-	1.0	Vdc	note 1
Input High Voltage	VIH1	2.0	-	-	Vdc	
Input Low Voltage	VIL2	-	-	1.0	Vdc	note 2
Input High Voltage	VIH2	2.2	-	-	Vdc	
Input Low Current (@VIL = VSS)	IIL	-66		-5	µA	For internal Pull up resistors, note 1 and note 3
Input High Current (@VIL = VDD)	IIH			5	µA	
Tri-State leakage Current	Ioz	-	-	10	µA	
Dynamic Supply Current	Idd3.3V	-	-	300	mA	note 4
Unloaded Supply Current	Isdd	-	-	30	mA	Device running, OEA and OEB at a logic low level (outputs disabled).
Input pin capacitance	Cin	-	-	5	pF	All input pins except XIN and XOUT
Pin inductance	Lpin	-	-	7	nH	
Crystal pin capacitance	Cxtal	32	34	38	pF	from XIN and XOUT Pins to Ground. note 5
Crystal DC Bias Voltage	V_{BIAS}	0.3Vdd	Vdd/2	0.7Vdd	V	
Crystal Startup time	Txs	-	-	40	µS	From Stable 3.3V power supply.
VDD = AVDD = VDDA = VDDB = 3.3V ±5%, TA = 0ºC to +70ºC						

Note1: Applicable to input signals: SA0, SA1, SB0, SB1, OEA, OEB and SSCG#
Note2: Applicable to Sdata, and Sclk.
Note3: Although internal pull-up resistors have a typical value of 250K, this value may vary between 200K and 500K.
Note4: All outputs load in accordance with table 1, all output buffers enabled and all OE pins at a logic 1 level.
Note5: Although the device will reliably interface with crystals of a 17pF – 20pF C_L range, it is optimized to interface with a typical C_L = 18pF crystal specifications.

AC Parameters

Symbol	Parameter	Output Frequency								Units	Notes
		133 MHz		100 MHz		66 MHz		33 MHz			
		Min	Max	Min	Max	Min	Max	Min	Max		
Tcyc	CLKA(0:4) CLKB(0:4) period	7.0	8.0	9.5	10.5	14.5	15.5	25.5	30.5	ns	1, 2, 4
THIGH	CLKA(0:4) CLKB(0:4) period	3	-	4	-	6	-	11	-	ns	2,6
TLOW	CLKA(0:4) CLKB(0:4) low time	3	-	4	-	6	-	11	-	ns	2, 7
Tr / Tf	CLKA(0:4) a, CLKB(0:4)rise and fall times	0.50	1.33	0.50	1.33	0.50	1.33	0.50	1.33	ns	2, 3
TSKEW	(Any CLK) to (Any CLK) Skew time	-	250	-	250	-	250	-	250	ps	2, 4, 5. 9
TCCJ	CLK(A:B)(0:4) Cycle to Cycle Jitter	250 or 175 (see note 10)								ps	2, 4, 5, 10
Tr / Tf	REFOUT rise and fall times	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns	2, 3
TCCJ	REFOUT Cycle to Cycle Jitter	750								ps	2, 4
tpZL, tpZH	OE to clock enable delay (all outputs)	-	10.0	-	10.0	-	10.0	-	10.0	ns	
tpLZ, tpHZ	OE to clock disable delay (all outputs)	-	10.0	-	10.0	-	10.0	-	10.0	ns	
tstable	All clock Stabilization from power-up	-	3	-	3	-	3	-	3	ms	8

Note 1: This parameter is measured as an average over 1uS duration, with an input frequency of 33.333 MHz
Note 2: All outputs loaded as per table 1 below.
Note 3: Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V (see Fig.6A and Fig.6B)
Note 4: Probes are placed on the pins, and measurements are acquired at 1.5V. (See Figs.6A & 6B)
Note 5: This measurement is applicable with Spread ON or OFF.
Note 6: Probes are placed on the pins, and measurements are acquired at 2.4Vs, (see Figs. 6A & 6B)
Note 7: Probes are placed on the pins, and measurements are acquired at 0.4V.
Note 8: The time specified is measured from when all VDD's reach their respective supply rail (3.3V) till the frequency output is stable and operating within the specifications
Note 9: Applicable only to clocks within the same bank
Note10: The cycle to cycle jitter of the device is dependent on 2 factors. They are the jitter component of the input reference clock and whether the 2 output clock banks are operating at the same frequency, When the frequency of the output banks is the same, output jitter is guaranteed to not be more than 175pSec. When the output clocks of each bank differ in frequency, the device is guaranteed to be no more than 250 pSec.

Output Name	Max Load (in pF)
REF	20
CLK(A:B)(0:4)	30

Table 1

Test and Measurement Setup

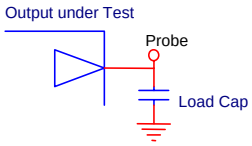


Fig. 6A

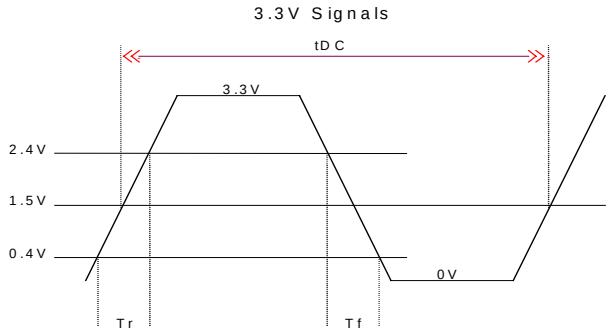


Fig. 6B

Output Buffer Characteristics

Buffer Characteristics for CLKA(0:4), CLKB(0:4), and REF

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current	IOH_1	-33	-	-	mA	VDD-0.5
Pull-Up Current	IOH_2	-11	-	-	mA	1.2V
Pull-Down Current	IOL_1	9.4	-	-	mA	0.4V
Pull-Down Current	IOL_2	22	-	-	mA	1.2V
VDD = AVDD = VDDA = VDDB = 3.3V ±5%, TA = 0ºC to +70ºC						

Suggested Oscillator Crystal Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Frequency	F_o	33.0	33.33	33.5	MHz	
Tolerance	T_C	-	-	+/-100	PPM	Note 1
	T_S	-	-	+/- 100	PPM	Stability (T_A -10 to +60C) Note 1
	T_A	-	-	5	PPM	Aging (first year @ 25C) Note 1
Operating Mode	-	-	-	-		Parallel Resonant, Note 1
Load Capacitance	C_{XTAL}	-	20	-	pF	The crystal's rated load. Note 1
Effective Series Resistance (ESR)	R_{ESR}	-	40	-	Ohms	Note 2

Note1: For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meets or exceeds these specifications

Note 2: Larger values may cause this device to exhibit oscillator startup problems

To obtain the maximum accuracy, the total circuit loading capacitance should be equal to C_{XTAL}. This loading capacitance is the effective capacitance across the crystal pins and includes the clock generating device pin capacitance (C_{FTG}), any circuit traces (C_{PCB}), and any onboard discrete load capacitors (C_{DISC}).

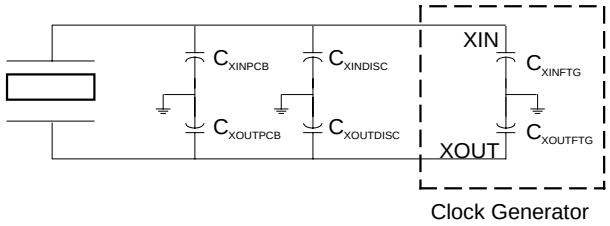
Suggested Oscillator Crystal Parameters (Cont.)

The following formula and schematic may be used to understand and calculate either the loading specification of a crystal for a design or the additional discrete load capacitance that must be used to provide the correct load to a known load rated crystal.

$$C_L = \frac{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) \times (C_{XOUTPCB} + C_{XOUTFTG} + C_{XOUTDISC})}{(C_{XINPCB} + C_{XINFTG} + C_{XINDISC}) + (C_{XOUTPCB} + C_{XOUTFTG} + C_{OUTDISC})}$$

Where:

C_{XTAL} = the load rating of the crystal
$C_{XOUTFTG}$ = the clock generators XIN pin effective device internal capacitance to ground
$C_{XOUTFTG}$ = the clock generators XOUT pin effective device internal capacitance to ground
C_{XINPCB} = the effective capacitance to ground of the crystal to device PCB trace
$C_{XOUTPCB}$ = the effective capacitance to ground of the crystal to device PCB trace
$C_{XINDISC}$ = any discrete capacitance that is placed between the XIN pin and ground
$C_{XOUTDISC}$ = any discrete capacitance that is placed between the XOUT pin and ground

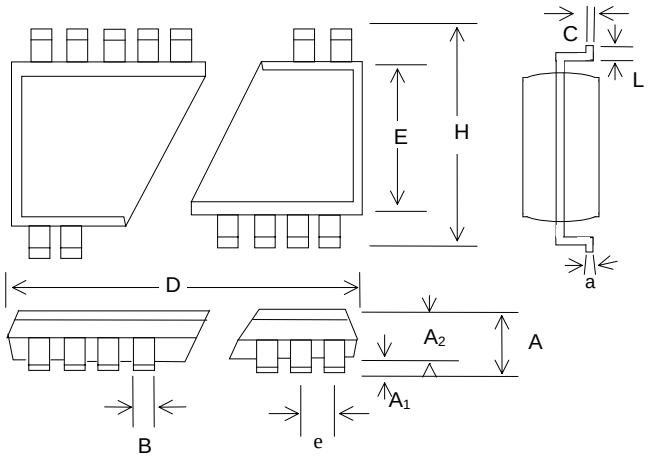


As an example, and using this formula for this datasheet's device, a design that has no discrete loading capacitors (C_{DISC}) and each of the crystal to device PCB traces has a capacitance (C_{PCB}) to ground of 4pF (typical value) would calculate as:

$$C_L = \frac{(4pF + 36pF + 0pF) \times (4pF + 36pF + 0pF)}{(4pF + 36pF + 0pF) + (4pF + 36pF + 0pF)} = \frac{40 \times 40}{40 + 40} = \frac{1600}{80} = 20pF$$

Therefore to obtain output frequencies that are as close to this data sheets specified values as possible, in this design example, you should specify a parallel cut crystal that is designed to work into a load of 20pF.

Package Drawing and Dimensions



48 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.011	0.17	-	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.488	0.492	0.496	12.40	12.50	12.60
E	0.236	0.240	0.244	6.00	6.10	6.20
e	0.02 BSC			0.50 BSC		
H	0.315	0.319	0.323	8.00	8.10	8.20
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

48 Pin SSOP Outline Dimensions

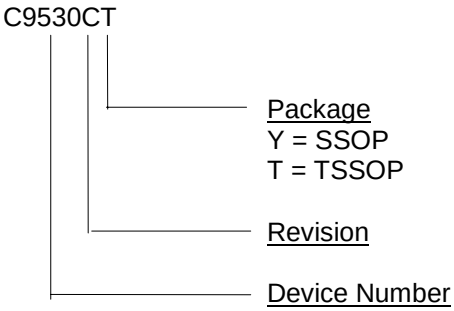
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.095	0.102	0.110	2.41	2.59	2.79
A_1	0.008	0.012	0.016	0.203	0.305	0.406
A2	0.088	-	0.092	2.24	-	2.34
B	0.008	-	0.0135	0.203	-	0.343
C	0.005	-	0.010	0.127	-	0.254
D	0.620	0.625	0.630	15.75	15.88	16.00
E	0.291	0.295	0.299	7.39	7.49	7.60
e	0.025 BSC			0.635 BSC		
H	0.395	-	0.420	10.03	-	10.67
L	0.020	-	0.040	0.508	-	1.016
a	0º	-	8º	0º	-	8º

Ordering Information

Part Number	Package Type	Production Flow
C9530CY	48 Pin SSOP	Commercial, 0°C to +70°C
C9530CT	48 Pin TSSOP	Commercial, 0°C to +70°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: CYPRESS
C9530CT
Date Code, Lot #



Notice

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Document Title: C9530 PCIX I/O System Clock Generator with EMI Control Features **Document Number:** 38-07033				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106961	06/12/01	IKA	Convert from IMI to Cypress