

IS64LP12832

IS64LP12836



128K x 32, 128K x 36 SYNCHRONOUS PIPELINED STATIC RAM

PRELIMINARY INFORMATION
JULY 2004

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-pin TQFP and 119-pin PBGA package
- Power-down snooze mode
- Power Supply
 - + 3.3V V_{DD}
 - + 3.3V OR 2.5V V_{DDQ} (I/O)
- Temperature offerings
 - Option A2: -40° C to +105° C
 - Option A3: -40° C to +125° C

DESCRIPTION

The *ISSI* IS64LP12832 and IS64LP12836 are high-speed synchronous static RAMs designed to provide high-performance memory with burst for high-speed networking and communication applications. IS64LP12832 is organized as 131,072 words by 32 bits. IS64LP12836 is organized as 131,072 words by 36 bits. The IS64LP12832 and IS64LP12836 are fabricated with *ISSI*'s advanced CMOS technology. These devices integrate a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. **BW1** controls DQa, **BW2** controls DQb, **BW3** controls DQc, **BW4** controls DQd, conditioned by **BWE** being LOW. A LOW on **GW** input would cause all bytes to be written.

Bursts can be initiated with either **ADSP** (Address Status Processor) or **ADSC** (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the **ADV** (burst address advance) input pin.

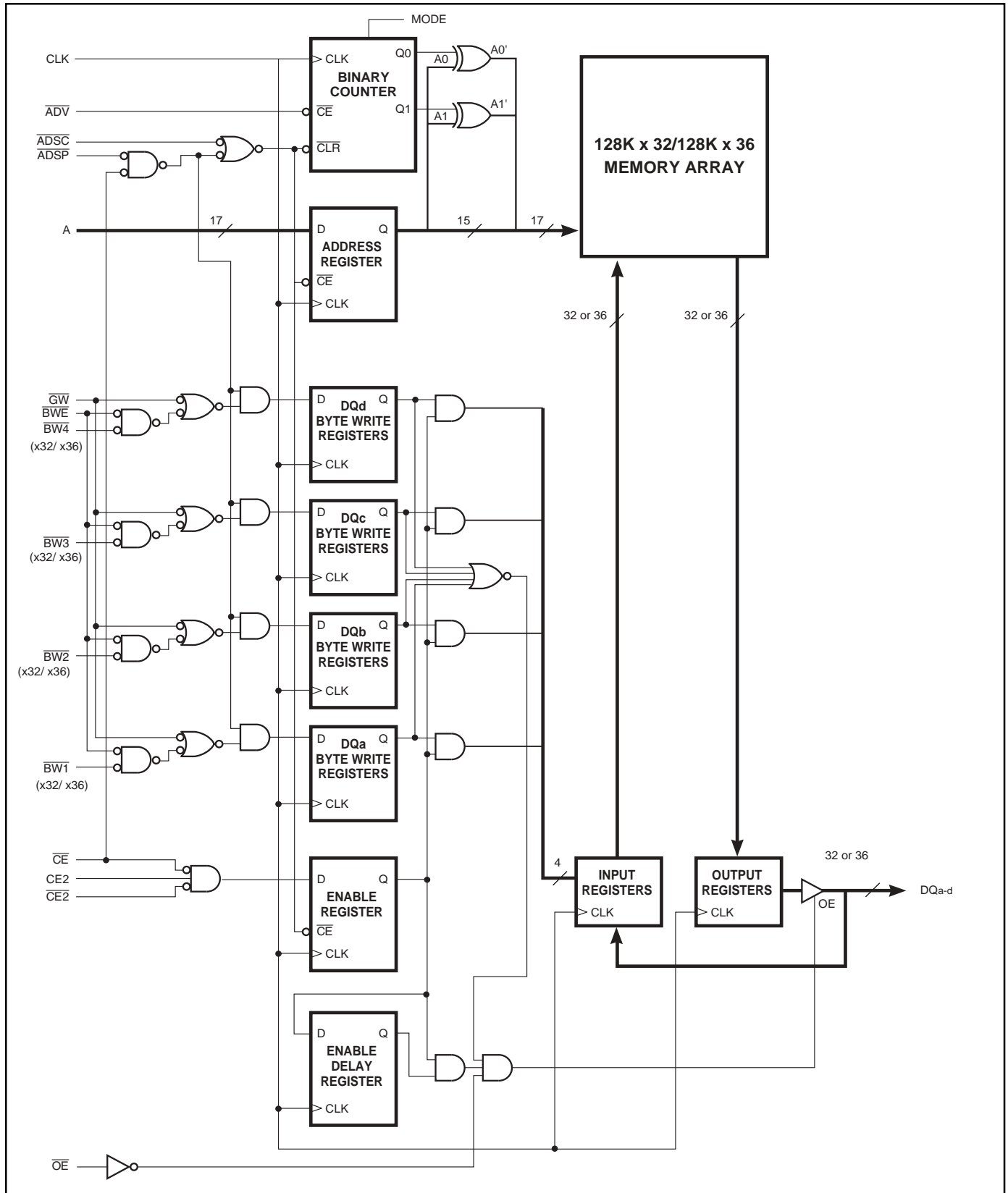
The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

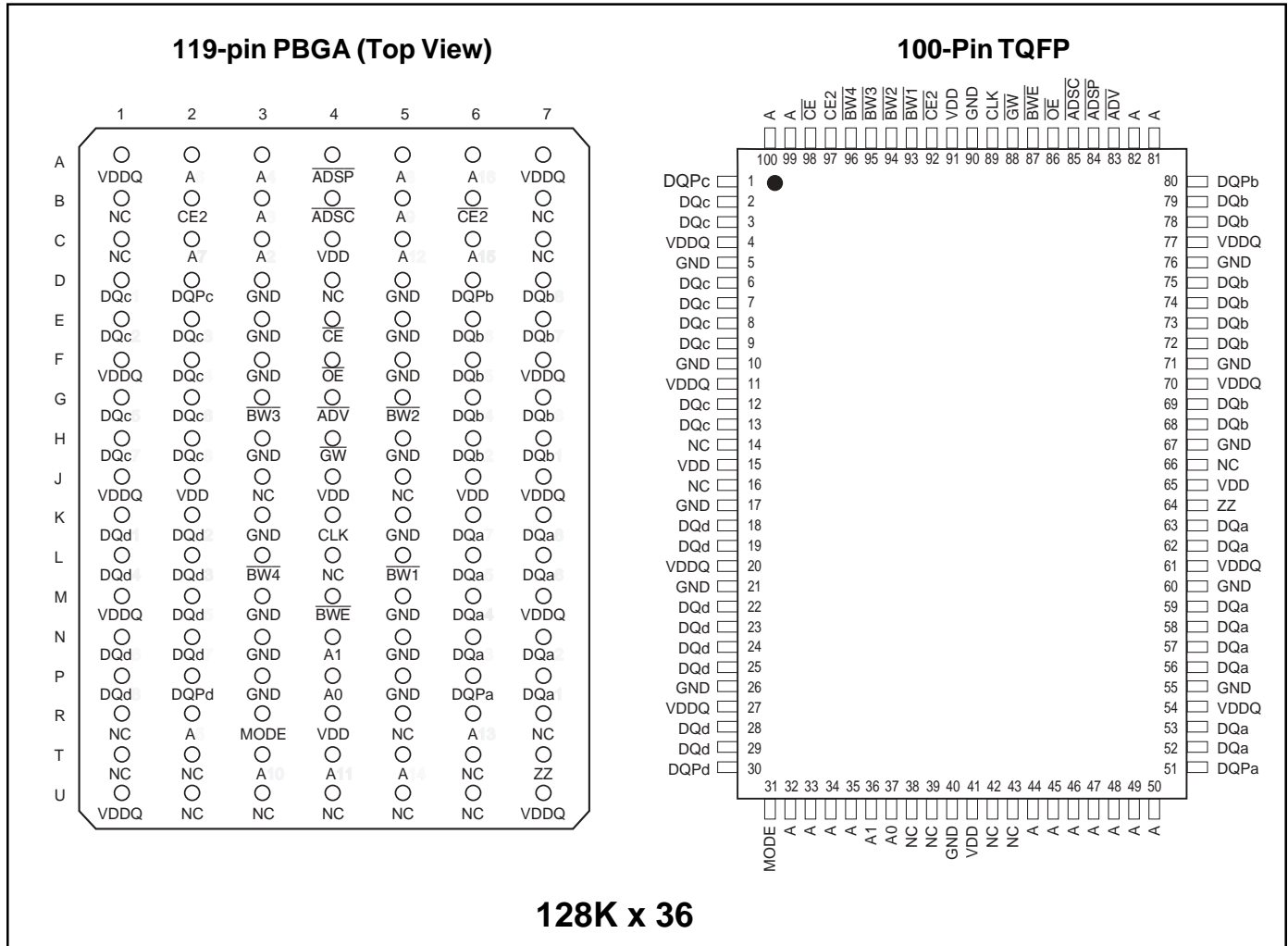
Symbol	Parameter	-150	Units
tkQ	Clock Access Time	4.3	ns
tkC	Cycle Time	6.7	ns
	Frequency	150	MHz

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BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{\text{ADSP}}$	Synchronous Processor Address Status
$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BW1-BW4}}$	Individual Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable

$\overline{\text{GW}}$	Synchronous Global Write Enable
$\overline{\text{CE}}, \overline{\text{CE2}}, \text{CE2}$	Synchronous Chip Enable
$\overline{\text{OE}}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V _{DD}	+3.3V Power Supply
GND	Ground
V _{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

TRUTH TABLE

Operation	Address Used	\overline{CE}	CE2	$\overline{CE2}$	ADSP	ADSC	ADV	WRITE	\overline{OE}	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	X	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	X	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

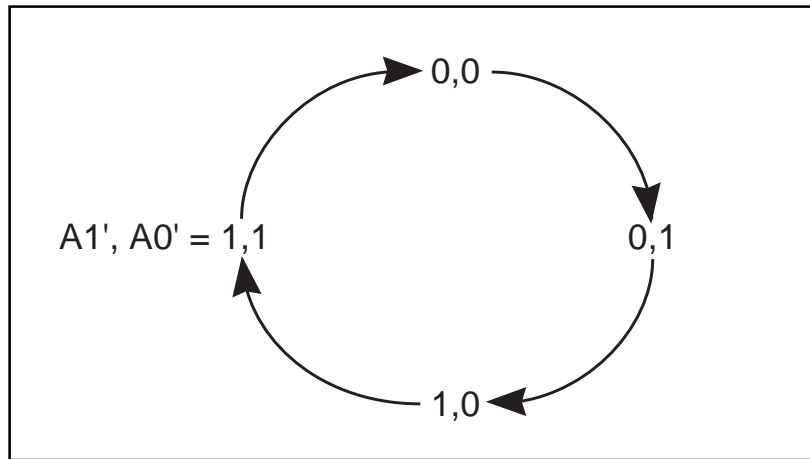
PARTIAL TRUTH TABLE

Function	\overline{GW}	\overline{BWE}	BW1	BW2	BW3	BW4
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-55 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	-0.5 to V _{DDQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	-0.5 to V _{DD} + 0.5	V
V _{DD}	Voltage on V _{DD} Supply Relative to GND	-0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{DD}	3.3V (I/O)		2.5V (I/O)	
			V _{DDQ}	V _{DDQ}	V _{DDQ}	V _{DDQ}
A2	-40°C to +105°C	3.3V, +10%, -5%	3.3V, +10%, -5%	2.5V ± 5%		
A3	-40°C to +125°C	3.3V, +10%, -5%	3.3V, +10%, -5%	2.5V ± 5%		

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	2.5V (I/O)		3.3V (I/O)		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0 mA (3.3V) I _{OH} = 1.0 mA (2.5V)	2.0	—	2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V _{IH}	Input HIGH Voltage		1.7	V _{DD} + 0.3	2.0	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.7	-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{DD}	-5	5	-5	5	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{DDQ} , $\overline{OE} = V_I$	-5	5	-5	5	μA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	-150		Unit
			Max.	Max.	
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs = V _{IL} or V _{IH} $\overline{OE} = V_{IH}$, V _{DD} = Max. Cycle Time ≥ t _{kc} min.	A2	280	mA
			A3	290	mA
I _{SB}	Standby Current	Device Deselected, V _{DD} = Max., All Inputs = V _{IH} or V _{IL} CLK Cycle Time ≥ t _{kc} min.	A2	80	mA
			A3	90	mA
I _{ZZ}	Power-down Mode Current	ZZ = V _{DD} Clock Running All Inputs ≤ GND + 0.2V or ≥ V _{DD} - 0.2V	A2	20	mA
			A3	25	mA

Notes:

- The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{DD}.
- The MODE pin should be tied to V_{DD} or GND. It exhibits ±10 μA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{DD} - 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

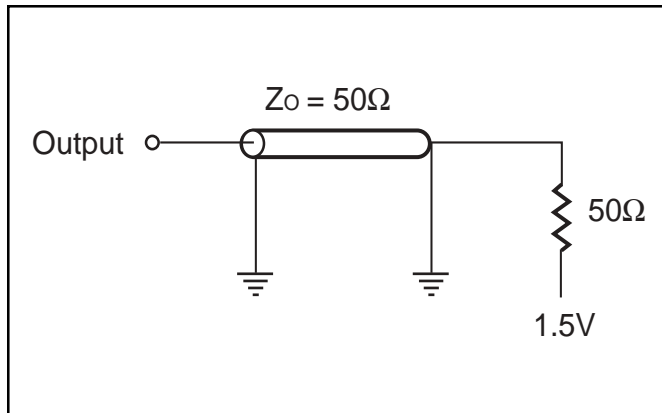


Figure 1

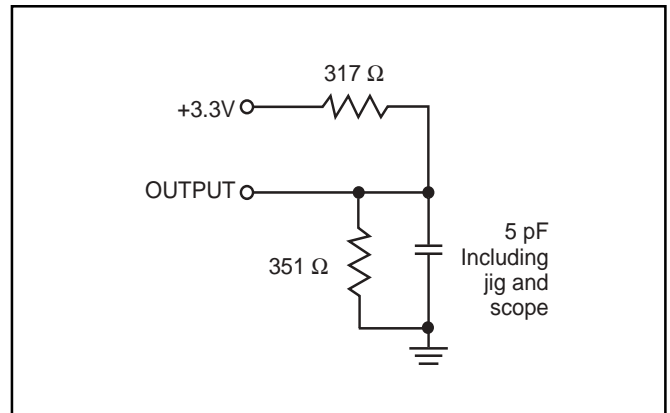


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

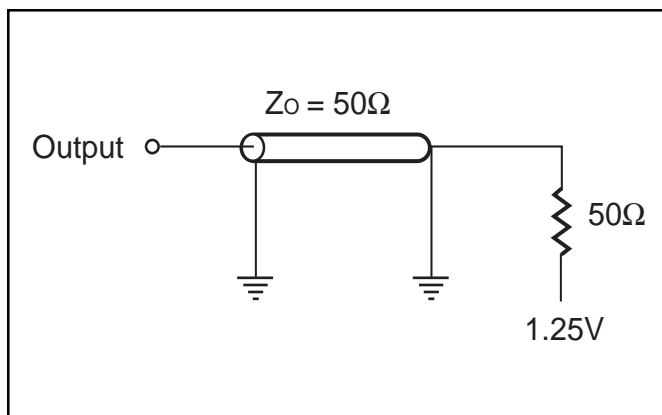


Figure 3

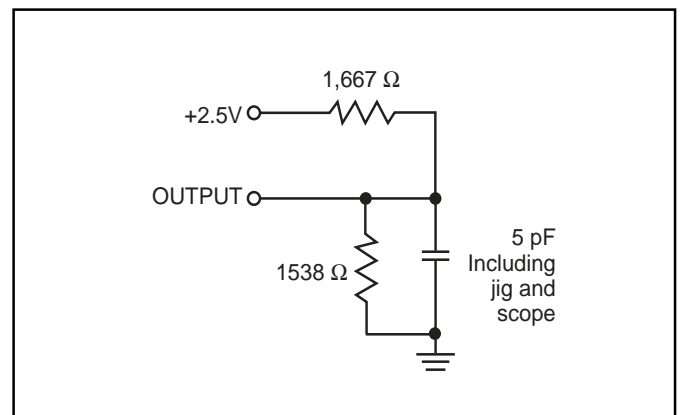


Figure 4

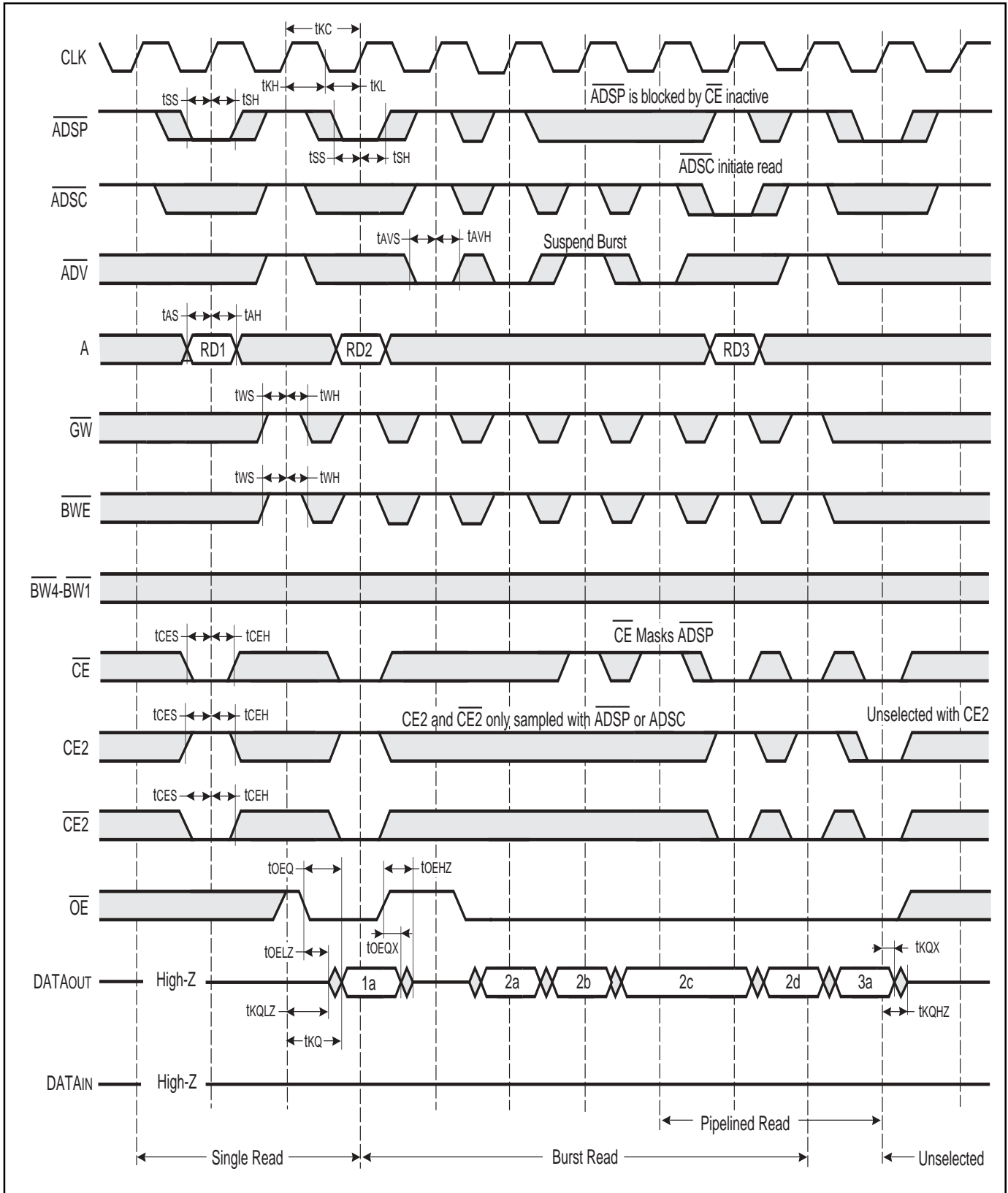
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-150		Unit
		Min.	Max.	
f _{MAX} ⁽³⁾	Clock Frequency	—	150	MHz
t _{KC} ⁽³⁾	Cycle Time	6.7	—	ns
t _{KH}	Clock High Time	2.6	—	ns
t _{KL} ⁽³⁾	Clock Low Time	2.6	—	ns
t _{KQ} ⁽³⁾	Clock Access Time	—	4.3	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	3.0	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	1.5	3.5	ns
t _{OEQ} ⁽³⁾	Output Enable to Output Valid	—	4.2	ns
t _{OEQX} ⁽¹⁾	Output Disable to Output Invalid	0	—	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	ns
t _{OEHZ} ^(1,2)	Output Disable to Output High-Z	2.0	3.5	ns
t _{AS} ⁽³⁾	Address Setup Time	2.0	—	ns
t _{SS} ⁽³⁾	Address Status Setup Time	1.5	—	ns
t _{WS} ⁽³⁾	Write Setup Time	1.5	—	ns
t _{CES} ⁽³⁾	Chip Enable Setup Time	2.0	—	ns
t _{AVS} ⁽³⁾	Address Advance Setup Time	1.5	—	ns
t _{AH} ⁽³⁾	Address Hold Time	1.0	—	ns
t _{SH} ⁽³⁾	Address Status Hold Time	1.0	—	ns
t _{WH} ⁽³⁾	Write Hold Time	1.0	—	ns
t _{CEH} ⁽³⁾	Chip Enable Hold Time	1.0	—	ns
t _{AVH} ⁽³⁾	Address Advance Hold Time	1.0	—	ns

Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

READ/WRITE CYCLE TIMING



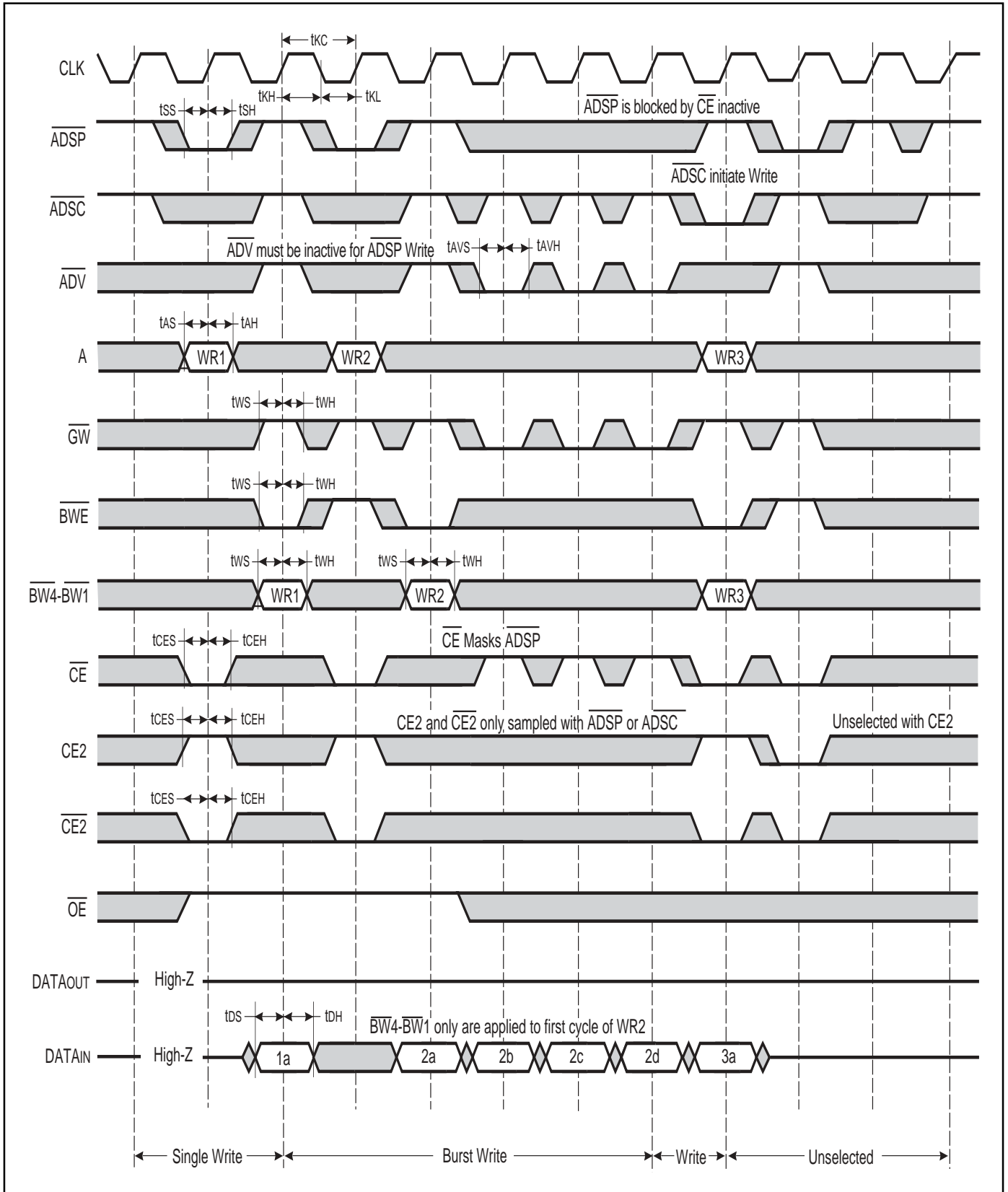
WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-150		Unit
		Min.	Max.	
t _{KC} ⁽¹⁾	Cycle Time	6.7	—	ns
t _{KH} ⁽¹⁾	Clock High Time	2.6	—	ns
t _{KL} ⁽¹⁾	Clock Low Time	2.6	—	ns
t _{AS} ⁽¹⁾	Address Setup Time	2.0	—	ns
t _{SS} ⁽¹⁾	Address Status Setup Time	1.5	—	ns
t _{WS} ⁽¹⁾	Write Setup Time	1.5	—	ns
t _{DS} ⁽¹⁾	Data In Setup Time	1.5	—	ns
t _{CES} ⁽¹⁾	Chip Enable Setup Time	2.0	—	ns
t _{AVS} ⁽¹⁾	Address Advance Setup Time	1.5	—	ns
t _{AH} ⁽¹⁾	Address Hold Time	1.0	—	ns
t _{SH} ⁽¹⁾	Address Status Hold Time	1.0	—	ns
t _{DH} ⁽¹⁾	Data In Hold Time	1.0	—	ns
t _{WH} ⁽¹⁾	Write Hold Time	1.0	—	ns
t _{CEH} ⁽¹⁾	Chip Enable Hold Time	1.0	—	ns
t _{AVH} ⁽¹⁾	Address Advance Hold Time	1.0	—	ns

Note:

1. Tested with load in Figure 1.

WRITE CYCLE TIMING



SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS

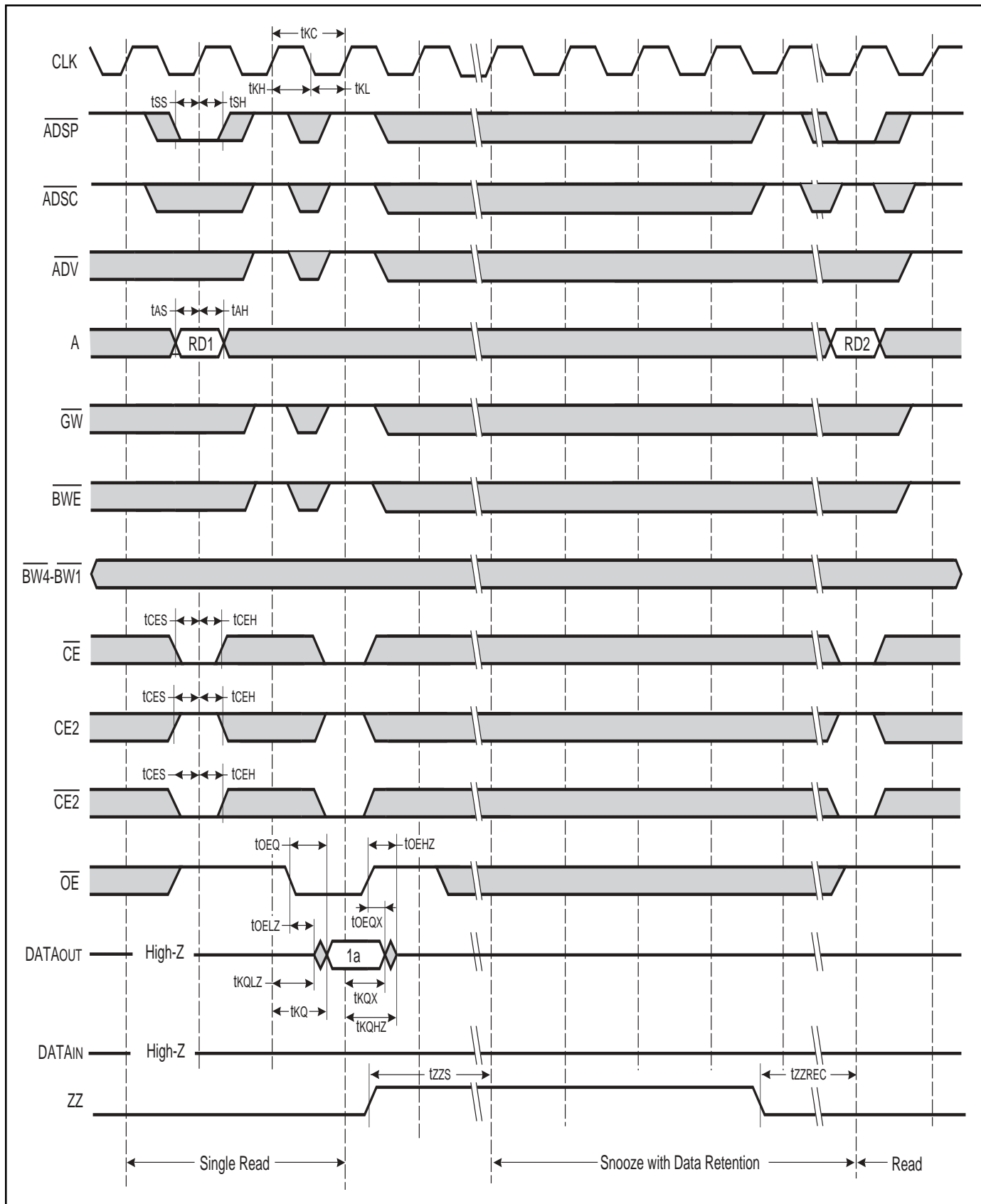
(Over Operating Range)

Symbol	Parameter	-150		Unit
		Min.	Max.	
t _{KC} ⁽³⁾	Cycle Time	6.7	—	ns
t _{KH} ⁽³⁾	Clock High Time	2.6	—	ns
t _{KL} ⁽³⁾	Clock Low Time	2.6	—	ns
t _{KQ} ⁽³⁾	Clock Access Time	—	4.3	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	3.0	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	1.5	3.5	ns
t _{OEQ} ⁽³⁾	Output Enable to Output Valid	—	4.2	ns
t _{OEQX} ⁽¹⁾	Output Disable to Output Invalid	0	—	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	ns
t _{OEHZ} ^(1,2)	Output Disable to Output High-Z	2	3.5	ns
t _{AS} ⁽³⁾	Address Setup Time	2.0	—	ns
t _{SS} ⁽³⁾	Address Status Setup Time	1.5	—	ns
t _{CES} ⁽³⁾	Chip Enable Setup Time	2.0	—	ns
t _{AH} ⁽³⁾	Address Hold Time	1.0	—	ns
t _{SH} ⁽³⁾	Address Status Hold Time	1.0	—	ns
t _{CEH} ⁽³⁾	Chip Enable Hold Time	1.0	—	ns
t _{ZZS}	ZZ Standby	2	—	cyc
t _{ZZREC}	ZZ Recovery	2	—	cyc

Notes:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION

Temperature Range (A2): -40°C to +105°C

Speed	Order Part No.	Organization	Package
150 MHz	IS64LP12832-150TQA2	128Kx32	TQFP
	IS64LP12836-150TQA2	128Kx36	TQFP

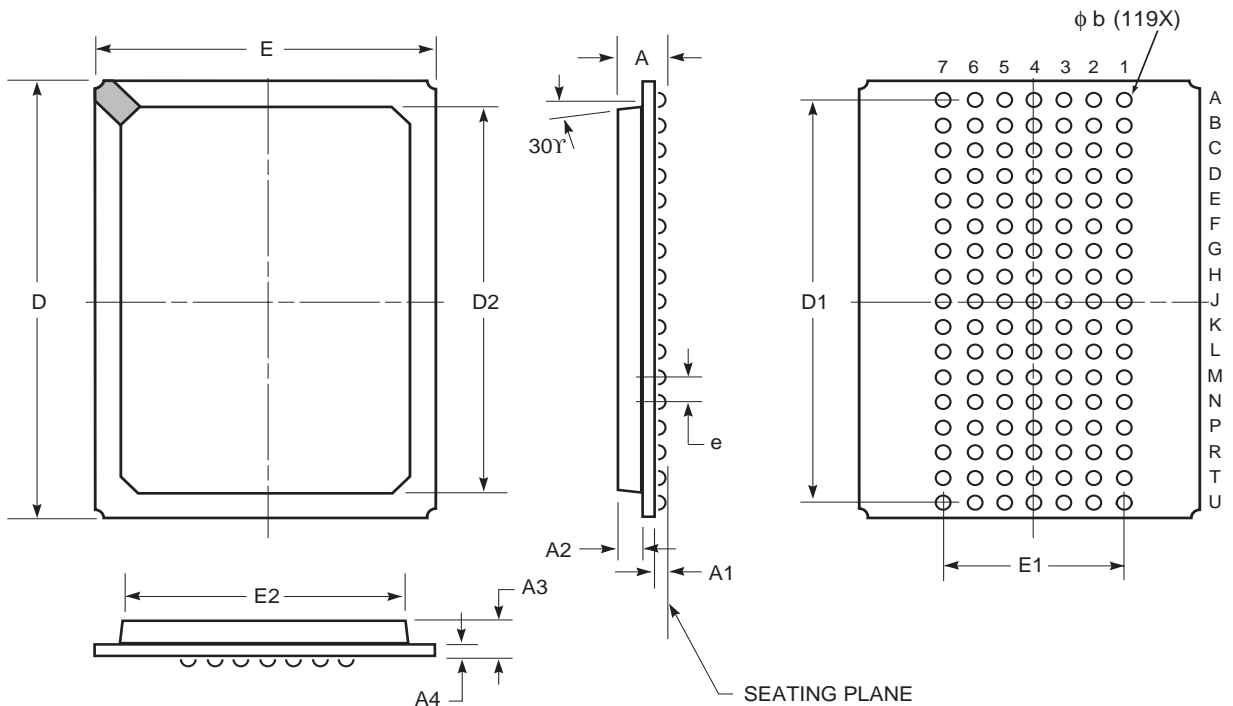
Temperature Range (A3): -40°C to +125°C

Speed	Order Part No.	Organization	Package
150 MHz	IS64LP12832-150TQA3	128Kx32	TQFP
	IS64LP12836-150TQA3	128Kx36	TQFP
	IS64LP12836-150BA3	128Kx36	PBGA

PACKAGING INFORMATION



Plastic Ball Grid Array Package Code: B (119-pin)



	MILLIMETERS		INCHES	
Sym.	Min.	Max.	Min.	Max.
N0. Leads	119			
A	—	2.41	—	0.095
A1	0.50	0.70	0.020	0.028
A2	0.80	1.00	0.032	0.039
A3	1.30	1.70	0.051	0.067
A4	0.56 BSC		0.022 BSC	
b	0.60	0.90	0.024	0.035
D	21.80	22.20	0.858	0.874
D1	20.32 BSC		0.800 BSC	
D2	19.40	19.60	0.764	0.772
E	13.80	14.20	0.543	0.559
E1	7.62 BSC		0.300 BSC	
E2	11.90	12.10	0.469	0.476
e	1.27 BSC		0.050 BSC	

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC=Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusion and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

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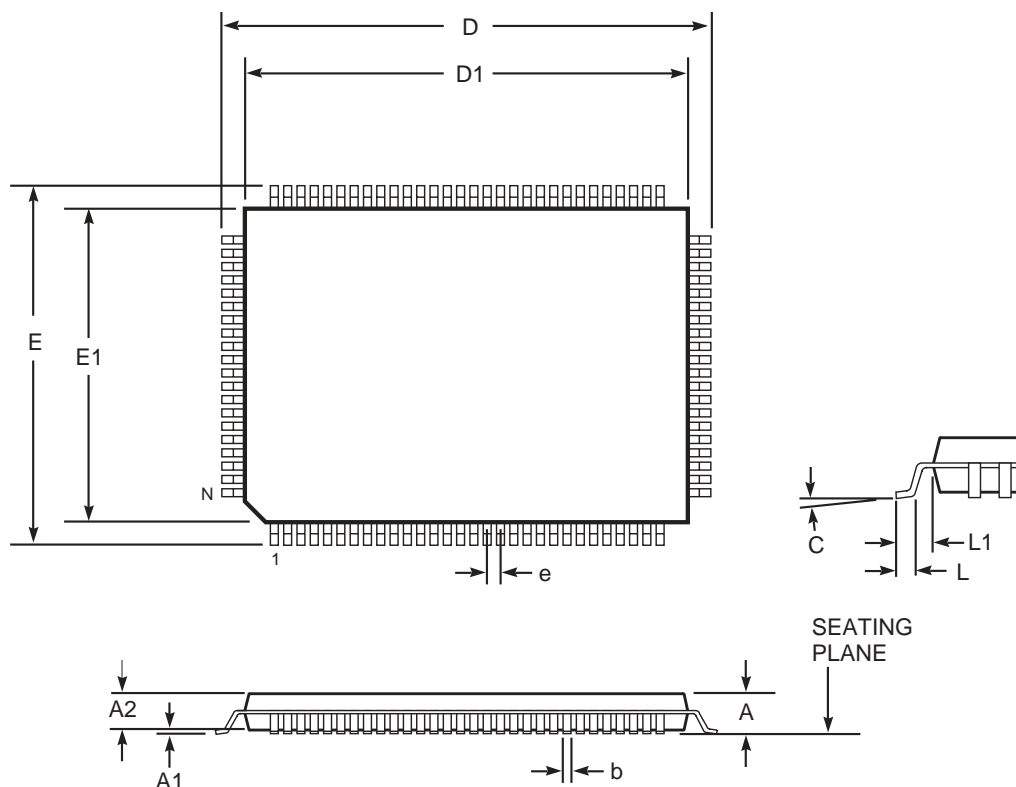
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Rev. B
02/12/03

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)

Package Code: TQ



Thin Quad Flat Pack (TQ)									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
Ref. Std.									
No. Leads (N)	100				128				
A	—	1.60	—	0.063	—	1.60	—	0.063	
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	
A2	1.35	1.45	0.053	0.057	1.35	1.45	0.053	0.057	
b	0.22	0.38	0.009	0.015	0.17	0.27	0.007	0.011	
D	21.90	22.10	0.862	0.870	21.80	22.20	0.858	0.874	
D1	19.90	20.10	0.783	0.791	19.90	20.10	0.783	0.791	
E	15.90	16.10	0.626	0.634	15.80	16.20	0.622	0.638	
E1	13.90	14.10	0.547	0.555	13.90	14.10	0.547	0.555	
e	0.65 BSC		0.026 BSC		0.50 BSC		0.020 BSC		
L	0.45	0.75	0.018	0.030	0.45	0.75	0.018	0.030	
L1	1.00 REF.		0.039 REF.		1.00 REF.		0.039 REF.		
C	0°	7°	0°	7°	0°	7°	0°	7°	

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.