**UCC1588/-1**
**UCC2588/-1**
**UCC3588/-1**
**ADVANCED INFORMATION**

# 5-Bit Programmable Output BiCMOS Power Supply Controller

## FEATURES

- 5-Bit Digital-to-Analog Converter (DAC) supports Intel Pentium II™
- Microprocessor VID Codes
- Compatible with 5V or 12V Systems
- 1% Output Voltage Accuracy Guaranteed
- Drives 2 N-Channel MOSFETs
- Programmable Frequency to 800kHz
- Power Good OV / UV / OVP Voltage Monitor
- Undervoltage Lockout and Softstart Functions
- Short Circuit Protection
- Low Impedance MOSFET Drivers
- Chip Disable

## DESCRIPTION

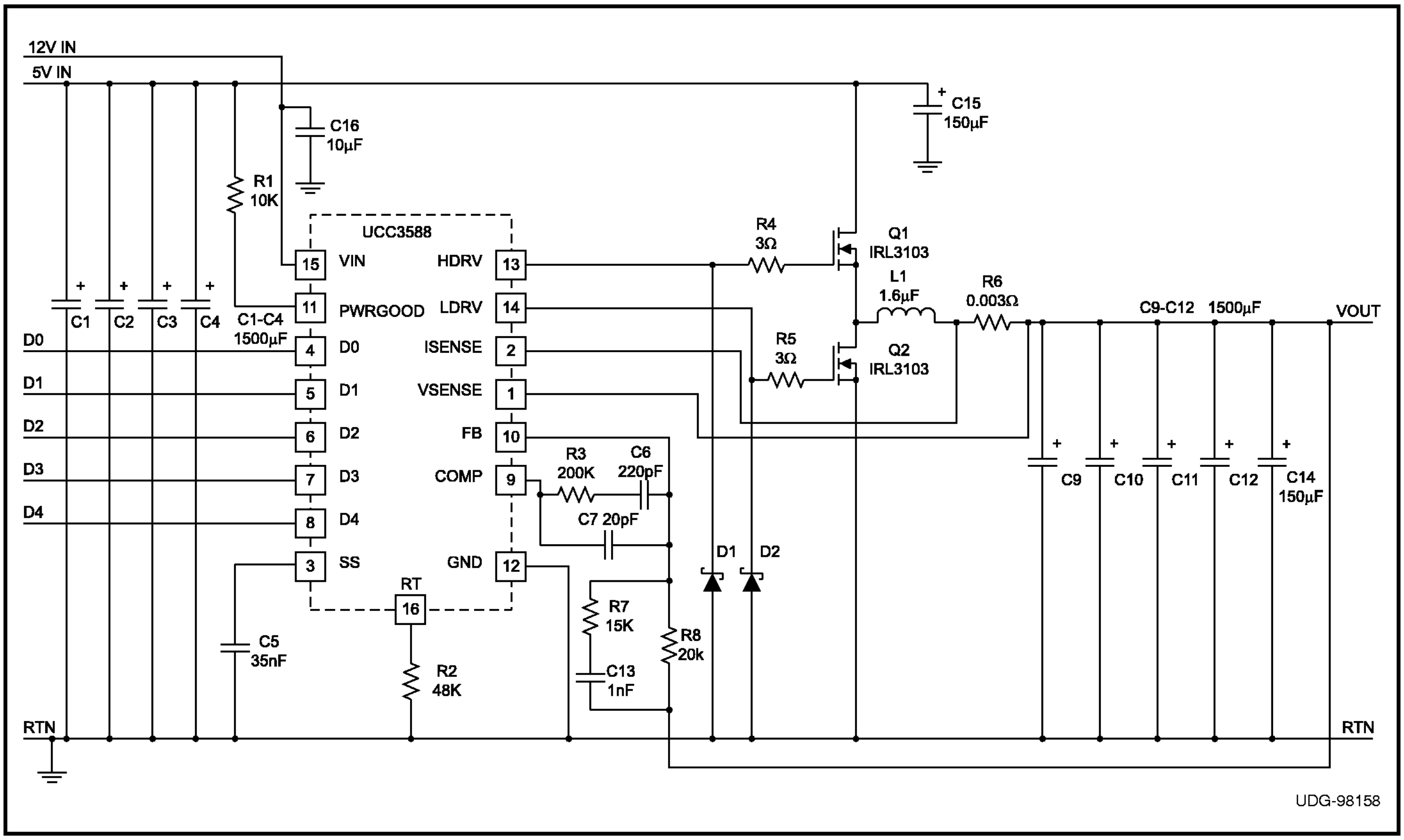
The UCC1588 synchronous step-down (Buck) regulator provides accurate high efficiency power conversion. Using few external components, the UCC1588 converts 5V to an adjustable output ranging from 3.5VDC to 2.1VDC in 100mV steps and 2.05VDC to 1.8VDC in 50mV steps (1.75VDC to 1.3VDC in 50mV steps, –1 only) with 1% DC system accuracy. A high level of integration and novel design allow this 16-pin controller to provide a complete control solution for todays demanding microcontroller power requirements. Typical applications include on board or VRM based power conversion for Intel Pentium II™ microprocessors, as well as other processors from a variety of manufacturers. High efficiency is obtained through the use of synchronous rectification.

The softstart function provides a controlled ramp up of the system output voltage. Overcurrent circuitry detects a hard (or soft) short on the system output voltage and invokes a timed softstart/shutdown cycle to reduce the PWM controller on time to 5%.

The oscillator frequency is externally programmed with RT and operates over a range of 50kHz to 800kHz. The gate drivers are low impedance to-tem pole output stages capable of driving large external MOSFETs. Cross conduction is eliminated by fixed delay times between turn off and turn on of the external high side and synchronous MOSFETs. The chip includes undervoltage lockout circuitry which assures the correct logic states at the outputs during power up and power down.

(continued)

## APPLICATION DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15V
Gate Drive Current, 50% Duty Cycle . . . . . . . . . . . . . . . . . . 1A
Input Voltage, $V_{SENSE}$, $V_{FB}$, SS, COMMAND, COMP . . . . . 5V
Input Voltage, D0, D1, D2, D3, D4 . . . . . . . . . . . . . . . . . . 6V
Input Current, RT, COMP . . . . . . . . . . . . . . . . . . . . . . . . 5mA

*Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.*

## THERMAL DATA

Plastic DIP Package
Thermal Resistance Junction to Leads, θjc . . . . . . . . 45°C/W
Thermal Resistance Junction to Ambient, θja . . . . . . 90°C/W
Ceramic DIP Package
Thermal Resistance Junction to Leads, θjc . . . . . . . . 28°C/W
Thermal Resistance Junction to Ambient, θja . . . . . 120°C/W
Standard Surface Mount Package
Thermal Resistance Junction to Leads, θjc . . . . . . . . 35°C/W
Thermal Resistance Junction to Ambient, θja . . . . . 120°C/W

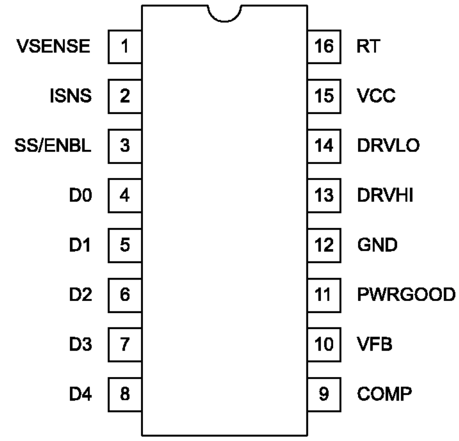
***Note:*** *The above numbers for θja and θjc are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device and PC-board system. All of the above numbers assume no ambient airflow, see the packaging section of Unitrode Product Data Handbook for more details.*

## DESCRIPTION (cont.)

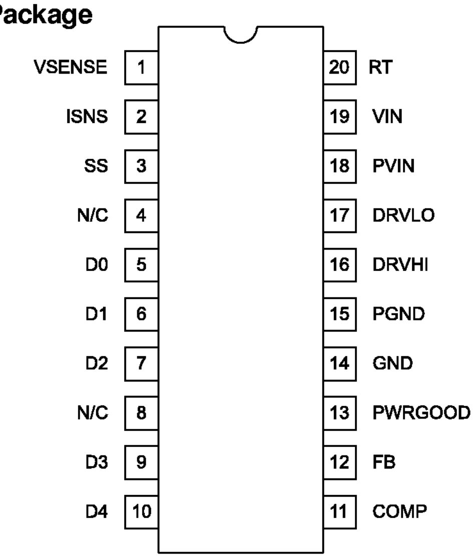
This device is available in 16- pin surface mount, plastic and ceramic DIP, TSSOP packages, and 20 pin surface mount. The UCC1588 is specified for operation from –55°C to +125°C, the UCC2588 is specified for operation from –25°C to +85°C, and the UCC3588 is specified for operation from 0°C to +70°C.

## CONNECTION DIAGRAMS

**DIP-16, SOIC-16, TSSOP-16 (TOP VIEW)**
**N, J, D and PW Packages**




**SOIC-20 (TOP VIEW)**
**DW Package**




**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications hold for $T_A$ = 0°C to 70°C for the UCC3588, –25°C to +85°C for the UCC2588, and –55°C to +125°C for the UCC1588, $T_A = T_J$. $V_{CC}$ = 12V, RT = 49k.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Supply Current Section** | | | | | |
| Supply Current, On | $V_{CC}$ = 12V | | 4.5 | | mA |
| **UVLO Section** | | | | | |
| VCC UVLO Turn-On Threshold | | | 10.5 | 10.80 | V |
| UVLO Threshold Hysteresis | | | 500 | | mV |
| **Voltage Error Amplifier Section** | | | | | |
| Input Bias Current | $V_{CM}$ = 2.0V | | –0.02 | 0 | µA |
| Open Loop Gain | 0.6 < $V_{COMP}$ < 2.5 | | 90 | | dB |
| Output Voltage High | $I_{COMP}$ = –500µA | | 3.4 | | V |
| Output Voltage Low | $I_{COMP}$ = +500µA | | 0.2 | 0.5 | V |
| Output Source Current | $V_{VFB}$ = 2V, $V_{COMMAND}$ = $V_{COMP}$ = 2.5V | | –500 | | µA |
| Output Sink Current | $V_{VFB}$ = 3V, $V_{COMMAND}$ = $V_{COMP}$ = 2.5V | | 10 | | mA |

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications hold for $T_A$ = 0°C to 70°C for the UCC3588, –25°C to +85°C for the UCC2588, and –55°C to +125°C for the UCC1588, $T_A$ = $T_J$. $V_{CC}$ = 12V, RT = 49k.

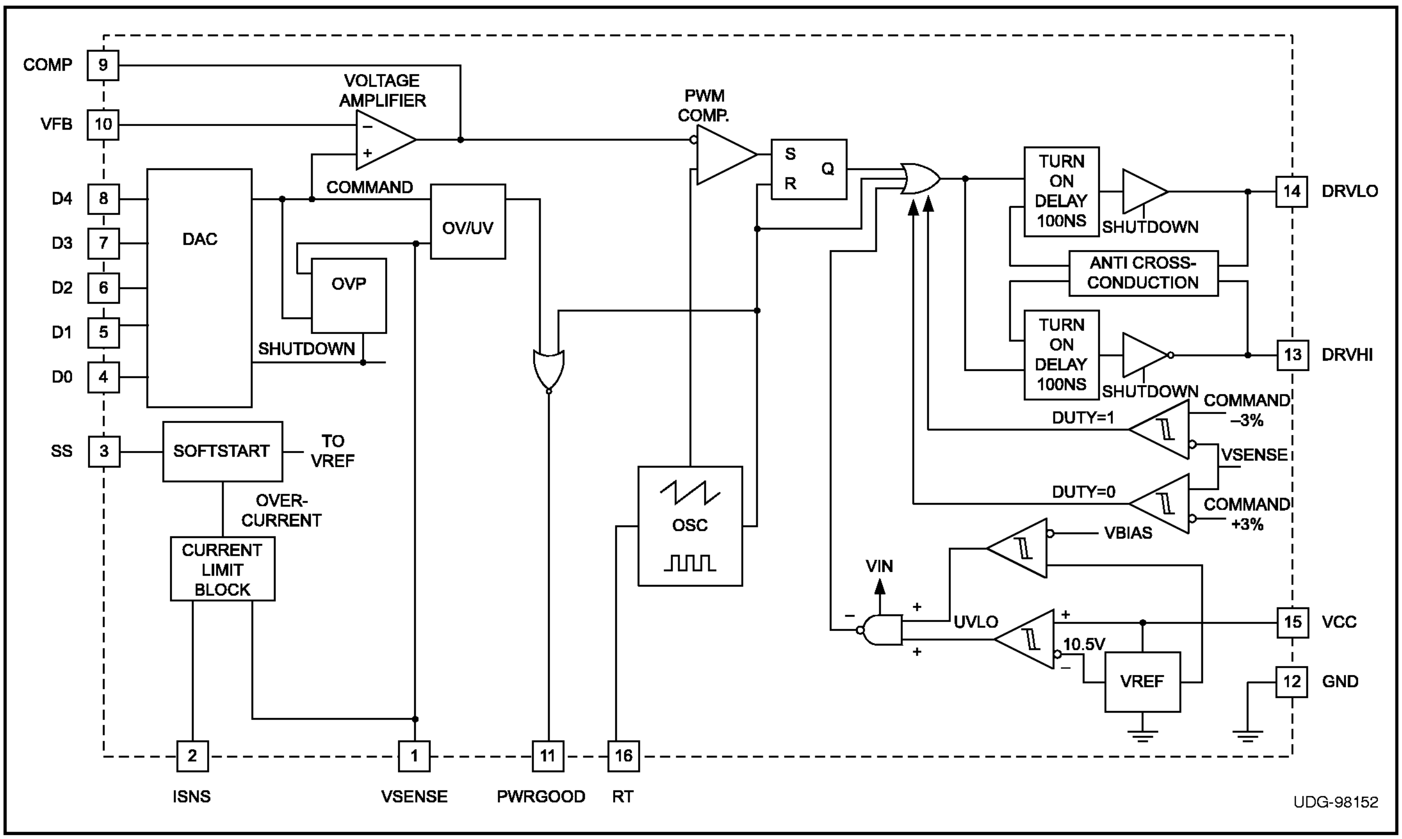
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Oscillator/PWM Section** | | | | | |
| Initial Accuracy | $T_A$ = 25°C | 240 | 300 | 360 | kHz |
| | 0°C < $T_A$ < 70°C | 220 | 300 | 380 | kHz |
| | –25°C < $T_A$ < 85°C | 210 | 300 | 390 | kHz |
| | –55°C < $T_A$ < 150°C | 200 | 300 | 400 | kHz |
| Voltage Stability | $V_{CC}$ = 10.8V to 13.2V | | 1 | | % |
| Ramp Amplitude (p–p) | | | 1.85 | | V |
| Ramp Valley Voltage | | | 0.65 | | V |
| PWM Max Duty Cycle | COMP = 3V | | 95 | | % |
| PWM Min Duty Cycle | COMP = 0. 3V | | 0 | | % |
| PWM Delay to Outputs (High to Low) | COMP = 1.5V | | 150 | | ns |
| PWM Delay to Outputs (Low to High) | COMP = 1.5V | | 150 | | ns |
| **Transient Window Comparator Section** | | | | | |
| Detection Range High (Duty Cycle = 0) | % Over $V_{COMMAND}$, (Note 1) | 1 | 3 | 5 | % |
| Detection Range Low (Duty Cycle = 1) | % Under $V_{COMMAND}$, (Note 1) | –1 | –3 | –5 | % |
| Propogation Delay ($V_{SENSE}$ to Outputs) | | | 150 | | nS |
| **Soft Start/ Shutdown Section** | | | | | |
| SS Charge Current (Normal Start Up) | Measured on SS | | –10 | | μA |
| SS Charge Current (Short Circuit Fault Condition) | Measured on SS | | –100 | | μA |
| SS Discharge Current (During Timeout Sequence) | Measured on SS | | 2.5 | | μA |
| Shutdown Threshold | Measured on SS | | 4.2 | | V |
| Restart Threshold | Measured on SS | 0.4 | 0.5 | | V |
| Soft Start Complete Threshold (Normal Start-Up) | Measured on SS | | 3.7 | | V |
| **DAC / Reference Section** | | | | | |
| COMMAND Voltage Accuracy | 10.8V < $V_{IN}$ < 13.2V, measured on COMP, 0°C < $T_A$ < +70°C, (Note 2) | –1.00 | | 1.00 | % |
| | 10.8V < $V_{IN}$ < 13.2V, measured on COMP, –25°C < $T_A$ < +85°C, (Note 2) | –1.10 | | 1.10 | % |
| D0–D4 Voltage High | | | 6 | | V |
| D0–D4 Voltage Threshold | | | 3 | | V |
| D0–D4 Voltage Input Bias Current | V(D4,...,D0) < 0.5V | | –90 | –20 | μA |
| **Overvoltage Comparator Section** | | | | | |
| Trip Point | % Over $V_{COMMAND}$, (Note 1) | 5.00 | 8.60 | 12.00 | % |
| Hysteresis | | 10 | 20 | 30 | mV |
| **Undervoltage Comparator Section** | | | | | |
| Trip Point | % Under $V_{COMMAND}$, (Note 1) | –12.00 | –8.60 | –5.00 | % |
| Hysteresis | | 10 | 20 | 30 | mV |
| **PWRGOOD Signal Section** | | | | | |
| Output Impedance | $V_{IN}$ = 12V, $I_{PWRGOOD}$ = 1mA | | | 470 | Ω |
| **Overvoltage Protection Section** | | | | | |
| Trip Point | % Over $V_{COMMAND}$, (Note 1) | 10 | 17.50 | 25.00 | % |
| Hysteresis | | | 20 | 30 | mV |
| VSENSE Input Bias Current | OV, OVP, UV Combined | | –10 | | μA |

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications hold for $T_A$ = 0°C to 70°C for the UCC3588, –25°C to +85°C for the UCC2588, and –55°C to +125°C for the UCC1588, $T_A$ = $T_J$. $V_{CC}$ = 12V, RT = 49k.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Gate Drivers (DRVHI, DRVLO) Section** | | | | | |
| Output High Voltage | $I_{GATE}$ = 100mA, $V_{IN}$ = 12V | | 11.5 | | V |
| Output Low Voltage | $I_{GATE}$ =– 100mA, $V_{IN}$ = 12V | | 0.5 | | V |
| Driver Non-overlap Time (DRVHI– to DRVLO+) | (Note 3) | | 100 | | nS |
| Driver Non-overlap Time (DRVLO– to DRVHI+) | (Note 3) | | 50 | | nS |
| Driver Rise Time (3nF Capacitive Load) | | | 80 | | nS |
| Driver Fall Time (3nF Capacitive Load) | | | 80 | | nS |
| **Current Limit Section** | | | | | |
| Current Limit Detect to Softstart Quick Charge | $V_{ISNS}$ = $V_{SENSE}$ + 75mV | | 170 | | nS |
| Start of Quick Charge to Shutdown Threshold | $V_{ISNS}$ = $V_{SENSE}$ + 75mV, $C_{SS}$ = 10nF, (Note 4) | | 1.6 | | µS |
| Current Limit Threshold Voltage | $V_{THRESHOLD}$ = $V_{ISNS}$ – $V_{VSENSE}$ | 50 | 54 | 58 | mV |
| ISNS Input Bias Current | | | –10 | | µA |

***Note 1:*** *This percentage is measured with respect to the ideal command voltage programmed by the $V_{ID}$ (D0 to D4) pins and applies to all DAC codes from 1.8 to 3.5V.*
***Note 2:*** *Reference and error amplifier offset trimmed while the voltage amp is set in unity gain mode.*
***Note 3:*** *Deadtime delay is measured from the 50% point of DRVHI falling to the 50% point of DRVLO rising, and vice-verse.*
***Note 4:*** *This time is dependent on the value of $C_{SS}$.*

## BLOCK DIAGRAM



## PIN DESCRIPTION

**COMP:** (Voltage Amplifier Output) The system voltage compensation network is applied between COMP and VFB.

**D0, D1, D2, D3, D4:** These are the digital input control codes for the DAC. The DAC is comprised of two ranges set by D4, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected the pin to GND; a bit is set high by floating the pin. Each control pin is pulled up to approximately 6V by an internal pull-up. If one of the low voltage codes is commanded on the DAC inputs, the outputs will be disabled. The outputs will also be disabled for all 1's, the NO CPU command.

**DRVHI:** (PWM Output, MOSFET Driver) This output provides a low Impedance totem pole driver. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot. Minimize circuit trace length to prevent DRVHI from ringing below GND. DRVHI is disabled during UVLO conditions. DRVHI has a typical output impedance of 5Ω for a $V_{IN}$ voltage of 12V.

**DRVLO:** (synchronous rectifier output, MOSFET driver) This output provides a low Impedance totem pole driver to drive the low-side synchronous external MOSFET. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot. Minimize circuit trace length to prevent DRVLO from ringing below GND. DRVLO is disabled during UVLO conditions. DRVLO has a typical output impedance of 5Ω for a $V_{IN}$ voltage of 12V. Please see the "Typical Curves" section to determine the driver output impedance as a function of $V_{IN}$ Voltage.

**GND:** (Ground) All voltages measured with respect to ground. Vcc should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing to GND should be as short and direct as possible.

**ISNS:** (Current Limit Sense Input) A resistance connected between this sense connection and Vsense sets up the current limit threshold (54mV typical voltage threshold).

**PWRGOOD:** This pin is an open drain output which is driven low to reset the microprocessor when VSNS rises above or falls below its nominal value by 8.5%(typ). The on resistance of the open-drain switch is no higher than 470Ω. This output should be pulled up to a logic level voltage and should be programmed to sink 1mA or less.

**RT:** (Oscillator Charging Current) This pin is a low impedance voltage source set at ~1.25V. A resistor from RT to GND is used to program the internal PWM oscillator frequency. The equation for $R_T$ follows:

$$R_T = \left(\frac{1}{(f \bullet 67.2pF)}\right) - 800 \quad (1)$$

**SS/SD:** (Soft Start/Shut Down) A low leakage capacitor connected between SS and GND will provide a softstart function for the converter. The voltage on this capacitor will slowly charge on start-up via an internal current source (10µA typ.) and ultimately clamp at approximately 3.7V. The output of the voltage error amplifier (COMP) tracks this voltage thereby limiting the controller duty ratio. If a short circuit is detected, the clamp is released and the cap on SS charges with a 100µA (typ) current source. If the SS voltage exceeds 4.2V, the converter shuts down, and the 100µA current source is switched off. The SS cap will then be discharged with a 2.5µA (typ) current sink. When the voltage on SS falls below 0.5V, a new SS cycle is started. The equation for softstart time follows:

$$T_{SS} = 3.7\left(\frac{C_{SS}}{10\mu A}\right). \quad (2)$$

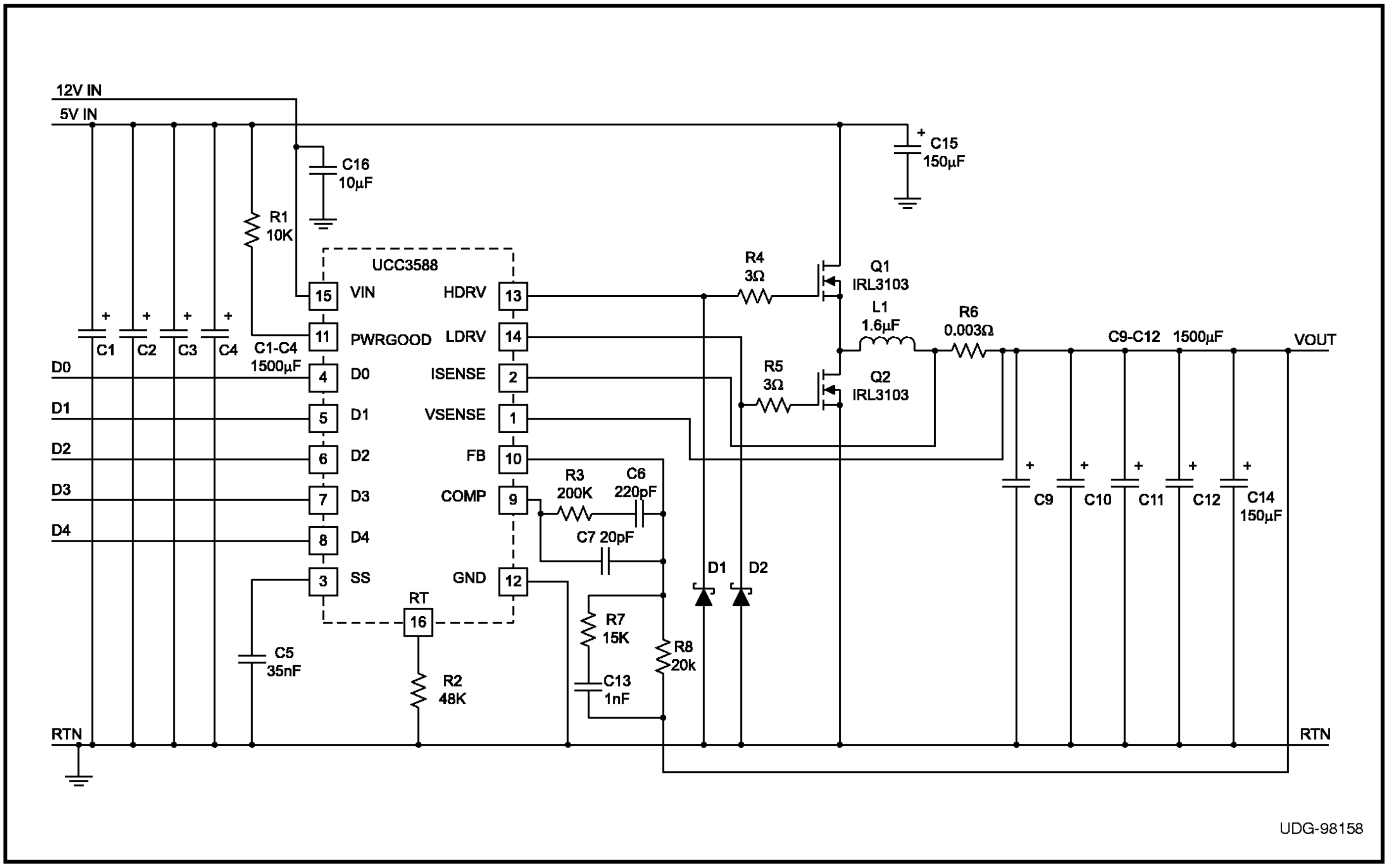
Shutdown is accomplished by pulling SS/SD below 0.5V.

**VCC:** (Positive Supply Voltage) This pin is normally connected to a 12V ±10% system voltage. The UCC1588 will commence normal operation when the voltage on VCC exceeds 10.5V (typ). Bypass $V_{CC}$ directly to GND with a 0.1µF (minimum) ceramic capacitor to supply current spikes required to charge external MOSFET gate capacitances.

**VFB:** (Voltage Amplifier Inverting Input) This is normally connected to a compensation network and to the power converter output through a divider network.

**VSENSE:** (Direct Output Voltage Connection) This pin is a direct kelvin connection to the output voltage used for over voltage, under voltage, and current sensing.

## APPLICATION DIAGRAM




## APPLICATION INFORMATION

Figure 1 shows a synchronous regulator using the UCC3588. It accepts +5V and +12V as input, and delivers a regulated DC output voltage. The value of the output voltage is programmable via a 5-bit DAC code to a value between 1.8Vand 3.5V. The example given here is for a 12A regulator, running from a 10% tolerance source, and operating at 300kHz.

The design of the power stage is straightforward buck regulator design. Assuming an output noise requirement of 50mV, and an output ripple current of 20% of full load, the value of the output inductor should be calculated at the highest input voltage and lowest output voltage that the regulator is likely to see. This insures that the ripple current will decrease as the input voltage and output voltage differential decreases. The minimum duty cycle, $\delta_{min}$, should also be calculated under this condition.

1) The current sense resistor is chosen to allow current limit to occur at 1.4 times the full load current.

$$R6 = \frac{V_{TRIP}}{(1.4 \bullet I_{OUT})} = \frac{50mV}{16.8A} = 3m\Omega \quad (3)$$

2) To properly approximate the full load duty cycle operating range, assumptions are made regarding the MOSFETs' $Rds_{ON}$, and the output inductor's DC resistance. Q1 and Q2 are IRF3103s, each with an $Rds_{ON}$ of 0.014Ω. The output inductor is allowed to dissipate one watt under full load, giving a DC resistance of 6.9mΩ, and R6 is 3mΩ. The resulting duty cycle at the operating extremes is then:

$$\delta_{min} = \frac{V_{OUT(lo)} + I_{OUT} \bullet (R6 + Rds_{ON} + R\ell)}{V_{IN(hi)}} \quad (4)$$

$$= \frac{1.8 + (12 \bullet 0.024)}{5.5} = 0.379$$

$$\delta_{max} = \frac{V_{OUT(hi)} + I_{OUT} \bullet (R6 + Rds_{ON} + R\ell)}{V_{IN(lo)}} \quad (5)$$

$$= \frac{3.5 + (12 \bullet 0.024)}{4.5} = 0.842$$

3) The value of the output inductor is chosen at the worst case ripple current point.

## APPLICATION INFORMATION (cont.)

$$L = \frac{V_{IN(hi)} - V_{OUT(lo)} \bullet \delta_{min} T_S}{\Delta I_{OUT}} \quad (6)$$

$$= \frac{(5.5 - 1.8) \bullet 0.379 \bullet 3.333\mu}{2.4} = 1.9\mu H$$

Four turns of #16 on a micrometals T51-52C core has an inductance of 1.9µH, has a DC resistance of 6.6mΩ, and will dissipate about 1W under full load conditions. With an output inductor value of 1.9µH, the ripple current will be 1750mA under the low-input-high-output condition.

4) To meet the output noise voltage requirement, the output capacitor(s) must be chosen so that the ripple voltage induced across the ESR of the capacitors by the output ripple current is less than 50mv.

$$ESR < \frac{50mV}{\Delta I_{OUT}} = 42m\Omega \quad (7)$$

Additionally, to meet output load transient response requirements, the capacitors' ESL and ESR must be low enough to avoid excessive voltage transient spikes. (See Application Note U-157 for a discussion of how to determine the amount and type of load capacitance.) For this example, four Sanyo MV-GX 1500µf, 6.3 V capacitors will be used. The ESR of each capacitor is approximately 44mΩ so the parallel combination of four results in an equivalent ESR of 11mΩ.

5) Q1 and Q2 are chosen to be IRF3103 N-Channel MOSFETs. Each MOSFET has an $Rds_{ON}$ of approximately 0.014Ω, a gate charge requirement of 50nC, and a turn OFF time of approximately 54ns.

To calculate the losses in the upper MOSFET, Q1, first calculate the RMS current it will be conducting.

$$I(Q1_{RMS}) = \sqrt{\delta\left(I_{OUT}^2 + \frac{\Delta I_{OUT}^2}{12}\right)} \quad (8)$$

Notice that with a higher output voltage, the duty cycle increases, and therefore so does the RMS current. Any heat sink design should take into account the worst case power dissipation the device will experience.

With the highest programmable output voltage of 3.5 volts and the lowest possible input voltage of 4.5V, the RMS current Q1 will conduct is 10.5 amps, and the conduction loss is

$$P_{CON}\,Q1 = \left(I_{Q1_{RMS}}\right)^2 \bullet Rds_{ON} = 1.5W \quad (9)$$

Next, the gate drive losses are found.

$$P_{GATE}\,Q1 = Q_G \bullet V_{IN(hi)} \bullet F_S = 0.08W \quad (10)$$

And the Turn OFF losses are estimated as

$$P_{T(OFF)}Q1 = \tfrac{1}{2} V_{IN(hi)} \bullet I_{D(pk)} \bullet tf \bullet F_S = 0.56W \quad (11)$$

The total loss in Q1is the sum of the three components, or about 2.1 watts.

The gate drive losses in Q2 will be the same as in Q1, but the turn OFF losses will be associated with the reverse recovery of the body diode, instead of the turn OFF of the channel. This is due to the UCC3588's delay built into the switching of the upper and lower MOSFET's drive. For example, when Q1 is turned OFF, the turn ON of Q2 is delayed for about 100ns, insuring that the circuit has time to commutate and that current has begun to flow in the body diode of Q2. When Q2 is turned OFF, current is diverted from the channel of Q2 into the body diode of Q2, resulting in virtually no power dissipation. When Q1 is turned ON 100ns later however, the circuit is forced to commutate again. This time causing reverse recovery loss in the body diode of Q2 as its polarity is reversed. The loss in the diode is expressed as:

$$P_{RR}Q2 = \tfrac{1}{2} \bullet Q_{RR} \bullet V_{IN(hi)} \bullet F_S = 0.26W \quad (12)$$

Where $Q_{RR}$, the reverse recovery of the body diode, is 310nC.

100ns before the turn ON of Q2, and 100ns after the turn OFF of Q2, current flows through Q2's intrinsic body diode. The power dissipation during this interval is:

$$P_{COM}Q2_{DIODE} = \quad (13)$$

$$I_{OUT} \bullet V_{DIODE} \bullet \frac{200ns}{3.33\mu s} = 12 \bullet 1.4 \bullet 0.06 = 1W$$

During the ON period of Q2, current flows through the $Rds_{ON}$ of the device. Where the highest RMS current in Q1 was at the low-input-and-high-output condition, the highest RMS current in Q2 is found when the input is at its highest, and the output is at its lowest. The equation for the RMS current in Q2 is:

$$I(Q2_{RMS}) = \quad (14)$$

$$\sqrt{\left(1 - \delta_{min} - \frac{200ns}{3.33\mu s}\right) \bullet \left(I_{OUT}^2 + \frac{\Delta I_{OUT}^2}{12}\right)} = 8.7A$$

$$P_{CON}Q2 = I\left(Q2_{RMS}^2\right) \bullet Rds_{ON} = 1.06W \quad (15)$$

The worst case loss in Q2 comes to about 2.4 watts.

6) Repeating the preceding procedure for various input and output voltage combinations yields a table of operating conditions.

## APPLICATION INFORMATION (cont.)

***Table 1. Regulator Operating Conditions***

| | $V_{IN}$= 4.5 | 5.0 | 5.5 |
|---|---|---|---|
| **$V_{OUT}$=3.5** | | | |
| Pd Q1 | 2.2 | 2.1 | 2 |
| Pd Q2 | 1.5 | 1.6 | 1.8 |
| Pd L | 0.95 | 0.95 | 0.95 |
| Pd Total | 5.1 | 5.2 | 5.4 |
| Average Input | 10.50 | 9.5 | 8.70 |
| Duty Cycle | 0.84 | 0.76 | 0.69 |
| **$V_{OUT}$=1.8** | | | |
| Pd Q1 | 1.5 | 1.4 | 1.4 |
| Pd Q2 | 2.3 | 2.4 | 2.5 |
| Pd L | 0.95 | 0.95 | 0.95 |
| Pd Total | 5.2 | 5.3 | 5.4 |
| Average Input | 6.00 | 5.40 | 4.96 |
| Duty Cycle | 0.46 | 0.42 | 0.38 |

7) Assuming the converter's input current is DC, the remaining switching current drawn by Q1 must come from the input capacitors. The next step then, is to find the worst case RMS current the capacitors will experience. (Equation 16). Where $I_{IN}$(avg) is the average input current.

Repeating the above calculation over the operating range of the regulator (see Table 2.) reveals that the worst case capacitor ripple current is found at low input, and at low output voltage. A Sanyo MV-GX, 1500μF, 6.3V capacitor is rated to handle 1.25 amps at 105°C. Derating the design to 70°C allows the use of four capacitors, each one experiencing one fourth of the total ripple current.

***Table 2. Regulator Operating Conditions***

| | $V_{IN}$= 4.5 | 5.0 | 5.5 |
|---|---|---|---|
| **$V_{OUT}$= 3.5** | | | |
| Total Input Cap RMS Current | 4.4 | 5.2 | 5.6 |
| Total Input Cap Power Dissipation | 0.21 | 0.29 | 0.34 |
| Total Power Dissipation | 5.1 | 5.3 | 5.4 |
| Power Train Efficiency | 0.89 | 0.88 | 0.87 |
| **$V_{OUT}$=1.8** | | | |
| Total Input Cap RMS Current | 6 | 5.9 | 5.8 |
| Total Input Cap Power Dissipation | 0.39 | 0.39 | 0.37 |
| Total Power Dissipation | 5.2 | 5.3 | 5.4 |
| Power Train Efficiency | 0.81 | 0.8 | 0.8 |

8) The voltage feedback loop is next. The gain and frequency response of the PWM and LC filter is shown in Equation 17.

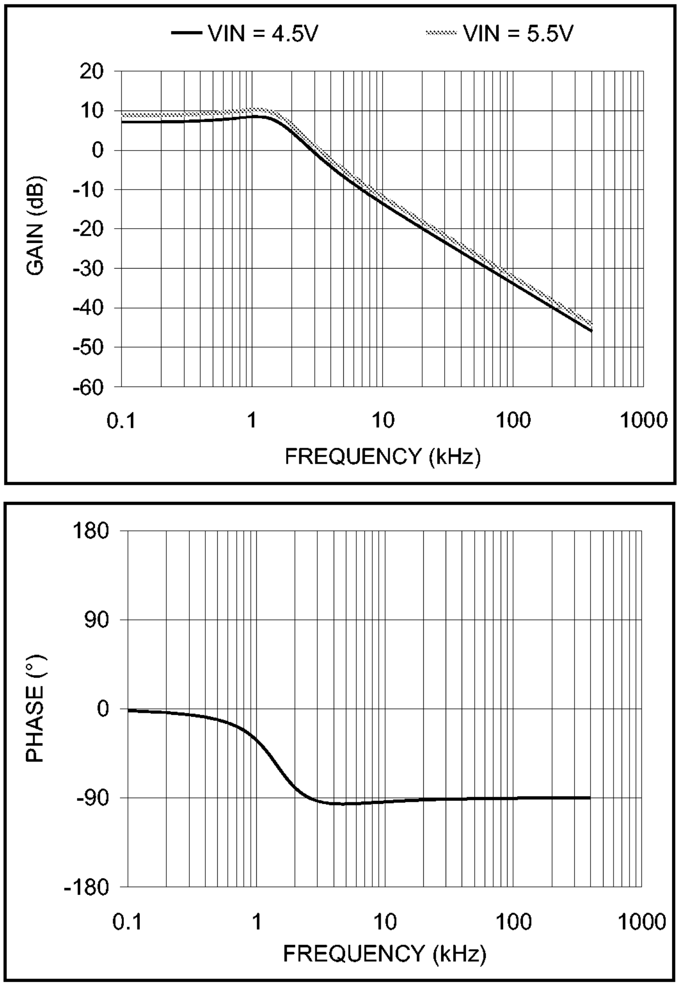



***Figure 1. Modulator Frequency Response***

To compensate the loop with as high a bandwidth as practical, additional gain is added to the loop with the voltage error amplifier.

$$I_{CAP_{RMS}} = \sqrt{\delta\left(\left(I_{OUT} - I_{IN\,avg}\right)^2 + \frac{\Delta I_{OUT}{}^2}{12}\right) + (1-\delta) \bullet \left(I_{IN\,avg}\right)^2} \tag{16}$$

$$K_{PWM}(f) = \frac{V_{IN}}{V_{RAMP}} = \frac{1 + 2\pi f \bullet R_{ESR} \bullet C_{OUT}}{1 - \left(4\pi^2 \bullet f^2 \bullet LC_{OUT}\right) + \left(\left(R6 + R\ell + R_{ESR}\right) \bullet C_{OUT} + \frac{L}{R_{LOAD}}\right)} \tag{17}$$

## APPLICATION INFORMATION (cont.)

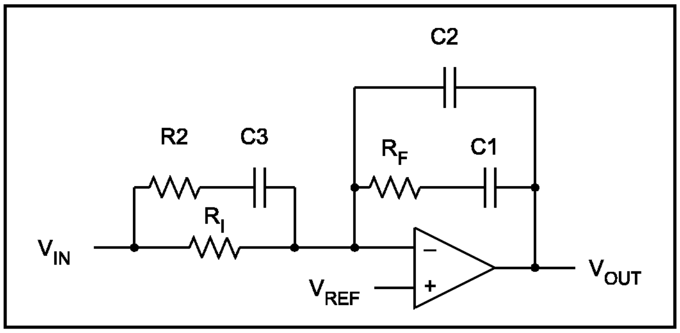



*Figure 3. Voltage error amplifier configuration.*

The equation for the gain of the voltage amplifier in this configuration is:

$$K_{EA} = \frac{\left(1+s\left(C1Rf\right)\right)\bullet\left(1+s\left(C3\left(R_I+R2\right)\right)\right)}{R_I\left(s^2C1C2Rf+s\left(C1+C2\right)\right)\bullet\left(1+s\left(C3R2\right)\right)} \qquad (18)$$

For good transient response, select the $R_F$-C1 zero at 5kHz. Add additional phase margin by placing the $R_I$-C3 zero also at 5kHz. To roll off the gain at high frequency, selece the R2-C3 pole to be at 10kHz, and the final C2-$R_F$ pole at 40kHz. Results are $R_I$=20k, $R_F$=200k, R2=15k, C1=220nf, C2=20pF, C3=1000pf. The Gain-Phase plots of the voltage error amplifier and the overall loop are plotted below.

9) The value of RT is given by:

$$RT = \left(\frac{1}{F_S \bullet 67.2pF}\right) - 800 = 48k\Omega \qquad (19)$$

10) The value of the soft start capacitor is given by:

$$C_{SS} = 10\mu \bullet \frac{t_{SS}}{3.7V} \qquad (20)$$

Where $t_{SS}$ is the desired soft start time.

To insure that soft start is long enough so that the converter does not enter current limit during startup, the minimum value of soft start may be determined by:

$$C_{SS} \geq \frac{C_{OUT} \bullet I_{CH}}{\left(\frac{V_{LIM}}{R_{SENSE}}\right) - I_{OUT}} \bullet \frac{V_{IN}}{V_{RAMP}} \qquad (21)$$

Where $C_{OUT}$ is the output capacitance, Ich is the soft start charging current (10µa typ), $V_{LIM}$ is the current limit trip voltage (54mV typ), $I_{OUT}$ is the load current, $V_{IN}$ is the 5V supply, and $V_{RAMP}$ is the internal oscillator ramp voltage (1.85V typ). For this example, $C_{SS}$ must be greater than 35nF, and the resulting soft start time will be 13ms.

11) The output of the regulator is adjustable by programming the following codes into the D0 - D4 pins according to the table below. To program a logic zero, ground the pin. To program a logic 1, then leave the pin floating. Do not tie the pin to an external voltage source.

12) A series resistor should be placed in series with the gate of each MOSFET to prevent excessive ringing due to parasitic effects. A value of 3Ω to 5Ω is usually sufficient in most cases. Additionally, to prevent pins 13 and 14 from ringing more than 0.5V below ground, a clamp schottky rectifier placed as close as possible to the IC is also recommended.

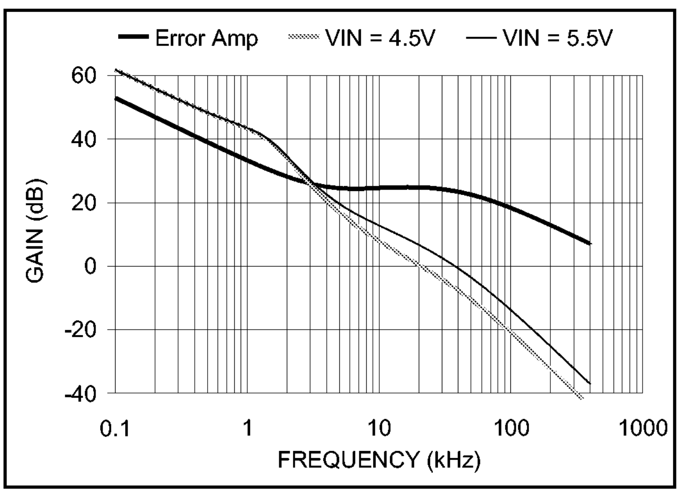



*Figure 4. Error amplifier and loop frequency response.*

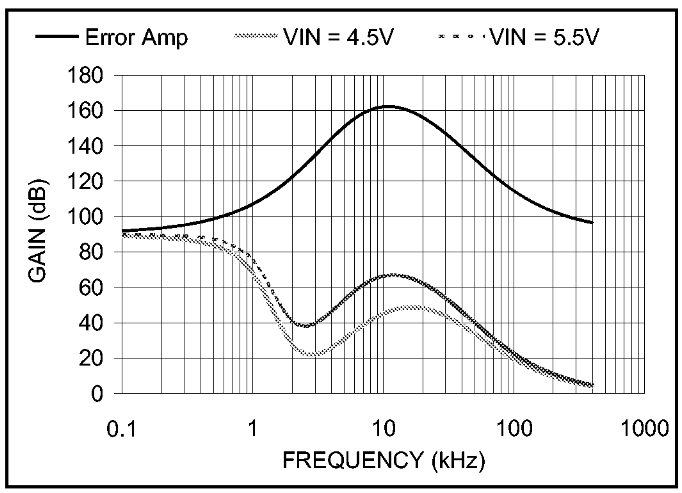



*Figure 5. Error amplifier and loop frequency response.*

## APPLICATION INFORMATION (cont.)

*Table 3.*
*VID Codes and Resulting Regulator Output Voltage*

| D4 | D3 | D2 | D1 | D0 | $V_{OUT}$ |
|---|---|---|---|---|---|
| **For -1 Parts Only** | | | | | |
| 0 | 1 | 1 | 1 | 1 | 1.3 |
| 0 | 1 | 1 | 1 | 0 | 1.35 |
| 0 | 1 | 1 | 0 | 1 | 1.4 |
| 0 | 1 | 1 | 0 | 0 | 1.45 |
| 0 | 1 | 0 | 1 | 1 | 1.5 |
| 0 | 1 | 0 | 1 | 0 | 1.55 |
| 0 | 1 | 0 | 0 | 1 | 1.6 |
| 0 | 1 | 0 | 0 | 0 | 1.65 |
| 0 | 0 | 1 | 1 | 1 | 1.7 |
| 0 | 0 | 1 | 1 | 0 | 1.75 |
| **For all parts** | | | | | |
| 0 | 0 | 1 | 0 | 1 | 1.8 |
| 0 | 0 | 1 | 0 | 0 | 1.85 |
| 0 | 0 | 0 | 1 | 1 | 1.9 |
| 0 | 0 | 0 | 1 | 0 | 1.95 |
| 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 2.05 |
| 1 | 1 | 1 | 1 | 1 | No outputs |
| 1 | 1 | 1 | 1 | 0 | 2.1 |
| 1 | 1 | 1 | 0 | 1 | 2.2 |
| 1 | 1 | 1 | 0 | 0 | 2.3 |
| 1 | 1 | 0 | 1 | 1 | 2.4 |
| 1 | 1 | 0 | 1 | 0 | 2.5 |
| 1 | 1 | 0 | 0 | 1 | 2.6 |
| 1 | 1 | 0 | 0 | 0 | 2.7 |
| 1 | 0 | 1 | 1 | 1 | 2.8 |
| 1 | 0 | 1 | 1 | 0 | 2.9 |
| 1 | 0 | 1 | 0 | 1 | 3 |
| 1 | 0 | 1 | 0 | 0 | 3.1 |
| 1 | 0 | 0 | 1 | 1 | 3.2 |
| 1 | 0 | 0 | 1 | 0 | 3.3 |
| 1 | 0 | 0 | 0 | 1 | 3.4 |

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## Mechanical Drawings

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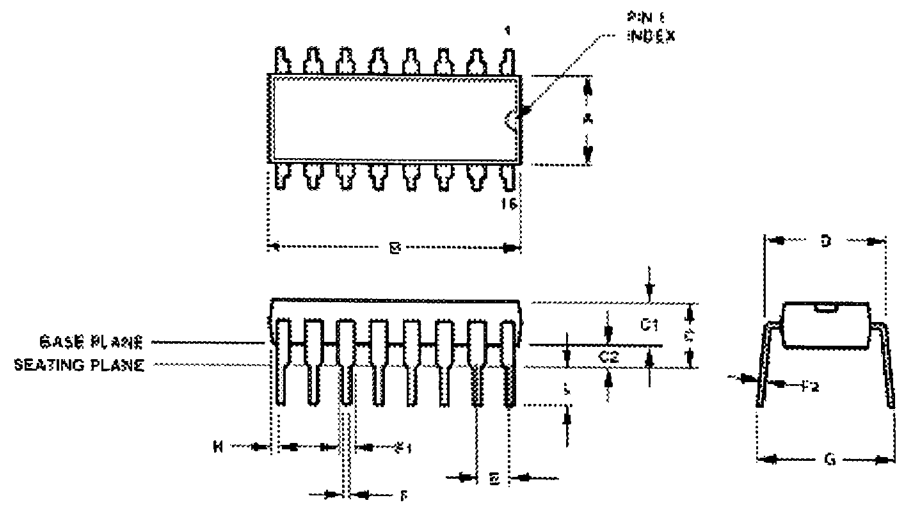
## 16-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

| DIMENSIONS | | | | | NOTES |
|---|---|---|---|---|---|
| | INCHES | | MILLIMETERS | | NOTES |
| | MIN | MAX | MIN | MAX | |
| A | .245 | .260 | 6.22 | 6.60 | 1 |
| B | .745 | .775 | 18.92 | 19.68 | 1 |
| C | - | .210 | - | 5.33 | |
| C1 | .125 | .150 | 3.18 | 3.81 | |
| C2 | .015 | .055 | 0.38 | 1.40 | 2 |
| D | .300 | .325 | 7.62 | 8.26 | 3 |
| E | .100 BSC | | 2.54 BSC | | 4 |
| F | .014 | .022 | 0.35 | 0.56 | |
| F1 | .045 | .070 | 1.14 | 1.78 | |
| F2 | .008 | .014 | 0.20 | 0.35 | |
| G | .300 | .400 | 7.62 | 10.16 | 5 |
| H | .005 | - | 0.13 | - | |
| L | .115 | .160 | 2.92 | 4.06 | |




**NOTES:**

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

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UNITRODE

Mechanical Drawings

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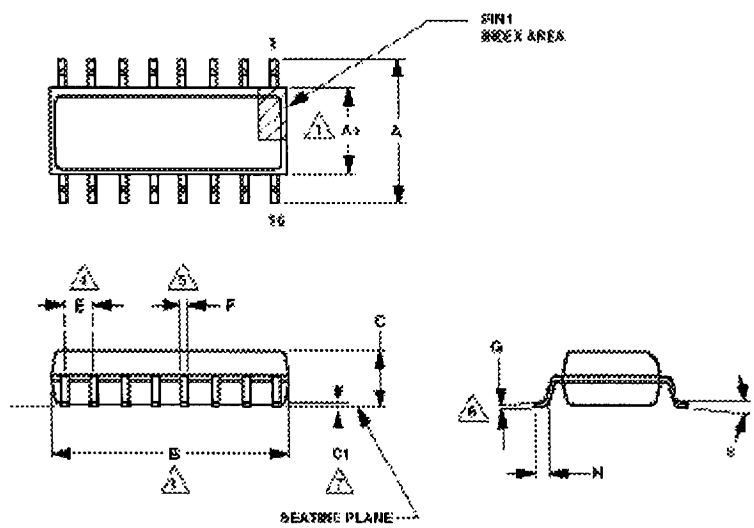
## 16-PIN SOIC SURFACE MOUNT~ D, DP, DS PACKAGE SUFFIX

| DIMENSIONS | | | | |
|---|---|---|---|---|
| | INCHES | | MILLIMETERS | |
| | MIN | MAX | MIN | MAX |
| A | .228 | .244 | 5.80 | 6.20 |
| A1 | .150 | .158 | 3.80 | 4.00 |
| B | .386 | .393 | 9.80 | 9.98 |
| C | .053 | .069 | 1.35 | 1.75 |
| C1 | .004 | .009 | 0.10 | 0.22 |
| E | .050 BSC | | 1.27 BSC | |
| F | .014 | .019 | 0.36 | 0.48 |
| G | .007 | .010 | 0.19 | 0.25 |
| H | .016 | .035 | 0.41 | 0.89 |
| θ | 0° | 8° | 0° | 8° |




**NOTES:**

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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Mechanical Drawings

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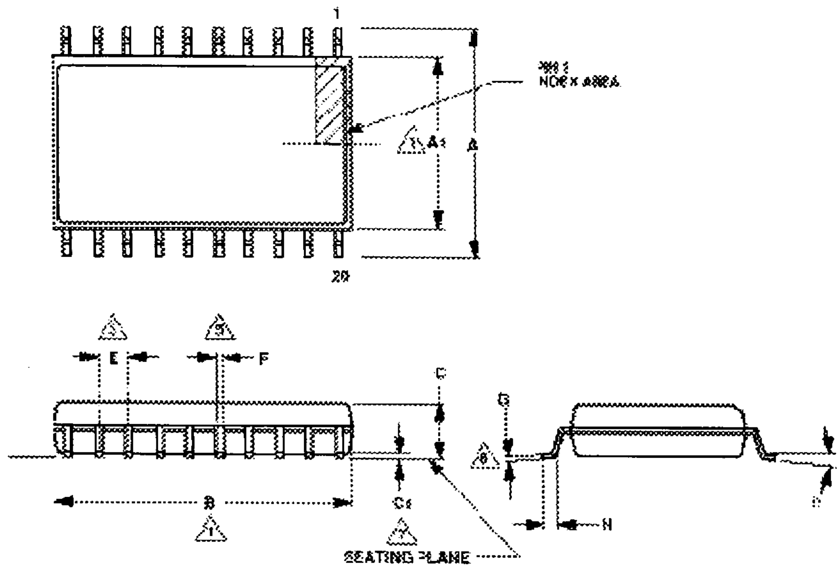
## 20-PIN SOIC SURFACE MOUNT~ DW PACKAGE SUFFIX

| DIMENSIONS | | | | |
|---|---|---|---|---|
| | INCHES | | MILLIMETERS | |
| | MIN | MAX | MIN | MAX |
| A | .394 | .419 | 10.00 | 10.64 |
| A1 | .292 | .299 | 7.42 | 7.59 |
| B | .504 | .511 | 12.80 | 12.98 |
| C | .097 | .104 | 2.46 | 2.64 |
| C1 | .004 | .011 | 0.10 | 0.28 |
| E | .050 BSC | | 1.27 BSC | |
| F | .014 | .019 | 0.36 | 0.48 |
| G | .009 | .012 | 0.23 | 0.30 |
| H | .018 | .035 | 0.46 | 0.89 |
| θ | 0° | 8° | 0° | 8° |




**NOTES:**

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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## Mechanical Drawings

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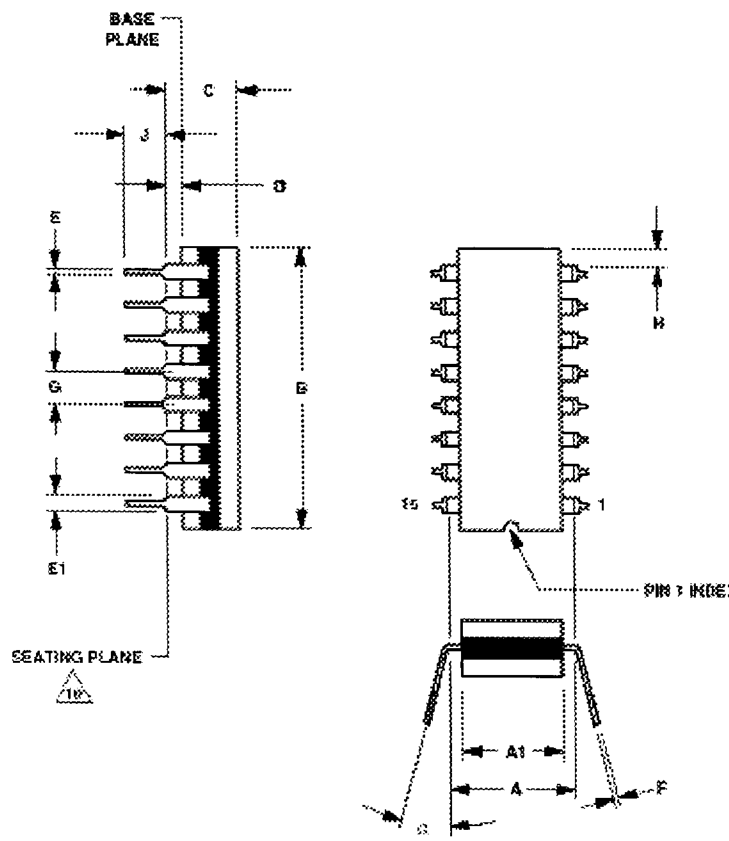
# 16-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

| | DIMENSIONS | | | | |
|---|---|---|---|---|---|
| | INCHES | | MILLIMETERS | | NOTES |
| | MIN | MAX | MIN | MAX | |
| A | 0.290 | 0.320 | 7.37 | 8.13 | 7 |
| A1 | 0.220 | 0.310 | 5.59 | 7.87 | 4 |
| B | - | 0.840 | - | 21.34 | 4 |
| C | - | 0.200 | - | 5.08 | |
| D | 0.015 | 0.060 | 0.38 | 1.52 | 3 |
| E | 0.014 | 0.026 | 0.36 | 0.66 | 8 |
| E1 | 0.045 | 0.065 | 1.14 | 1.65 | 2 |
| F | 0.008 | 0.018 | 0.20 | 0.46 | 8 |
| G | 0.100 BSC | | 2.54 BSC | | 5 |
| H | 0.005 | - | 0.13 | - | 6 |
| J | 0.125 | 0.200 | 3.18 | 5.08 | |
| α | 0° | 15° | 0° | 15° | |




**NOTES:**

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 8, 9 AND 16 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 8, 9 AND 16).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN α= 0°.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

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## Mechanical Drawings

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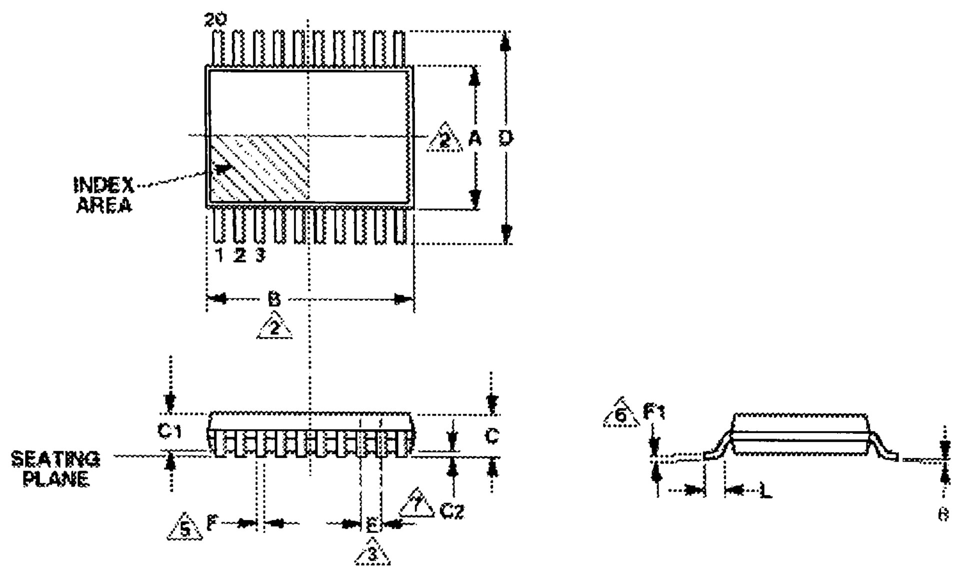
## 20-PIN TSSOP ~ PW PACKAGE SUFFIX

| DIMENSIONS | | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN | MAX | MIN | MAX |
| A | 4.30 | 4.48 | .169 | .176 |
| B | 6.40 | 6.60 | .252 | .260 |
| C | - | 1.10 | - | .043 |
| C1 | .90 REF | | .0354 REF | |
| C2 | .05 | .15 | .002 | .006 |
| D | 6.25 | 6.50 | .246 | .256 |
| E | .065 BSC | | .0256 BSC | |
| F | .18 | .30 | .007 | .012 |
| F1 | .09 | .18 | .003 | .007 |
| L | .50 | .70 | .020 | .028 |
| θ | 0° | 8° | 0° | 8° |




**NOTES:**

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. (△) 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. (△) THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. (△) DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. (△) THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. (△) 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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