# R65012
# One-Chip Microprocessor

## SECTION 1
## INTRODUCTION

### SUMMARY

The Rockwell R65012 is a complete, high performance 8-bit NMOS-3 microcomputer on a single chip and is compatible with all members of the R6500 family.

The R65012 consists of an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of Random Access Memory (RAM), and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 32 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts, and bus expandability. The R65012 can be thought of as a modified R6501 and the major feature differences are shown in bold.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the R65012 a leading candidate for microcomputer applications.

Rockwell supports development of the R65012 with the Low Cost Emulator (LCE) Development System and the R6500/* Family of Personality Modules. Complete in-circuit emulation with the R6500/* Family of Personality Modules allows total system test and evaluation.

This product description assumes that the reader is familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Document Order No. 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Document Order No. 202).

### FEATURES

* Enhanced 6502 CPU
  - Four new bit manipulation instructions
       Set Memory Bit (SMB)
       Reset Memory Bit (RMB)
       Branch on Bit Set (BBS)
       Branch on Bit Reset (BBR)
  - **Binary arithmetic mode only**
  - 13 addressing modes
  - True indexing
  - **Stack on page one**
  - **Page select bit for zero page instructions**
* 192-byte static RAM
* 32 bidirectional, TTL-compatible I/O lines (four ports)
  - One 8-bit port may be tri-stated under software control
  - One 8-bit port may have latched inputs under software control
  - Internal pull-up resistors on ports PA and PB
* Two 16-bit programmable counter/timers, with latches
  - Pulse width measurement
  - Asymmetrical pulse generation
  - Pulse generation
  - Interval timer
  - Event counter
  - Retriggerable interval timer
* Serial Port
  - Full-duplex asynchronous operation mode
  - **One stop bit only**
  - Selectable 5- to 8-bit characters
  - Wake-up feature
  - Synchronous shift register mode
  - Standard programmable bit rates programmable up to 62.5K bits/sec @ 1 MHz
* Ten interrupts
  - Four edge-sensitive lines; two positive, two negative
  - Reset and non-maskable interrupt
  - Two counter underflows
  - Serial data received and serial data transmitted
* Bus expandable to 64K bytes of external memory

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## FEATURES (Cont'd)

- Flexible clock circuitry
  - **3 MHz (R65012B), 2 MHz (R65012A) or 1 MHz (R65012) internal operation**
  - Crystal or clock input
- **0.66 µs minimum instruction execution time at 3 MHz**
- Single +5V power supply
- 12 mW standby power for 32 bytes of the 192-byte RAM
- Available in 64-pin plastic QUIP and 68-pin PLCC packages

## ORDERING INFORMATION

T-49-17-06

Part Number:
R65012

Temperature Range (T$_L$ to T$_H$):
No Letter =   0°C to 70°C
E =          −40°C to +85°C

Package
J =   68-Pin PLCC
Q =   64-Pin Plastic QUIP

Frequency
No Letter =   1 MHz Operation
A =           2 MHz Operation
B =           3 MHz Operation

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## SECTION 2
## INTERFACE REQUIREMENTS

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This section describes the interface requirements for the R65012. Figure 2-1 and 2-2 show the interface and the pin assignments for both devices. Table 2-1 describes the function of each pin.
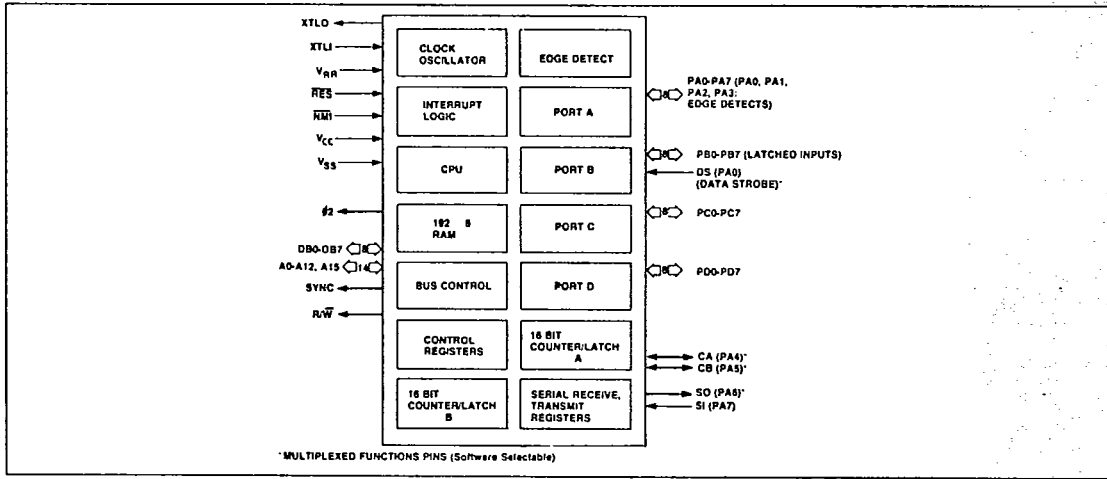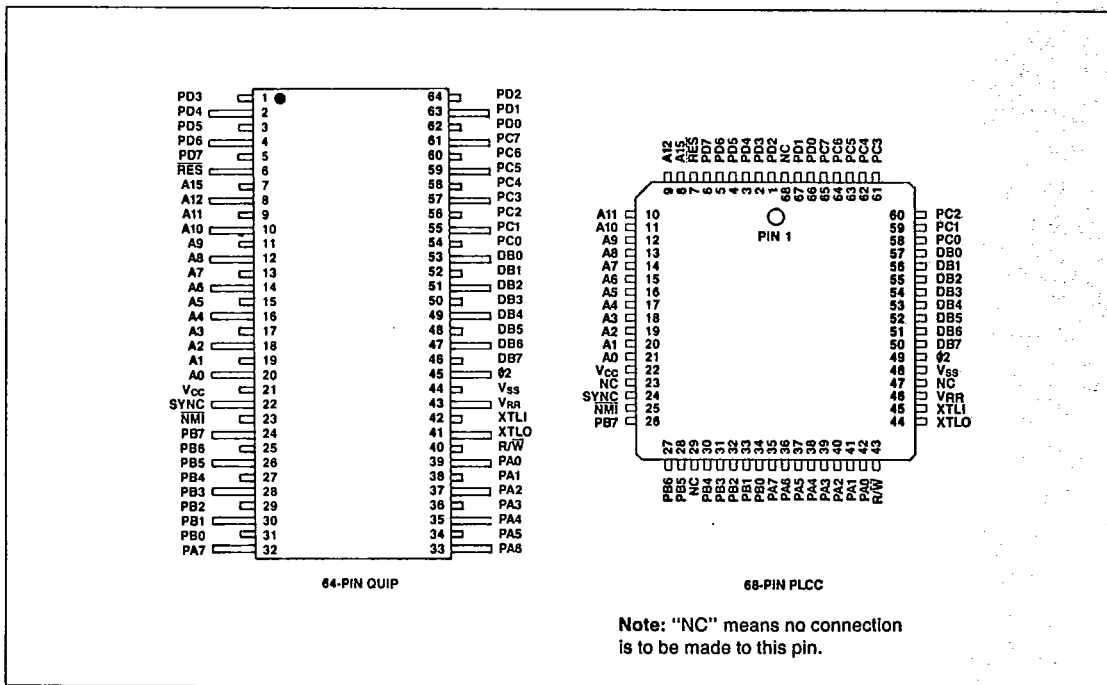


**Figure 2-1. R65012 Interface Diagram**



**Note:** "NC" means no connection is to be made to this pin.

**Figure 2-2. R65012 Pin Assignments**

Table 2-1. R65012 Pin Descriptions                T-49-17-06

| Signal Name | I/O | Pin No. 64-Pin QUIP | Pin No. 68-Pin PLCC | Description |
|---|---|---|---|---|
| $V_{CC}$ | I | 21 | 22 | **Power.** Main power supply. +5V. |
| $V_{RR}$ | I | 43 | 46 | **RAM Retention Power.** Separate power pin for RAM. In the event that $V_{CC}$ power is off, this power retains RAM data. +5V. |
| $V_{SS}$ | | 44 | 48 | **Ground.** Signal and power ground (OV). |
| XTLI | I | 42 | 45 | **Crystal In.** Crystal or clock input for internal clock oscillator. Allows input of X1 clock signal if XTLO is connected to $V_{SS}$, or of X4 (R65012A) or X2(R65012A) clock if XTLO is floated. |
| XTLO | O | 41 | 44 | **Crystal Out.** Crystal output from internal clock oscillator. |
| $\overline{RES}$ | I | 6 | 7 | **RESET.** The Reset input is used to initialize the device. This signal must not transition from low to high for at least eight cycles after $V_{CC}$ reaches operating range and the internal oscillator has stabilized. |
| $\phi2$ | O | 45 | 49 | **Phase 2 Clock.** Clock signal output at internal frequency. |
| $\overline{NMI}$ | I | 23 | 25 | **Non-Maskable Interrupt.** A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated with the CPU. |
| PA0-PA7 | I/O | 39-32 | 42-35 | **Port A.** General purpose I/O Port A. |
| PB0-PB7 | I/O | 31-24 | 34-30, 28-26 | **Port B.** General purpose I/O Port B. |
| PC0-PC7 | I/O | 54-61 | 58-65 | **Port C.** General purpose I/O Port C. |
| PD0-PD7 | I/O | 62-64, 1-5 | 66, 67, 1-6 | **Port D.** General purpose I/O Port D. |
| | | | | Four 8-bit ports used for input/output. Each line of Ports A, B and C consists of an active transistor to $V_{SS}$ and a passive pull-up to $V_{CC}$. Port D functions as either an 8-bit input or an 8-bit output port. It has active pull-up and pull-down transistors. |
| A0-A12, A15 | O | 20-8, 7 | 21-9, 8 | **Address Lines.** Fourteen address lines used to address a complete 65K byte external address space. Note: A13 and A14 are sourced through PC6 and PC7 when in the Full Address Mode. |
| DB0-DB7 | I/O | 53-46 | 57-50 | **Data Lines.** Eight bidirectional data bus lines used to transmit data to and from external memory. |
| SYNC | O | 22 | 24 | **SYNC.** SYNC is a positive going signal for the full clock cycle whenever the CPU is performing an op code fetch. |
| $R/\overline{W}$ | O | 40 | 43 | **READ/WRITE.** $R/\overline{W}$ controls the direction of data transfer between the CPU and the external 65K byte address space. The signal is high when reading or low when writing. |

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# SECTION 3
# SYSTEM ARCHITECTURE                    T-49-17-06

This section provides a functional description of the R65012. Functionally, the R65012 consists of a CPU, RAM, four 8-bit parallel I/O ports, a serial I/O port, dual counter/latch circuits, a mode control register, an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

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**NOTE**

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

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## 3.1 CPU LOGIC

The R65012 internal CPU is a standard 6502 configuration with an 8-bit Accumulator register, two 8-bit index registers (X and Y); an 8-bit Stack Pointer register, an arithmetic and logic unit (ALU), a 16-bit Program Counter, and standard Instruction register/decode and internal timing control logic.

### 3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

### 3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially using those data tables.

### 3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, an internal interrupt request (IRQ), or the external non-maskable interrupt input (NMI). The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI, and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may be accessed only from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus and data are read from the memory location addressed by the Stack Pointer.

The stack is located on page one, i.e., memory locations 01FF-0100. After reset, which leaves the Stack Pointer indeterminate, normal usage calls for its initialization at 01FF.

### 3.1.4 Arithmetic And Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

### 3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order 8 bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

### 3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register, then decoded along with timing

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**Figure 3-1.  Detailed Block Diagram**

and interrupt signals to generate control signals for the various registers.

### 3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is set to T0 each time an instruction fetch is executed and is advanced at the beginning of each Phase One clock pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

### 3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; RES, NMI and IRQ. IRQ is generated by any one of eight conditions: 2 Counter Overflows, 2 Positive Edge Detects, 2 Negative Edge Detects, and 2 Serial Port Conditions.

## 3.2 NEW INSTRUCTIONS

In addition to the standard R65012 instruction set, four new bit manipulation instructions have been added to the R65012. The added instructions and their format are explained in the following paragraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions. The four added instructions do not impact the CPU processor status register. These operate on data in page zero or page two. The page is selected by the CLD or SED instruction.

### 3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and one of eight bits to be set. The second byte of the instruction designates address (0-255) of the byte to be operated upon.

### 3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

### 3.2.3 Branch On Bit Set Relative
### (BBS m, Addr, DEST)

This instruction tests one of eight bits designated by a 3-bit immediate field with in the first byte of the instruction.

The second byte designates the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction specifies the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

### 3.2.4 Branch On Bit Reset Relative
### (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

## 3.3 READ-ONLY-MEMORY (ROM)

The R65012 has no ROM and its Reset vector is at FFFC.

## 3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 bytes of read/write memory with an assigned page zero address of 0040 through 00FF. The R65012 provides a separate power pin ($V_{RR}$) which may be used for standby power for 32 bytes located at 0040-005F. In the event of the loss of $V_{CC}$ power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the $V_{RR}$ pin. If the RAM data retention is not required, then $V_{RR}$ must be connected to $V_{CC}$. During operation $V_{RR}$ must be at the $V_{CC}$ level.

For the RAM to retain data upon loss of $V_{CC}$, $V_{RR}$ must be supplied within operating range and RES must be driven low at least eight $\phi2$ clock pulses before $V_{CC}$ falls out of operating range. RES must then be held low while $V_{CC}$ is out of operating range and until at least eight $\phi2$ clock cycles after $V_{CC}$ is again within operating range and the internal $\phi2$ oscillator is stabilized. $V_{RR}$ must remain within $V_{CC}$ operating range during normal operation. When $V_{CC}$ is out of operating range, $V_{RR}$ must remain within the $V_{RR}$ retention range in order to retain data. Figure 3-2 shows typical waveforms.
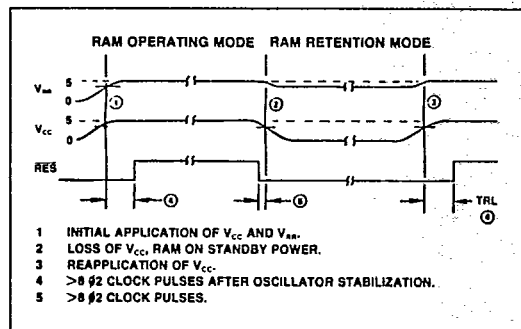


Figure 3-2. Data Retention Timing

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## 3.5 CLOCK OSCILLATOR

The R65012 has been configured for a crystal oscillator, a countdown network, and for Master Mode Operation.

A reference frequency can be generated with the on-chip oscillator using either an external crystal or an external oscillator. The oscillator reference frequency passes through an internal countdown network to obtain the internal operating frequency.

The on-chip oscillator is designed for a parallel resonant crystal connected between XTLI and XTLO pins. The equivalent oscillator circuit is shown in Figure 3-3a.

A parallel resonant crystal is specified by its load capacitance and series resonant resistance. For proper oscillator operation, the load capacitance ($C_L$), series resistance ($R_S$) and the crystal resonant frequency (F) must meet the following two relations:

$$(C + 27) = 2C_L \text{ or } C = 2C_L - 27 \text{ pF}$$

$$R_S \le R_{SMAX} = \frac{2 \times 10^6}{(FC_L)^2}$$

where: F is in MHz; C and $C_L$ are in pF; R is in ohms.

To select a parallel resonant crystal for the oscillator, first select the load capacitance from a crystal manufacturer's catalog. Next, calculate $R_{SMAX}$ based on F and $C_L$. The selected crystal must have a $R_S$ less than $R_{SMAX}$.

For example, if $C_L$ = 22 pF for a 4 MHz parallel resonant crystal, then

C = (2 x 22) – 27 = 17 pF (use standard value of 18 pF)

The series resistance of the crystal must be less than

$$R_{SMAX} = \frac{2 \times 10^6}{(4 \times 22)^2} = 258 \text{ ohms}$$

Internal timing can also be controlled by driving the XTLI pin with an external frequency source. Figure 3-3b shows typical connections. If XTLO is left floating, the external source is divided by the internal countdown network. However, if XTLO is tied to Vss, the internal countdown network is bypassed causing the chip to operate at the frequency of the external source.

## 3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B. Its setting, along with the setting of the Serial Communications Control Register (SCCR), determines the basic configuration of the R65012 in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-4.
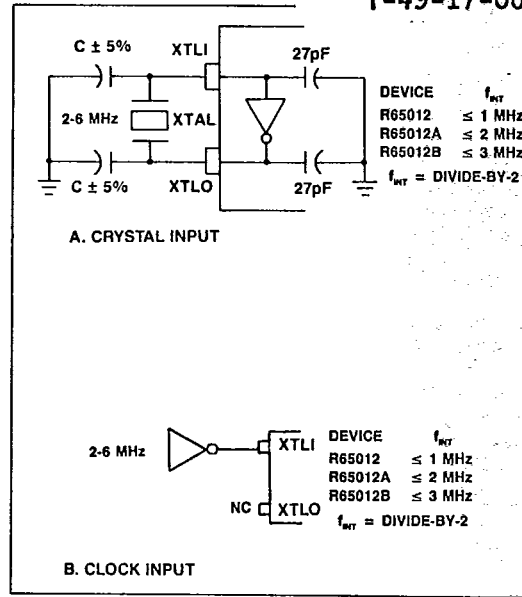


Figure 3-3. Clock Oscillator Input Options
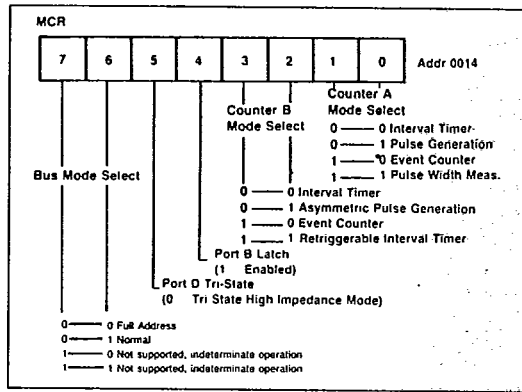


Figure 3-4. Mode control Register

## 3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An interrupt request (IRQ) can be initiated by any or all of eight possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts cause the interrupt request to remain active until all interrupting conditions have been serviced and cleared.
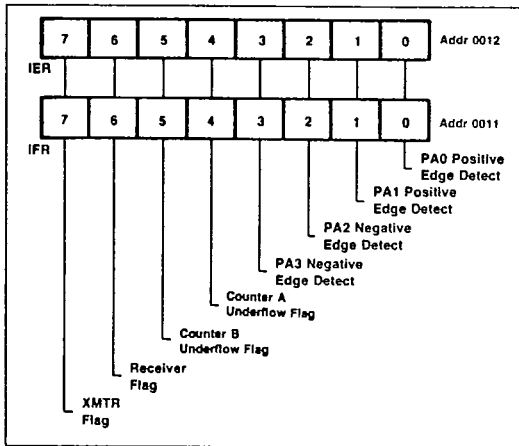
Figure 3-5. Interrupt Enable and Flag Registers

The Interrupt Flag register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. A logic "1" is ignored when writing to edge detect IFR bits.

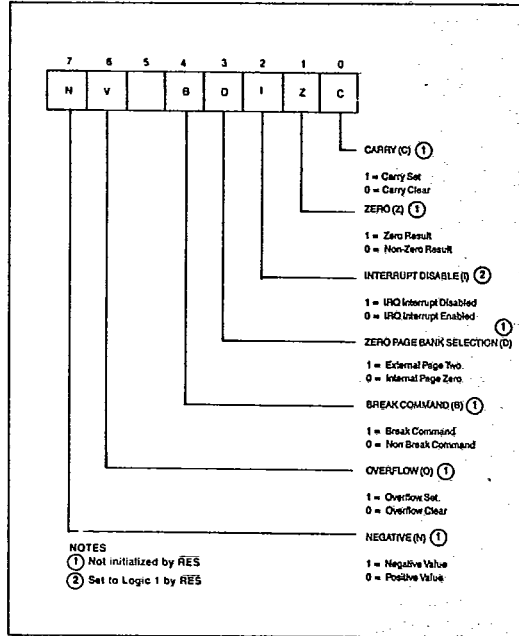Each IFR bit has corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits

may be cleared by writing a "0" in the respective bit position, or by RES. If set to a "1", an IRQ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-5 and the functions of each bit are explained in Table 3-1.



Figure 3-6. Processor Status Register

Table 3-1. Interrupt Flag Register Bit Codes

| Bit Code | Function |
|---|---|
| IFR 0: | PA0 Positive Edge Detect Flag—Set to a "1" when a positive goning edge is detected on PA0. Cleared by RMB 0 (0010) instruction or by RES. |
| IFR 1: | PA1 Positive Edge Detect Flag—Set to a 1 when a positive going edge is detected on PA1. Cleared by RMB 1 (0010) instruction or by RES. |
| IFR2: | PA2 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA2. Cleared by RMB 2 (0010) instruction or by RES. |
| IFR 3: | PA3 Negative Edge Detect Flag—Set to a 1 when a negative going edge is detected on PA3. Cleared by RMB 3 (0010) instruction or y RES. |
| IFR 4: | Counter A Underflow Flag—Set to a 1 when Counter A underflow occurs. Cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by RES. |
| IFR 5: | Counter B Underflow Flag—Set to a 1 when Counter B underflow occurs. Cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES. |
| IFR 6: | Receiver Interrupt Flag—Set to a 1 when any of the Serial Communication Status Register bits 0 through 3 is set to a 1. Cleared when the Receiver Status bits (SCSR 0-3) are cleared or by RES. |
| IFR 7: | Transmitter Interrupt Flag—Set to a 1 when SCSR 6 is set to a 1 while SCSR 5 is a 0 or SCSR 7 is set to a 1, Cleared when the Transmitter Status bits (SCSR 6 &7) are cleared or by RES. |

The use of Counter A Mode Select is shown in Section 6.1.

The use of Counter B Mode Select is shown in Section 6.2.

The use of Port B Latch Enable is shown in Section 4.4

The use of Port D in Tri-State Enable is shown in Section 4.6.

The use of bus Mode Select is shown in Section 4.5 and 4.6.

## 3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-6, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R65012 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

### 3.8.1 Carry Bit (C)

The Carry Bit (C) can be consipergagitated considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

### 3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R65012 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

### 3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) controls the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the IRQ signal will be serviced. If the bit is set to logic 1, the IRQ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET (RES), IRQ, or Non-Maskable Interrupt (NMI) signal is detected.

The I Bit is cleared by the Clear Interrupt Mask (CLI) instruction and is set by the Set Interrupt Mask (SEI) instruction. This bit is set by the BRK instruction. The return from Interrupt (RTI) and Pull Processor Status (PLP) instructions also affect the I bit.

### 3.8.4 Zero Page Bank Select Bit (D)

This bit is used to bank select the zero page. When this bit is set to logic 1, instructions that operate on zero page memory locations will operate on memory locations 0200 through 02FF of external RAM. When this bit is cleared to logic 0, instructions that operate on zero page memory locations will operate on locations 0000 through 00FF of internal memory.

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**CAUTION**

The Zero Page Bank Select Bit will either set or clear in an unpredictable manner upon power application. This bit must be initialized to the desired state by the user program or erroneous results may occur.

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### 3.8.5 Break Bit (B)

The Break Bit (B) indicates the condition which caused the IRQ service routine to be entered. If the IRQ service routine was entered because the CPU executed a BRK command, the Break Bit is set to logic 1. If the IRQ routine was entered as the result of an IRQ signal being generated, the B Bit is cleared to logic 0. There are no instructions which can set or clear this bit.

### 3.8.6 Overflow Bit (V)

The Overflow Bit (V) indicates that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits ($-128 \leq n \leq 127$).

This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or −128; otherwise the bit is cleared to logic 0. The V Bit is also be cleared by the Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction—which may be used to sample interface devices—allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instruction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions affecting the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

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**3.8.7 Negative Bit (N)**

The Negative Bit (N) indicates that the sign bit (bit 7) in the resulting value of a data movement or data arithmetic operation is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

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# SECTION 4
# PARALLEL INPUT/OUTPUT PORTS & BUS MODES

The devices have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC, and PD). Ports A through C may be used either for input or output individually or in groups of any combination. Port D may be used as all inputs or all outputs.

Multifunction I/O's such as Port A and Port C are protected from normal port I/O instructions when they are programmed to perform a multiplexed function.

Internal pull-up resistors (FETs with an impedance range of $3K \leq R_L \leq 12K$ ohm) are provided on all port pins except Port D.

The direction of the 32 I/O lines is controlled by four 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, thus simplifying I/O handling. The I/O addresses are shown in Table 4-1.

**Table 4-1.  I/O Port Addresses**

| Port | Address |
|------|---------|
| A | 0000 |
| B | 0001 |
| C | 0002 |
| D | 0003 |

## 4.1 INPUTS

Inputs for Ports A, B, and C are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An RES signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port D may only be all inputs or all outputs. All inputs is selected by setting bit 5 of the Mode control Register (MCR5) to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, & PD. During the Read cycle of a Read/Modify/Write instructions, the Port I/O register is read. For all other read instruction the port input lines are read. Read/Modify/Write instructions are: ASL, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

## 4.2 OUTPUTS

Outputs for Ports A through D are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output.

Port D all outputs are selected by setting MCR5 to a "1".

## 4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) and the Serial Communications Control Register (SCCR) as standard parallel 8-bit, bit independent, I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges and PA2 and PA3 can detect negative going edges. A proper transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi2$ clock rate.

## 4.4 PORT B (PB)

Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register (MCR). Table 4-3 tabulates the control and usage of Port B. An Input Data Strobe signal must be provided through PA0 when Port B is programmed to be used with latched input option. Input data latch timing for Port B is shown in Appendix E.3.

**Table 4-2.  Port A Control and Usage**

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**PA0 (2)**

| PA0 I/O | | PORT B LATCH MODE | |
|---|---|---|---|
| MCR4 = 0 | | MCR4 = 1 | |
| SIGNAL | | SIGNAL | |
| NAME | TYPE | NAME | TYPE |
| PA0 | I/O | PORT B LATCH STROBE | INPUT (1) |

**PA1 (2)**
**PA2 (3)**
**PA3 (3)**

| PA1–PA3 I/O | |
|---|---|
| SIGNAL | |
| NAME | TYPE |
| PA1 | I/O |
| PA2 | I/O |
| PA3 | I/O |

**PA4**

| PA4 I/O | | COUNTER A I/O | | | |
|---|---|---|---|---|---|
| MCR0 = 0<br>MCR1 = 0<br>SCCR7 = 0<br>RCVR S/R MODE = 0<br>(4) (5) | | MCR0 = 1<br>MCR1 = 0<br>SCCR7 = 0<br>RCVR S/R MODE = 0<br>(4) | | SCCR7 = 0<br>SCCR6 = 0<br>MCR1 = 1 | |
| SIGNAL | | SIGNAL | | SIGNAL | |
| NAME | TYPE | NAME | TYPE | NAME | TYPE |
| PA4 | I/O | CNTA | OUTPUT | CNTA | INPUT (1) |

| SERIAL I/O SHIFT REGISTER CLOCK | | | |
|---|---|---|---|
| SCCR7 = 1<br>SCCR5 = 1 | | RCVR S/R MODE = 1<br>(4) | |
| SIGNAL | | SIGNAL | |
| NAME | TYPE | NAME | TYPE |
| XMTR CLOCK | OUTPUT | RCVR CLOCK | INPUT (1) |

**PA5**

| PA5 I/O | | COUNTER B I/O | | | |
|---|---|---|---|---|---|
| MCR3 = 0<br>MCR2 = 0 | | MCR3 = 0<br>MCR2 = 1 | | MCR3 = 1<br>MCR2 = X | |
| SIGNAL | | SIGNAL | | SIGNAL | |
| NAME | TYPE | NAME | TYPE | NAME | TYPE |
| PA5 | I/O | CNTB | OUTPUT | CNTB | INPUT (1) |

**PA6**

| PA6 I/O | | SERIAL I/O<br>XMTR OUTPUT | |
|---|---|---|---|
| SCCR7 = 0 | | SCCR7 = 1 | |
| SIGNAL | | SIGNAL | |
| NAME | TYPE | NAME | TYPE |
| PA6 | I/O | XMTR | OUTPUT |

**PA7**

| PA7 I/O | | SERIAL I/O<br>RCVR INPUT | |
|---|---|---|---|
| SCCR6 = 0 | | SCCR6 = 1 | |
| SIGNAL | | SIGNAL | |
| NAME | TYPE | NAME | TYPE |
| PA7 | I/O | RCVR | INPUT (1) |

(1) HARDWARE BUFFER FLOAT
(2) POSITIVE EDGE DETECT
(3) NEGATIVE EDGE DETECT
(4) RCVR S/R MODE = 1 WHEN SCCR6 · S̄C̄C̄R̄5̄ · SCCR4 = 1
(5) For the following mode combinations PA4 is available as an Input Only pin:
S̄C̄C̄R̄7̄·SCCR6·SCCR5·MCR1
+S̄C̄C̄R̄7̄·SCCR6·SCCR4·MCR1
+S̄C̄C̄R̄7̄·S̄C̄C̄R̄6̄·SCCR5
+S̄C̄C̄R̄7̄·SCCR5·SCCR4·

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### Table 4-3. Port B Control and Usage

| Pin Name | I/O Mode MCR4 = 0 | | Latch Mode[2] MCR4 = 1 | |
| | Signal Name | Signal Type[1] | Signal Name | Signal Type |
|---|---|---|---|---|
| PB0 | PB0 | I/O | PB0 | INPUT |
| PB1 | PB1 | I/O | PB1 | INPUT |
| PB2 | PB2 | I/O | PB2 | INPUT |
| PB3 | PB3 | I/O | PB3 | INPUT |
| PB4 | PB4 | I/O | PB4 | INPUT |
| PB5 | PB5 | I/O | PB5 | INPUT |
| PB6 | PB2 | I/O | PB6 | INPUT |
| PB7 | PB2 | I/O | PB7 | INPUT |

NOTES: 1. Resistive Pull-Up, Active Buffer Pull-Down
2. Input data is stored in Port B latch by PA0 Pulse

### 4.5 PORT C (PC)

Port C can be programmed as an I/O port, as part of the full address bus. When operating in the Full Address Mode, PC6 and PC7 serve as A13 and A14 with PC0-PC5 operating as normal I/O pins. Table 4-4 shows the Port C control and usage.

### Table 4-4. Port C Control and Usage

| Pin Name | Full Address Mode MCR7 = 0 MCR6 = 0 | | Normal Mode MCR7 = 0 MCR6 = 1 | |
| | Signal Name | Signal Type | Signal Name | Signal Type[1] |
|---|---|---|---|---|
| PC0 | PC0 | I/O[1] | PC0 | I/O |
| PC1 | PC1 | I/O[1] | PC1 | I/O |
| PC2 | PC2 | I/O[1] | PC2 | I/O |
| PC3 | PC3 | I/O[1] | PC3 | I/O |
| PC4 | PC4 | I/O[1] | PC4 | I/O |
| PC5 | PC5 | I/O[1] | PC5 | I/O |
| PC6 | A13 | OUTPUT[2] | PC6 | I/O |
| PC7 | A14 | OUTPUT[2] | PC7 | I/O |

NOTES: 1. Resistive Pull-Up, Active Buffer Pull-Down
2. Input data is stored in Port B latch by PA0 Pulse

### 4.6 PORT D (PD)

Port D can be programmed as an I/O port, an 8-bit tri-state data bus. Mode selection for Port D is made by the Mode Control Register (MCR). The Port D output drivers can be selected as tri-state drivers by setting bit 5 of the MCR to 1. Table 4-5 shows the necessary settings for the MCR to achieve the various modes for Port D.

### Table 4-5. Port D Control and Usage

| Pin Name | Normal Mode MCR7 = 0 MCR6 = X MCR5 = 0 | | Normal Mode MCR7 = 0 MCR6 = X MCR5 = 1 | |
| | Signal Name | Signal Type[1] | Signal Name | Signal Type[2] |
|---|---|---|---|---|
| PD0 | PD0 | INPUT | PD0 | OUTPUT |
| PD1 | PD1 | INPUT | PD1 | OUTPUT |
| PD2 | PD2 | INPUT | PD2 | OUTPUT |
| PD3 | PD3 | INPUT | PD3 | OUTPUT |
| PD4 | PD4 | INPUT | PD4 | OUTPUT |
| PD5 | PD5 | INPUT | PD5 | OUTPUT |
| PD6 | PD6 | INPUT | PD6 | OUTPUT |
| PD7 | PD7 | INPUT | PD7 | OUTPUT |

NOTES: 1. Tri-State Buffer is in High Impedance Mode
2. Tri-State Buffer is in Active Mode

### 4.7 BUS MODES

A special attribute of Port C and Port D is their capability to be configured via the Mode Control Register (see Section 3.6) into four different modes.

In the Full Address Mode, the separate address and data bus are used in conjunction with PC6 and PC7, which automatically provide A13 and A14. The remaining ports perform the normal I/O function.

In the Normal Mode, all ports serve as I/O. The address and data bus are still functional but without A13 and A14. Since the internal RAM and registers are in the 00XX location, A15 can be used for chip select and A0-A12 used for selecting 8K of external memory.

Figures 4-1a and 4-1b show the possible configurations of the two bus modes. Figure 4-2 shows a memory map of the part as a function of the Bus Mode and further shows which addresses are active or inactive on each of the three possible buses.

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A. FULL ADDRESS MODE                    B. NORMAL BUS MODE
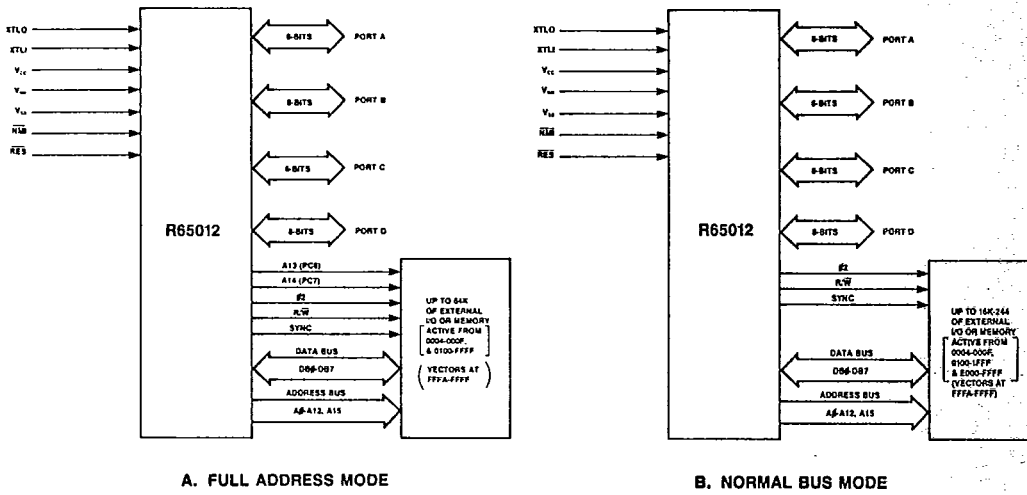
Figure 4-1.  R65012 Bus Mode Configurations

T-49-17-06
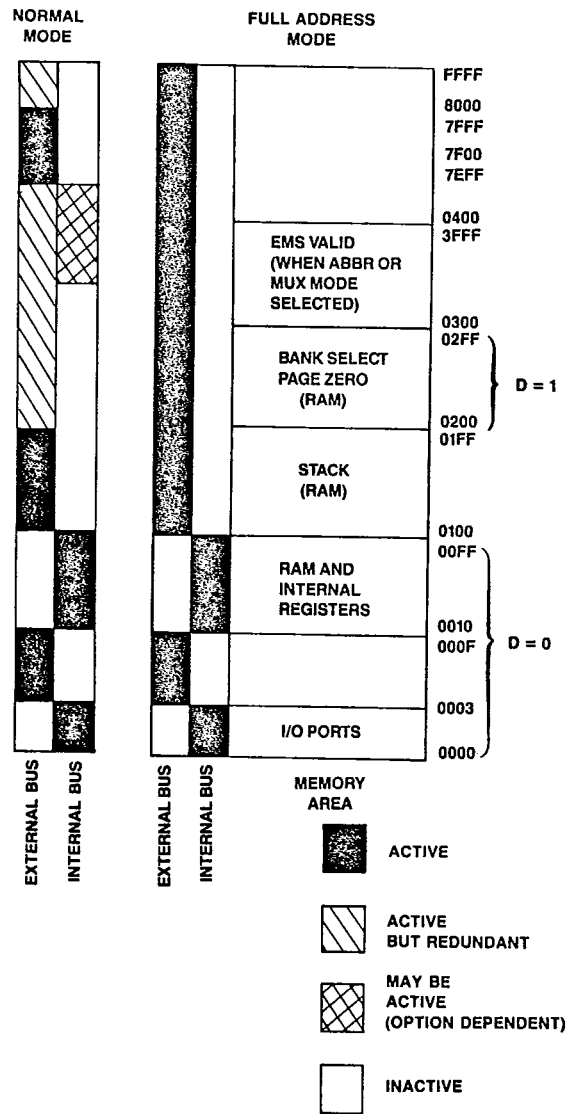


**Figure 4-2.  R65012 Memory Map**

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# SECTION 5
## SERIAL INPUT/OUTPUT CHANNEL

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The device provides a full duplex serial I/O channel with programmable bit rates and operating modes. The serial I/O functions are controlled by the Serial Communication Control Register (SCCR). The SCCR bit assignment is shown in Figure 5-1. The serial bit rate is determined by Counter A for all modes except the Receiver Shift Register (RCVR S/R) mode for which an external shift clock must be provided. The maximum data rate using the internal clock is 62.5K bits per second (at $\phi2 = 1$ MHz). The transmitter (XMTR) and receiver (RCVR) can be independently programmed to operate in different modes and can be independently enabled or disabled.
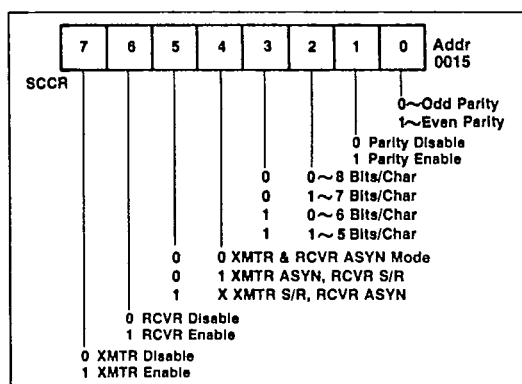


Figure 5-1. Serial Communication Control Register

Except for the Receiver Shift Register Mode (RCVR S/R), all XMTR and RCVR bit rates will occur at one sixteenth of the Counter A interval timer rate. Counter A is forced into an interval timer mode whenever the serial I/O is enabled in a mode requiring an internal clock.

Whenever Counter A is required as a timing source it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Counter A (paragraph 6.1) for a table of hexadecimal values to represent the desired data rate.

## 5.1 TRANSMITTER OPERATION (XTMR)

The XTMR operation and the transmitter related control/status functions are enabled by bit 7 of the Serial Com-
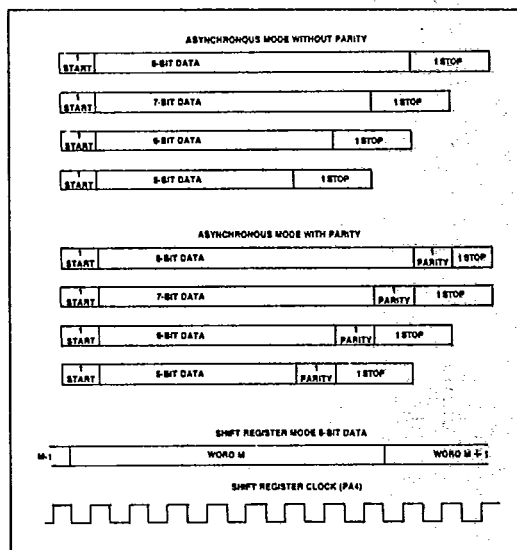


Figure 5-2. SIO Data Modes

munications Control Register (SCCR). The transmitter, when in the Asynchronous (ASYN) mode, automatically adds a start bit, one stop bit and, when enabled, a parity bit to the transmitted data. A word of transmitted data (in asynchronous parity mode) can have 5, 6, 7, or 8 bits of data. The nine data modes are shown in Figure 5-2. When parity is disabled, the 5, 6, 7, or 8 bits of data are terminated with one stop bit.

In the S/R mode, eight data bits are always shifted out. Bits character and parity control bits are ignored. The serial data is shifted out via the SO output (PA6) and the shift clock is available at the CA (PA4) pin. When the transmitter underrruns in the S/R mode the SO output and shift clock are held in a high state.

The XMTR Interrupt Flag bit (IFR7) is controlled by Serial Communication Status Register bits SCSR5, SCSR6 and SCSR7.

$$IFR7 = SCSR6 \, (\overline{SCSR5} + SCSR7)$$

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## 5.2 RECEIVER OPERATION (RCVR)

The receiver and its selected control and status functions are enabled when SCCR-6 is set to a "1". In the ASYN mode, data format must have a start bit, the appropriate number of data bits, a parity bit (if enabled), and one stop bit. Refer to paragraph 5.1 for a diagram of bit allocations. The receiver bit period is divided into 8 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit and strobe signal is generated at the approximate center of each incoming bit. Refer to Figure 5-3 for SYN Receive Data Timing. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. Framing error, over-run, and parity error conditions or a RCVR Data Register Full will set the appropriate status bits. Any of the above conditions will cause an Interrupt Request if the Receiver Interrupt Enable bit is set to logic 1.
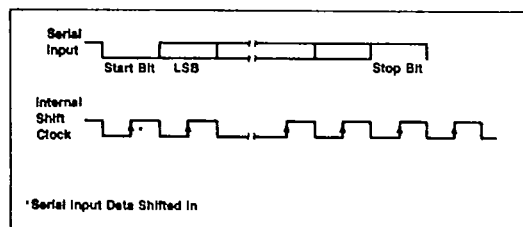


Figure 5-3.  ASYN Receive Data Timing

In the S/R mode, an external shift clock must be provided at CA (PA4) pin along with 8 bits of serial data (LSB first) at the SI input (PA7). The maximum data rate using an external shift clock is one-eighth the internal clock rate. Refer to Figure 5-4 for S/R Mode Timing.
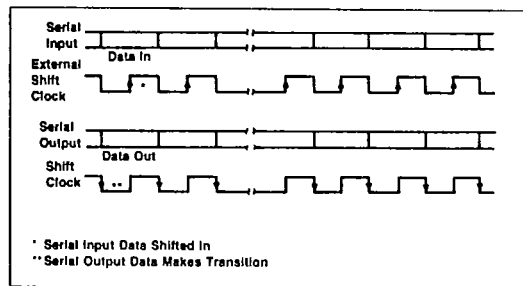


Figure 5-4.  S/R Mode Timing

A RCVR interrupt (IFR6) is generated whenever any of SCSR0-3 are true.

## 5.3  SERIAL COMMUNICATION STATUS REGISTER (SCSR)

The Serial Communication Status Register (SCSR) holds information on various communication error conditions, status of the transmitter and receiver data registers, a transmitter end-of-transmission condition, and a receiver idle line condition (Wake-Up Feature). The SCSR bit assignment is shown in Figure 5-5. Bit assignments and functions of the SCSR are as follows:

SCSR 0: *Receiver Data Register Full* - Set to a logic 1 when a character is transferred from the Receiver Shift Register to the Receiver Data Register. This bit is cleared by reading the Receiver Data Register, or by RES and is disabled if SCCR 6 = 0. The SCSR 0 bit will not be set to a logic 1 if the received data contains an error condition; instead, a corresponding error bit will be set to a logic 1.

SCSR 1: *Over-Run Error* - Set to a logic 1 when a new character is transferred from the Receiver Shift Register with the last character still in the Receiver Data Register. This bit is cleared by reading the receiver Data Register or by RES.

SCSR 2: *Parity Error* - Set to logic 1 when the RCVR is in the ASYN Mode, Parity Enable bit is set, and the received data has a parity error. This bit is cleared by reading the Receiver Data Register or by RES.

SCSR 3: *Framing Error* - Set to a logic 1 when the received data contains a zero bit after the last data or parity bit in the stop bit slot. Cleared by reading the Receiver Data Register or by RES (ASYN Mode only).

SCSR 4: *Wake-Up* - Set to a logic 1 by writing a "1" in bit 4 of address: 0016. The Wake-Up bit is cleared by RES or when the receiver detects a string of ten consecutive 1's. When the Wake-Up bit is set, SCSR0 through SCSR3 are inhibited.

SCSR 5: *End of Transmission* - Set to a logic 1 by writing a "1" in bit position 5 of address: 0016. The End of Transmission bit is cleared by RES or upon writing a new data word into the Transmitter Data Register. When the End-Of-Transmission bit is true the Transmitter Register Empty bit is disabled until a Transmitter Under-Run occurs.

SCSR 6: *Transmitter Data Register Empty* - Set to a logic 1 when the contents of the Transmitter Data Register are transferred to the Transmitter Shift Register. Cleared upon writing new data into the Transmit Data Register. This bit is initialized to a logic 1 by RES.

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SCSR 7: *Transmitter Under-Run* - Set to a logic 1 when the last data bit is transmitted if the transmitter is in a S/R Mode or when the last stop bit is transmitted if the XMTR is in the ASYN Mode while the Transmitter Data Register Empty Bit is set. Cleared by a transfer of new data into the Transmitter Shift Register or by RES.

## 5.4 WAKE-UP FEATURE

In a multi-distributed microprocessor or microcomputer applications, a destination address is usually included at the beginning of the message. The Wake-Up Feature allows non-selected DPU's to ignore the remainder of the message until the beginning of the next message by setting the Wake-Up bit. As long as the Wake-Up flag is true, the Receiver Data Register Full flag remains false. The Wake-Up bit is automatically cleared when the receiver detects a string of eleven consecutive 1's which indicates an idle transmit line. When the next byte is received, the Receiver Data Register Full Flag signals the CPU to wake-up and read the received data.
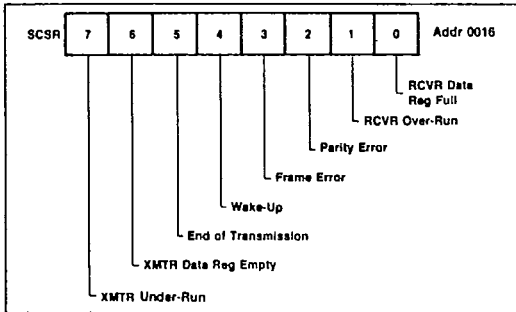


**Figure 5-5. SCSR Bit Allocations**

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<div align="center">

**SECTION 6**        T-49-17-06
**COUNTER/TIMERS**

</div>

The device contains two 16-bit counters (Counter A and Counter B) and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be independently programmed to operate in one of four modes:

| Counter A | Counter B |
|---|---|
| • Pulse Width Measurement | • Retriggerable Interval Counter |
| • Pulse Generation | • Asymetrical Pulse Generation |
| • Interval Timer | • Interval Timer |
| • Event Counter | • Event Counter |

Operating modes of Counter A and Counter B are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA4 is automatically selected for Counter A and PA5 is automatically selected for Counter B (see Table 4-2).

## 6.1 COUNTER A

Counter A consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter A (LCA), Upper Counter A (UCA), Lower Latch A (LLA), and Upper Latch A (ULA). The counter contains the count of either $\phi2$ clock pulses or external events, depending on the counter mode selected. The contents of Counter A may be read any time by executing a read at location 0019 for the Upper Counter A and at location 001A or location 0018 for the lower Counter A. A read at location 0018 also clears the Counter A Underflow Flag (IFR4).

The 16-bit latch contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch A at location 0019 and the Lower Latch A at location 0018. In either case, the contents of the accumulator are copied into the applicable latch register.

Counter A can be started at any time by writing to address: 001A. The contents of the accumulator will be copied into the Upper Latch A before the contents of the 16-bit latch are transferred to Counter A. Counter A is set to the latch value whenever Counter A underflows. When Counter A decrements from 0000, the next counter value will be the latch value—not FFFF—and the Counter A Underflow Flag (IFR4) will be set to a "1". This bit may be cleared by reading the Lower Counter A at location 0018, by writing to address location 001A, or by $\overline{RES}$.

Counter A operates in any of four modes. These modes are selected by the Counter A Mode Control bits in the Control Register.

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are $\phi2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

The Counter is set to the Interval Time Mode (00) when a $\overline{RES}$ signal is generated.

### 6.1.1 Interval Timer

In the Interval Timer mode, the Counter is initialized to the Latch value by either of two conditions:

| MCR1 (bit 1) | MCR0 (bit 0) | Mode |
|---|---|---|
| 0 | 0 | Interval Timer |
| 0 | 1 | Pulse Generation |
| 1 | 0 | Event Counter |
| 1 | 1 | Pulse Width Measurement |

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 001A, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the $\phi2$ clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1 $\mu s$ to 65.535 ms at the 1 MHz $\phi2$ clock rate, or 0.5 $\mu s$ to 32.767 ms at the 2 MHz $\phi2$ clock rate. Time intervals greater than the maximum counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When Counter A decrements from 0000, the Counter A Underflow (IFR4) is set to logic 1. If the Counter A Interrupt Enable Bit (IER4) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter A Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter A Underflow.

While the timer is operating in the Interval Timer Mode, PA4 operates as a PA I/O bit.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

<div align="center">20</div>

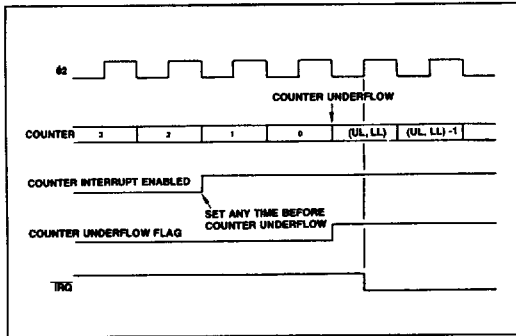**R65012**                                    **One-Chip Microprocessor**

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**Figure 6-1.  Interval Timer Timing Diagram**

### 6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the CA line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter A Underflow occurs or a write is performed to address 001A.

The normal output waveform is a symmetrical square-wave. The CA output is initialized high when entering the mode and transitions low when writing to 001A.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

### 6.1.3 Event Counter Mode

In this mode, the CA is used as an Event Input line, and the Counter decrements with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the $\phi2$ clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter A Underflow bit (IER4) is set to logic 1 if the underflow occurs.

Figure 6-2 is a timing diagram of the Event Counter Mode.
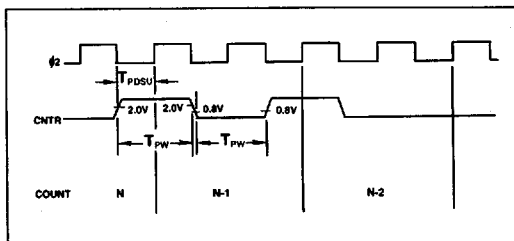


**Figure 6-2.  Event Counter Mode**

### 6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the CA line. The Counter decrements by one count at the $\phi2$ clock rate as long as the CA line is held in the low state. The Counter is stopped when CA is in the high state.

The Counter A underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the CA pin is held low. After the counter is stopped by a high level on CA, the count will hold as long as CA remains high. Any further low levels on CA will again cause the counter to count down from its present value. The state of the CA line can be determined by testing the state of PA4.

A timing diagram for the Pulse Width Measurement Mode is shown in Figure 6-3.
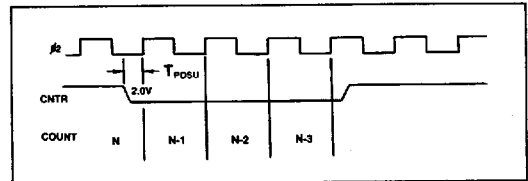


**Figure 6-3.  Pulse Width Measurement**

### 6.1.5 Serial I/O Data Rate Generation

Counter A also provides clock timing for the Serial I/O which establishes the data rate for the Serial I/O port. When the Serial I/O is enabled, Counter A is forced to operate at the internal clock rate. Counter A is not required for the RCVR S/R mode. The Counter I/O (PA4) may also be required to support the Serial I/O (see Table 4-2).

Table 6-1 identifies the values to be loaded in Counter A for selecting standard data rates with a $\phi2$ clock rate of 1 MHz and 2 MHz. Although Table 6-1 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{\phi2}{16 \times bps} - 1$$

where

| | | |
|---|---|---|
| N | = | decimal value to be loaded into Counter A using its hexadecimal equivalent. |
| $\phi2$ | = | the clock frequency (1 MHz or 2 MHz) |
| bps | = | the desired data rate. |

---
**NOTE**

In Table 6-1 you will notice that the standard data rate and the actual data rate may be slightly different. Transmitter and receiver errors of 1.5% or less are acceptable. A revised clock rate is included in Table 6-1 for those baud rates which fall outside this limit.

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Table 6-1. Counter A Values for Baud Rate Selection        T-49-17-06

| Standard Baud Rate | Hexadecimal Value | | | Actual Baud Rate At | | | Clock Rate Needed To Get Standard Baud Rate | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1 MHz | 2 MHz | 3 MHz | 1 MHz | 2 MHz | 3 MHz | 1 MHz | 2 MHz | 3 MHz |
| 50 | 04E1 | 09C3 | 0EA5 | 50.00 | 50.00 | 50.00 | 1.0000 | 2.0000 | 3.0000 |
| 75 | 0340 | 0682 | 09C3 | 75.03 | 74.99 | 75.20 | 1.0000 | 2.0000 | 3.0000 |
| 110 | 0237 | 046F | 06A8 | 110.04 | 110.04 | 109.97 | 1.0000 | 2.0000 | 3.0000 |
| 150 | 01A0 | 0340 | 04E1 | 149.88 | 150.06 | 150.00 | 1.0000 | 2.0000 | 3.0000 |
| 300 | 00CF | 01A0 | 0270 | 300.48 | 299.76 | 300.00 | 1.0000 | 2.0000 | 3.0000 |
| 600 | 0067 | 00CF | 0138 | 600.96 | 600.95 | 599.04 | 1.0000 | 2.0000 | 3.0000 |
| 1200 | 0033 | 0067 | 0096 | 1201.92 | 1201.92 | 1201.92 | 1.0000 | 2.0000 | 3.0000 |
| 2400 | 0019 | 0033 | 004D | 2403.85 | 2403.85 | 2403.85 | 1.0000 | 2.0000 | 3.0000 |
| 3600 | 0010 | 0021 | 0033 | 3676.47 | 3676.47 | 3605.77 | 0.9792 | 1.9584 | 3.0000 |
| 4800 | 000C | 0019 | 0026 | 4807.69 | 4807.69 | 4807.69 | 1.0000 | 2.0000 | 3.0000 |
| 7200 | 0008 | 0010 | 0019 | 6944.44 | 7352.94 | 7211.54 | 1.0368 | 1.9584 | 3.0000 |
| 9600 | 0006 | 000C | 0013 | 8928.57 | 9615.38 | 9375.00 | 1.0752 | 2.0000 | 3.0720 |

## 6.2 COUNTER B

Counter B consists of a 16-bit counter and two 16-bit latches organized as follows: Lower Counter B (LCB), Upper Counter B (UCB), Lower Latch B (LLB), Upper Latch B (ULB), Lower Latch C (LLC), and Upper Latch C (ULC). Latch C is used only in the asymmetrical pulse generation mode. The counter contains the count of either $\phi 2$ clock pulses or external events depending on the counter mode selected. The contents of Counter B may be read any time by executing a read at location 001D or 001C for the Lower Counter B. A read at location 001C also clears the Counter B Underflow Flag.

Latch B contains the counter initialization value and can be loaded at any time by executing a write to the Upper Latch B at location 001D and the Lower Latch B at location 001C. In each case, the contents of the accumulator are copied into the applicable latch register.

Counter B can be initialized at any time by writing to address 001E. The contents of the accumulator is copied into the Upper Latch B before the value in the 16-bit Latch B is transferred to Counter B. Counter B will also be set to the latch value and the Counter B Underflow Flag bit (IFR5) will be set to a "1" whenever Counter B underflows by decrementing from 0000.

IFR 5 may be cleared by reading the Lower Counter B at location 001C, by writing to address location 001E, or by RES.

Counter B operates in the same manner as Counter A in the Interval Timer and Event Counter modes. The Pulse Width Measurement Mode is replaced by the Retriggerable Interval Timer mode and the Pulse Generation mode is replaced by the Asymmetrical Pulse Generation mode. Mode Control Register bits MCR2 and MCR3 select

the four Counter B modes in a similar manner and coding as MCR0 and MCR1 select the modes of Counter A.

### 6.2.1 Retriggerable Interval Timer Mode

When operating in the Retriggerable Interval Timer mode, Counter B is initialized to the latch value by writing to address 001E, by a Counter B underflow, or whenever a positive edge occurs on the CB pin (PA5). The Counter B interrupt flag will be set if the counter underflows before a positive edge occurs on the CB line. Figure 6-4 illustrates the operation.
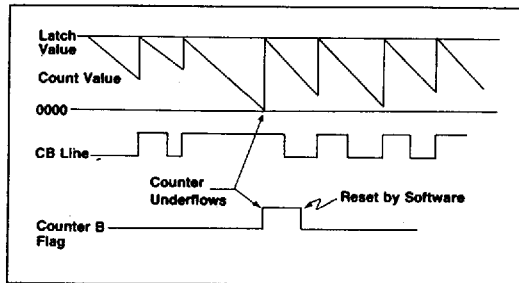


Figure 6-4. Counter B Retriggerable Interval Timer Mode

### 6.2.2 Asymmetrical Pulse Generation Mode

Counter B has a special Asymmetrical Pulse Generation Mode whereby a pulse train with programmable pulse width and period can be generated without the processor intervention once the latch values are initialized.

In this mode, the 16-bit Latch B is initialized with a value which corresponds to the duration between pulses (referred to as D in the following descriptions). The 16-bit Latch C is initialized with a value corresponding to the desired pulse width (referred to as P in the following

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descriptions). The initialization sequence for Latch B and C and the starting of a counting sequence are as follows:

1. The lower 8 bits of P are loaded into LLB by writing to address 001C; the upper 8 bits of P are loaded into ULB and the full 16 bits are transferred to Latch C by writing to address location 001D. At this point both Latch B and Latch C contain the value of P.

2. The lower 8 bits of D are loaded into LLB by writing to address 001C; the upper 8 bits of D are loaded into ULB by writing to address location 001E. Writing to address location 001E also causes the con-

tents of the 16-bit Latch B to be downloaded into the Counter B and the CB output to go low as shown in Figure 6-5.

3. When Counter B underflow occurs, the contents of the Latch C are loaded into the Counter B and the CB output toggles to a high level, staying high until another underflow occurs. Latch B is then downloaded and the CB output toggles to a low level repeating the whole process.
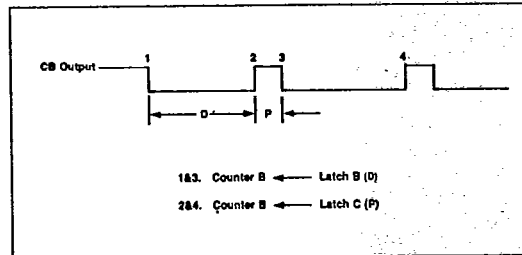


**Figure 6-5.  Counter B Pulse Generation**

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# SECTION 7
# POWER ON/INITIALIZATION CONSIDERATIONS

## 7.1 POWER ON TIMING

After application of $V_{CC}$ and $V_{RR}$ power to the device, $\overline{RES}$ must be held low for at least eight $\phi2$ clock cycles after $V_{CC}$ reaches operating range and the internal oscillator has stablized. This stabilization time is dependent upon the input $V_{CC}$ voltage and performance of the internal oscillator. The clock can be monitored at $\phi2$ (pin 3). Figure 7-1 illustrates the power turn-on waveforms. Clock stabilization time is typically 20 ms.
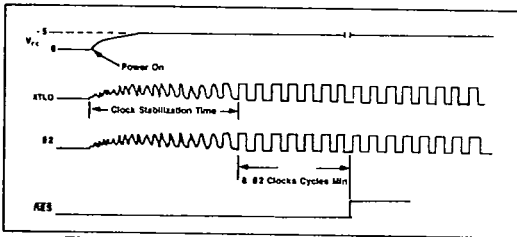


**Figure 7-1.  Power Turn-On Timing Detail**

## 7.2 POWER-ON RESET

When $\overline{RES}$ goes from low to high, the device sets the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiates a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports (PA, PB, PC, PD) are forced to the high (logic 1) state. All bits of the Control Register are cleared to logic 0 causing the Interval Timer Counter Mode (mode 00) to be selected and all interrupt enabled bits to be reset.

## 7.3 RESET ($\overline{RES}$) CONDITIONING

When $\overline{RES}$ is driven from low to high, the device is put in a reset state causing the registers and I/O ports to be configured as shown in Table 7-1.

All RAM and other CPU registers will initialized in a random, non-repeatable, data pattern.

**Table 7-1.  RES Initialization of I/O Ports and Registers**

|  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Registers** | | | | | | | | |
| Processor Status | – | – | – | – | – | 1 | – | – |
| Mode Control (MCR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Int. Enable (IER) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Int. Flag (IFR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Ser. Com. Control (SCCR) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Ports** | | | | | | | | |
| PA Latch | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| PB Latch | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| PC Latch | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| PD Latch | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## 7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$, as indicated in the preceding paragraphs. After stabilization of the internal clock (if a power on situation), an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls as required
5. Clear Interrups

A typical initialization subroutine could be as follows:

| | |
|---|---|
| LDX | Load stack pointer starting address into X Register |
| TXS | Transfer X Register value to Stack Pointer |
| CLD | Zero Page Bank Select (Clear Decimal Mode) |
| SEC | Set Carry Flag |
| .... | Set-up Mode Control and |
| .... | special function registers |
| .... | and clear RAM as required |
| CLI | Clear Interrupts |

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# APPENDIX A
## ENHANCED R6502 INSTRUCTION SET

This appendix contains a summary of the enhanced R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, (Order No. 202). The four instructions notated with an asterisk (*) are added instructions to enhance the the standard 6502 instruction set.

## A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

| Mnemonic | Description | Mnemonic | Description |
|---|---|---|---|
| ADC | Add Memory to Accumulator with Carry | LDA | Load Accumulator with Memory |
| AND | "AND" Memory with Accumulator | LDX | Load Index X with Memory |
| ASL | Shift Left One Bit (Memory or Accumulator) | LDY | Load Index Y with Memory |
| | | LSR | Shift One Bit Right (Memory or Accumulator) |
| BBR* | Branch on Bit Reset Relative | | |
| BBS* | Branch on Bit Set Relative | NOP | No Operation |
| BCC | Branch on Carry Clear | | |
| BCS | Branch on Carry Set | ORA | "OR" Memory with Accumulator |
| BEQ | Branch on Result Zero | | |
| BIT | Test Bits in Memory with Accumulator | PHA | Push Accumulator on Stack |
| BMI | Branch on Result Minus | PHP | Push Processor Status on Stack |
| BNE | Branch on Result not Zero | PLA | Pull Accumulator from Stack |
| BPL | Branch on Result Plus | PLP | Pull Processor Status from Stack |
| BRK | Force Break | | |
| BVC | Branch on Overflow Clear | RMB* | Reset Memory Bit |
| BVS | Branch on Overflow Set | ROL | Rotate One Bit Left (Memory or Accumulator) |
| | | ROR | Rotate One Bit Right (Memory or Accumulator) |
| CLC | Clear Carry Flag | RTI | Return from Interrupt |
| CLD | Zero Page Bank Select - Page Zero | RTS | Return from Subroutine |
| CLI | Clear Interrupt Disable Bit | | |
| CLV | Clear Overflow Flag | SBC | Subtract Memory from Accumulator with Borrow |
| CMP | Compare Memory and Accumulator | SEC | Set Carry Flag |
| CPX | Compare Memory and Index X | SED | Zero Page Bank Select–Page Two |
| CPY | Compare Memory and Index Y | SEI | Set Interrupt Disable Status |
| | | SMB* | Set Memory Bit |
| DEC | Decrement Memory by One | STA | Store Accumulator in Memory |
| DEX | Decrement Index X by One | STX | Store Index X in Memory |
| DEY | Decrement Index Y by One | STY | Store Index Y in Memory |
| | | | |
| EOR | "Exclusive-Or" Memory with Accumulator | TAX | Transfer Accumulator to Index X |
| | | TAY | Transfer Accumulator to Index Y |
| INC | Increment Memory by One | TSX | Transfer Stack Pointer to Index X |
| INX | Increment Index X by One | TXA | Transfer Index X to Accumulator |
| INY | Increment Index Y by One | TXS | Transfer Index X to Stack Register |
| | | TYA | Transfer Index Y to Accumulator |
| JMP | Jump to New Location | | |
| JSR | Jump to New Location Saving Return Address | | |

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**A.2  R65012 INSTRUCTION SET SUMMARY TABLE**                    T-49-17-06



R65012 Instruction Set Summary Table (addressing modes, opcodes, cycles, bytes, and processor status codes by mnemonic).

**LEGEND**

| | | |
|---|---|---|
| X | = | Index X |
| Y | = | Index Y |
| A | = | Accumulator |
| M | = | Memory per effective address |
| Ms | = | Memory per stack pointer |
| Mz | = | Selected zero page memory bit |
| M7 | = | Memory Bit 7 |
| M6 | = | Memory Bit 6 |
| + | = | Add |
| − | = | Subtract |
| ∧ | = | And |
| ∨ | = | Or |
| ∀ | = | Exclusive Or |
| # | = | Number of cycles |
| | = | Number of Bytes |

**NOTES**
1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result.
5. Effects 8-bit data field of the specified zero page address.

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## A.3 INSTRUCTION CODE MATRIX

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| MSD\LSD | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | BRK Implied 1 7 | ORA (IND,X) 2 6 | | | | ORA ZP 2 3 | ASL ZP 2 5 | RMB0 ZP 2 5 | PHP Implied 1 3 | ORA IMM 2 2 | ASL Accum 1 2 | | | ORA ABS 3 4 | ASL ABS 3 6 | BBR0 ZP 3 5** |
| 1 | BPL Relative 2 2** | ORA (IND),Y 2 5* | | | | ORA ZP,X 2 4 | ASL ZP,X 2 6 | RMB1 ZP 2 5 | CLC Implied 1 2 | ORA ABS,Y 3 4* | | | | ORA ABS,X 3 4* | ASL ABS,X 3 7 | BBR1 ZP 3 5** |
| 2 | JSR Absolute 3 6 | AND (IND,X) 2 6 | | | BIT ZP 2 3 | AND ZP 2 3 | ROL ZP 2 5 | RMB2 ZP 2 5 | PLP Implied 1 4 | AND IMM 2 2 | ROL Accum 1 2 | | BIT ABS 3 4 | AND ABS 3 4 | ROL ABS 3 6 | BBR2 ZP 3 5** |
| 3 | BMI Relative 2 2** | AND (IND),Y 2 5* | | | | AND ZP,X 2 4 | ROL ZP,X 2 6 | RMB3 ZP 2 5 | SEC Implied 1 2 | AND ABS,Y 3 4* | | | | AND ABS,X 3 4* | ROL ABS,X 3 7 | BBR3 ZP 3 5** |
| 4 | RTI Implied 1 6 | EOR (IND,X) 2 6 | | | | EOR ZP 2 3 | LSR ZP 2 5 | RMB4 ZP 2 5 | PHA Implied 1 3 | EOR IMM 2 2 | LSR Accum 1 2 | | JMP ABS 3 3 | EOR ABS 3 4 | LSR ABS 3 6 | BBR4 ZP 3 5** |
| 5 | BVC Relative 2 2** | EOR (IND),Y 2 5* | | | | EOR ZP,X 2 4 | LSR ZP,X 2 6 | RMB5 ZP 2 5 | CLI Implied 1 2 | EOR ABS,Y 3 4* | | | | EOR ABS,X 3 4* | LSR ABS,X 3 7 | BBR5 ZP 3 5** |
| 6 | RTS Implied 1 6 | ADC (IND,X) 2 6 | | | | ADC ZP 2 3 | ROR ZP 2 5 | RMB6 ZP 2 5 | PLA Implied 1 4 | ADC IMM 2 2 | ROR Accum 1 2 | | JMP Indirect 3 5 | ADC ABS 3 4 | ROR ABS 3 6 | BBR6 ZP 3 5** |
| 7 | BVS Relative 2 2** | ADC (IND),Y 2 5* | | | | ADC ZP,X 2 4 | ROR ZP,X 2 6 | RMB7 ZP 2 5 | SEI Implied 1 2 | ADC ABS,Y 3 4* | | | | ADC ABS,X 3 4* | ROR ABS,X 3 7 | BBR7 ZP 3 5** |
| 8 | | STA (IND,X) 2 6 | | | STY ZP 2 3 | STA ZP 2 3 | STX ZP 2 3 | SMB0 ZP 2 5 | DEY Implied 1 2 | | TXA Implied 1 2 | | STY ABS 3 4 | STA ABS 3 4 | STX ABS 3 4 | BBS0 ZP 3 5** |
| 9 | BCC Relative 2 2** | STA (IND),Y 2 6 | | | STY ZP,X 2 4 | STA ZP,X 2 4 | STX ZP,Y 2 4 | SMB1 ZP 2 5 | TYA Implied 1 2 | STA ABS,Y 3 5 | TXS Implied 1 2 | | | STA ABS,X 3 5 | | BBS1 ZP 3 5** |
| A | LDY IMM 2 2 | LDA (IND,X) 2 6 | LDX IMM 2 2 | | LDY ZP 2 3 | LDA ZP 2 3 | LDX ZP 2 3 | SMB2 ZP 2 5 | TAY Implied 1 2 | LDA IMM 2 2 | TAX Implied 1 2 | | LDY ABS 3 4 | LDA ABS 3 4 | LDX ABS 3 4 | BBS2 ZP 3 5** |
| B | BCS Relative 2 2** | LDA (IND),Y 2 5* | | | LDY ZP,X 2 4 | LDA ZP,X 2 4 | LDX ZP,Y 2 4 | SMB3 ZP 2 5 | CLV Implied 1 2 | LDA ABS,Y 3 4* | TSX Implied 1 2 | | LDY ABS,X 3 4* | LDA ABS,X 3 4* | LDX ABS,Y 3 4* | BBS3 ZP 3 5** |
| C | CPY IMM 2 2 | CMP (IND,X) 2 6 | | | CPY ZP 2 3 | CMP ZP 2 3 | DEC ZP 2 5 | SMB4 ZP 2 5 | INY Implied 1 2 | CMP IMM 2 2 | DEX Implied 1 2 | | CPY ABS 3 4 | CMP ABS 3 4 | DEC ABS 3 6 | BBS4 ZP 3 5** |
| D | BNE Relative 2 2** | CMP (IND),Y 2 5* | | | | CMP ZP,X 2 4 | DEC ZP,X 2 6 | SMB5 ZP 2 5 | CLD Implied 1 2 | CMP ABS,Y 3 4* | | | | CMP ABS,X 3 4* | DEC ABS,X 3 7 | BBS5 ZP 3 5** |
| E | CPX IMM 2 2 | SBC (IND,X) 2 6 | | | CPX ZP 2 3 | SBC ZP 2 3 | INC ZP 2 5 | SMB6 ZP 2 5 | INX Implied 1 2 | SBC IMM 2 2 | NOP Implied 1 2 | | CPX ABS 3 4 | SBC ABS 3 4 | INC ABS 3 6 | BBS6 ZP 3 5** |
| F | BEQ Relative 2 2** | SBC (IND),Y 2 5* | | | | SBC ZP,X 2 4 | INC ZP,X 2 6 | SMB7 ZP 2 5 | SED Implied 1 2 | SBC ABS,Y 3 4* | | | | SBC ABS,X 3 4* | INC ABS,X 3 7 | BBS7 ZP 3 5** |

Legend:

```
  0
+--------+    — OP Code
0| BRK    |    — Addressing Mode
 | Implied|
 | 1   7  |    — Instruction Bytes; Machine Cycles
+--------+
```

*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page; add 2 to N if branch occurs to different page.

## APPENDIX B
## KEY REGISTER SUMMARY

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**CPU Registers**

| | A | | ACCUMULATOR | A |
| | Y | | INDEX REGISTER Y | Y |
| | X | | INDEX REGISTER X | X |
| PCH | PCL | | PROGRAM COUNTER | PC |
| | SP | | STACK POINTER | S |
| N V B D I Z C | | | PROCESSOR STATUS REG | P |

**Processor Status Register**

| N | V | | B | D | I | Z | C |

CARRY (C) ①
  1 = Carry Set
  0 = Carry Clear
ZERO (Z) ①
  1 = Zero Result
  0 = Non-Zero Result
INTERRUPT DISABLE (I) ① ②
  1 = IRQ Interrupt Disabled
  0 = IRQ Interrupt Enabled
ZERO PAGE BANK SELECTION (D) ①
  1 = External Page Two
  0 = Internal Page Zero
BREAK COMMAND (B) ①
  1 = Break Command
  0 = Non Break Command
OVERFLOW (O) ①
  1 = Overflow Set
  0 = Overflow Clear
NEGATIVE (N) ①
  1 = Negative Value
  0 = Positive Value

NOTES
① Not initialized by RES
② Set to Logic 1 by RES

**Mode Control Register**

MCR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   Addr 0014

Counter A
Mode Select
  0 —— 0 Interval Timer
  0 —— 1 Pulse Generation
  1 —— 0 Event Counter
  1 —— 1 Pulse Width Meas.

Counter B
Mode Select
  0 —— 0 Interval Timer
  0 —— 1 Asymmetric Pulse Generation
  1 —— 0 Event Counter
  1 —— 1 Retriggerable Interval Timer

Port B Latch (1—Enable)
Port D Tri-State (0—Tri-State High Impedance Mode)

Bus Mode Select
  0 —— 0 Full Address
  0 —— 1 Normal
  1 —— 0 Not supported, indeterminate operation
  1 —— 1 Not supported, indeterminate operation

**Interrupt Enable and Flag Registers**

IFR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   Addr 0011

IER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   Addr 0012

PA0 Positive Edge Detect
PA1 Positive Edge Detect
PA2 Negative Edge Detect
PA3 Negative Edge Detect
Counter A Underflow Flag
Counter B Underflow Flag
RCVR Flag
XMTR Flag

**Serial Communications Control Register**

SCCR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   Addr 0015

0~Odd Parity
1~Even Parity
0 Parity Disable
1 Parity Enable

0 0~8 Bits/Char
0 1~7 Bits/Char
1 0~6 Bits/Char
1 1~5 Bits/Char

0 —— 0 XMTR & RCVR ASYN Mode
0 —— 1 XMTR ASYN, RCVR S/R
1 —— X XMTR S/R, RCVR ASYN

0 RCVR Disable
1 RCVR Enable

0 XMTR Disable
1 XMTR Enable

**Serial Communications Status Register**

SCSR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   Addr 0016

RCVR Data Reg Full
RCVR Over-Run
Parity Error
Frame Error
Wake-Up
End of Transmission
XMTR Data Reg Empty
XMTR Under-Run

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## APPENDIX C
## ADDRESS ASSIGNMENTS/MEMORY
## MAPS/PIN FUNCTIONS

**C.1 I/O AND INTERNAL REGISTER ADDRESSES**

| ADDRESS (HEX) | READ | WRITE |
|---|---|---|
| 001F | — — | — — |
| 1E | Lower Counter B | Upper Latch B, Cntr B←Latch B, CLR Flag |
| 1D | Upper Counter B | Upper Latch B, Latch C←Latch B |
| 1C | Lower Counter B, CLR Flag | Lower Latch B. |
| 1B | — — | — — |
| 1A | Lower Counter A | Upper Latch A, Cntr A←Latch A, CLR Flag |
| 19 | Upper Counter A | Upper Latch A |
| 18 | Lower Counter A, CLR Flag | Lower Latch A |
| 17 | Serial Receiver Data Register | Serial Transmitter Data Register |
| 16 | Serial Comm. Status Register | Serial Comm. Status Reg. Bits 4 & 5 only |
| 15 | Serial Comm. Control Register | Serial Comm. Control Register |
| 14 | Mode Control Register | Mode Control Register |
| 13 | — — | — — |
| 12 | Interrupt Enable Register | Interrupt Enable Register |
| 11 | Interrupt Flag Register | — — |
| 0010 | Read FF | Clear Int Flag (Bits 0–3 only, Write 0's only) |
| 0F | | |
| 0E | | |
| 0D | | |
| 0C | | |
| 0B | **RESERVED** | |
| 0A | These addresses are reserved and are used by the CPU during Read and Write | |
| 09 | operation over the external Data Bus (D0-D7). | |
| 08 | | |
| 07 | | |
| 06 | | |
| 05 | | |
| 04 | | |
| 03 | Port D | Port D |
| 02 | Port C | Port C |
| 01 | Port B | Port B |
| 0000 | Port A | Port A |

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## C.2 FULL ADDRESS MODE MEMORY MAP—R65012          T-49-17-06
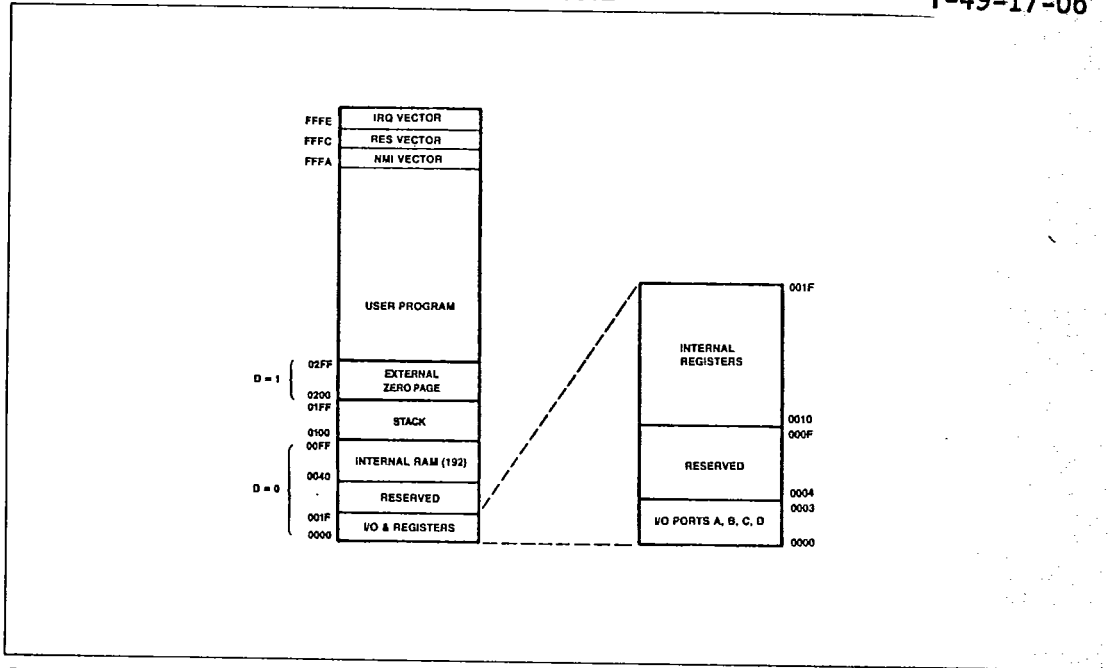


## C.3 MULTIPLE FUNCTION PIN ASSIGNMENTS—PORT C AND PORT D

| Full Address Mode | I/O Port Function |
|---|---|
| PC0<br>PC1<br>PC2<br>PC3 | PC0<br>PC1<br>PC2<br>PC3 |
| PC4<br>PC5<br>A13<br>A14 | PC4<br>PC5<br>PC6<br>PC7 |
| PD0<br>PD1<br>PD2<br>PD3 | PD0<br>PD1<br>PD2<br>PD3 |
| PD4<br>PD5<br>PD6<br>PD7 | PD4<br>PD5<br>PD6<br>PD7 |

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# APPENDIX D
# ELECTRICAL SPECIFICATIONS

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## MAXIMUM RATINGS*

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ & $V_{RR}$ | −0.3 to +7.0 | Vdc |
| Input Voltage | $V_{IN}$ | −0.3 to +7.0 | Vdc |
| Operating Temperature Range<br>Commercial<br>Industrial | $T_A$ | $T_L$ to $T_H$<br>0 to +70<br>−40 to +85 | °C |
| Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |

**\* NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

($V_{CC}$ = 5.0V ±5%; $V_{RR}$ = $V_{CC}$; $V_{SS}$ = 0V; $T_A$= $T_L$ to $T_H$ unless otherwise specified)

| Parameter | Symbol | Min | Typ[1] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RAM Standby voltage (Retention Mode) | $V_{RR}$ | 3.0 | – | $V_{CC}$ | V | |
| RAM Standby Current (Retention Mode) | $I_{RR}$ | – | 4 | – | mA | $T_A$ = 25°C |
| Input High Voltage<br>   All Except XTLI<br>   XTLI | $V_{IH}$ | <br>+2.0<br>+4.0 | <br>–<br>– | <br>$V_{CC}$<br>$V_{CC}$ | | |
| Input Low Voltage | $V_{IL}$ | −0.3 | – | +0.8 | V | |
| Input Leakage Current<br>   RES, NMI | $I_{IN}$ | – | – | ±10.0 | μA | $V_{IN}$ = 0 to 5.0V |
| Input Low Current<br>   PA, PB, PC, PD | $I_{IL}$ | – | −1.0 | −1.6 | mA | $V_{IL}$ = 0.4V |
| Output High Voltage (Except XTLO) | $V_{OH}$ | +2.4 | – | $V_{CC}$ | V | $I_{LOAD}$ = −100 μA |
| Output Low Voltage | $V_{OL}$ | – | – | +0.4 | V | $I_{LOAD}$ = 1.6 mA |
| I/O Port Pull-Up Resistance<br>   PA0-PA7, PB0-PB7, PC0-PC7 | $R_L$ | 3.0 | 6.0 | 1.5 | Kohm | |
| Output Leakage Current (Three-State Off) | $I_{OUT}$ | – | – | ±10 | μA | |
| Input Capacitance<br>   XTLI, XTLO<br>   All Others | $C_{IN}$ | <br>–<br>– | <br>–<br>– | <br>50<br>10 | pF | $T_A$ = 25C<br>$V_{IN}$ = 0V<br>f = 1.0 MHz |
| Output Capacitance (Three-State Off) | $C_{OUT}$ | – | – | 10 | pF | $T_A$ = 25°C<br>$V_{IN}$ = 0V<br>f = 1.0 MHz |
| Power Dissipation (Outputs High) | $P_D$ | – | 750 | 1100 | mW | $T_A$ = 0°C |

**Notes:**
1. Typical values measured at $T_A$ = 25°C and $V_{CC}$ = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.

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## APPENDIX E
## TIMING REQUIREMENTS AND CHARACTERISTICS

### E.1 GENERAL NOTES

1. $V_{CC} = 5V \pm 5\%$, $0°C \leq T_A \leq 70°C$

2. A valid $V_{CC} - \overline{RES}$ sequence is required before proper operation is achieved.

3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.

4. All time units are nanoseconds, unless otherwise specified.

5. All capacitive loading is 130 pF maximum, except as noted below:

   | | |
   |---|---|
   | PA, PB | – 50 pF maximum |
   | PC (I/O Modes Only) | – 50 pF maximum |
   | PC6, PC7 (Full Address Mode) | – 130 pF maximum |

### E.2 CLOCK TIMING

| Symbol | Parameter | 1 MHz | | 2 MHz | | 3 MHz | |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max |
| $T_{CYC}$ | Cycle Time | 1000 | 10 μs | 500 | 10 μs | 333 | 10 μs |
| $T_{PWX1}$ | XTLI Input Clock Pulse Width XTLO = $V_{SS}$ | 500 ±25 | – | 250 ±10 | – | 167 ±10 | – |
| $T_{PW02}$ | Output Clock Pulse Width at Minimum $T_{CYC}$ | $T_{PWX1}$ | $T_{PWX1}$ ±25 | $T_{PWX1}$ | $T_{PWX1}$ ±20 | $T_{PWX1}$ | $T_{PWX1}$ ±20 |
| $T_R$, $T_F$ | Output Clock Rise, Fall Time | – | 25 | – | 15 | – | 15 |
| $T_{IR}$, $T_{IF}$ | Input Clock Rise, Fall Time | – | 10 | – | 10 | – | 10 |



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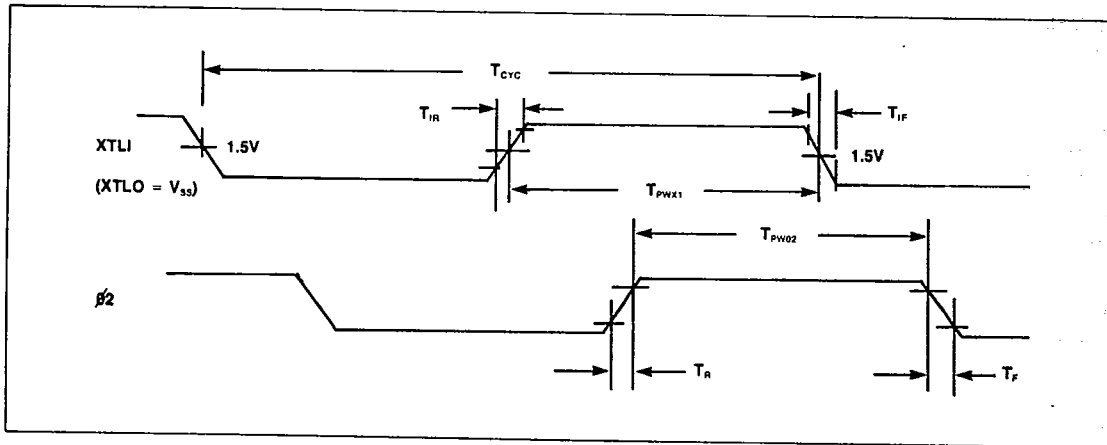
**T-49-17-06**

## E.3 I/O, EDGE DETECT, COUNTERS, AND SERIAL I/O TIMING

| Symbol | Parameter | 1 MHz | | 2 MHz | | 3 MHz | |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max |
| $T_{PDW}$[1] $T_{CMOS}$[1] $T_{PDDW}$ | Internal Write to Peripheral Data Valid<br>PA, PB, PC (TTL)<br>PA, PB, PC (CMOS)<br>PD | –<br>–<br>– | 500<br>1000<br>175 | –<br>–<br>– | 500<br>1000<br>150 | –<br>–<br>– | 333<br>666<br>135 |
| $T_{PDSU}$ | Peripheral Data Setup Time<br>PA, PB, PC<br>PD | 200<br>50 | –<br>– | 200<br>50 | –<br>– | 150<br>50 | –<br>– |
| $T_{PHA}$ | Peripheral Data Hold Time<br>PA, PB, PC<br>PD | 75<br>10 | –<br>– | 75<br>10 | –<br>– | 75<br>10 | –<br>– |
| $T_{EPW}$ | PA0-PA3 Edge Detect Pulse Width | $T_{CYC}$ | – | $T_{CYC}$ | – | $T_{CYC}$ | – |
| $T_{CPW}$ $T_{CD}$[1] | Counters A and B<br>PA4, PA5 Input Pulse Width<br>PA4, PA5 Output Delay | $T_{CYC}$<br>– | –<br>500 | $T_{CYC}$<br>– | –<br>500 | $T_{CYC}$<br>– | –<br>333 |
| $T_{PBLW}$ $T_{PLSU}$ $T_{PBLH}$ | Port B Latch Mode<br>PA0 Strobe Pulse Width<br>PB Data Setup Time<br>PB Data Hold Time | $T_{CYC}$<br>175<br>30 | –<br>–<br>– | $T_{CYC}$<br>150<br>30 | –<br>–<br>– | $T_{CYC}$<br>150<br>30 | –<br>–<br>– |
| $T_{PDW}$[1] $T_{CMOS}$[1] $T_{CPW}$ $T_{PDW}$[1] $T_{CMOS}$[1] | Serial I/O<br>PA6 XMTR (TTL)<br>PA6 XMTR (CMOS)<br>PA4 RCVR SR Clock Width<br>PA4 XMTR Clock –S/R Mode (TTL)<br>PA4 XMTR Clock –S/R Mode (CMOS) | –<br>–<br>4 $T_{CYC}$<br>–<br>– | 500<br>1000<br>–<br>500<br>1000 | –<br>–<br>4 $T_{CYC}$<br>–<br>– | 500<br>1000<br>–<br>500<br>1000 | –<br>–<br>4 $T_{CYC}$<br>–<br>– | 333<br>666<br>–<br>333<br>666 |

NOTES: 1. Maximum Load Capacitance: 50 pF; Passive Pull-Up Required.

### E.3.1 I/O, Edge Detect, Counter, and Serial I/O Timing



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**R65012**                                                    **One-Chip Microprocessor**
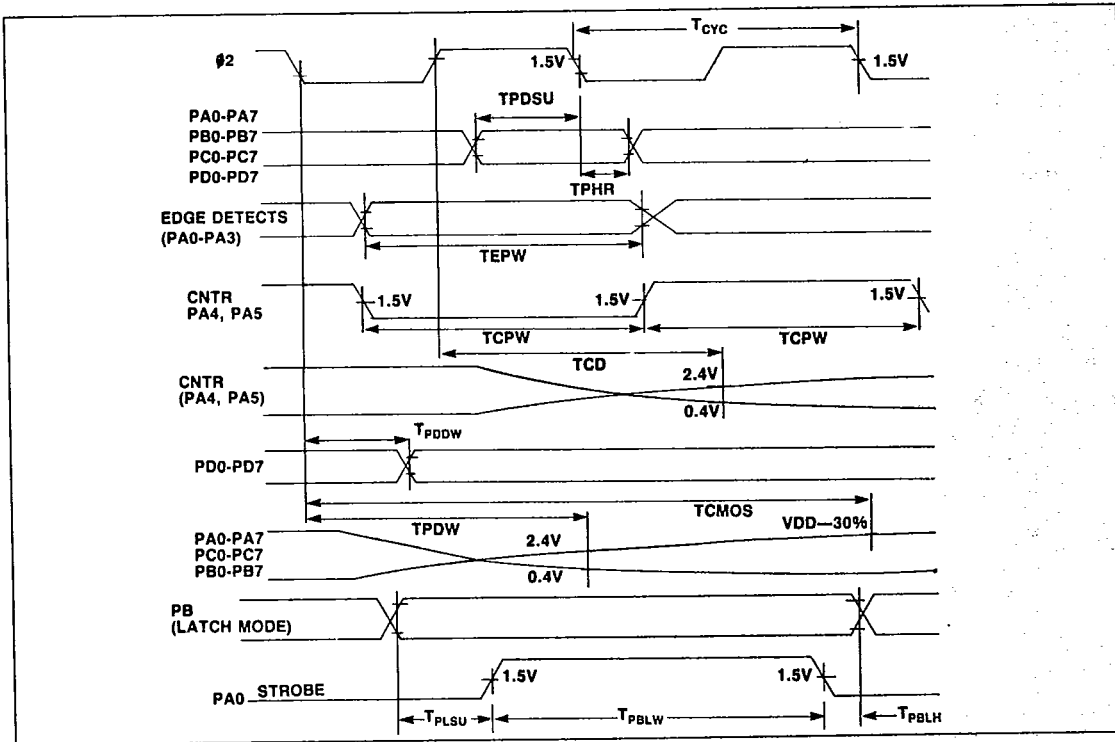
## E.4 MICROPROCESSOR TIMING (D0-D7, A0-A12, A15, SYNC, R/W)

| Symbol | Parameter | 1 MHz | | 2 MHz | | 3 MHz | |
|--------|-----------|-------|-----|-------|-----|-------|-----|
| | | Min | Max | Min | Max | Min | Max |
| $T_{RWS}$ | R/W Setup Time | – | 255 | – | 140 | – | 110 |
| $T_{ADS}$ | A0-A12, A15 Setup Time | – | 150 | – | 140 | – | 110 |
| $T_{DSU}$ | D0-D7 Data Setup Time | 50 | – | 35 | – | 25 | – |
| $T_{HR}$ | D0-D7 Read Hold Time | 10 | – | 10 | – | 10 | – |
| $T_{HW}$ | D0-D7 Write Hold Time | 30 | – | 30 | – | 30 | – |
| $T_{MOS}$ | D0-D7 Write Output Delay | – | 175 | – | 110 | – | 110 |
| $T_{SYN}$ | SYNC Setup Time | – | 225 | – | 175 | – | 110 |
| $T_{HA}$ | A0-A12, A15 Hold Time | 30 | – | 30 | – | 30 | – |
| $T_{HRW}$ | R/W Hold Time | 30 | – | 30 | – | 30 | – |
| $T_{ACC}$ | External Memory Access Time $T_{ACC} = T_{CYC} - T_F - T_{ADS} - T_{DSU}$ | – | $T_{ACC}$ | – | $T_{ACC}$ | – | $T_{ACC}$ |
| $T_{SYH}$ | SYNC Hold Time | 30 | – | 30 | – | 30 | – |

## E.4.1 Microprocessor Timing Diagram

R65012    **One-Chip Microprocessor**
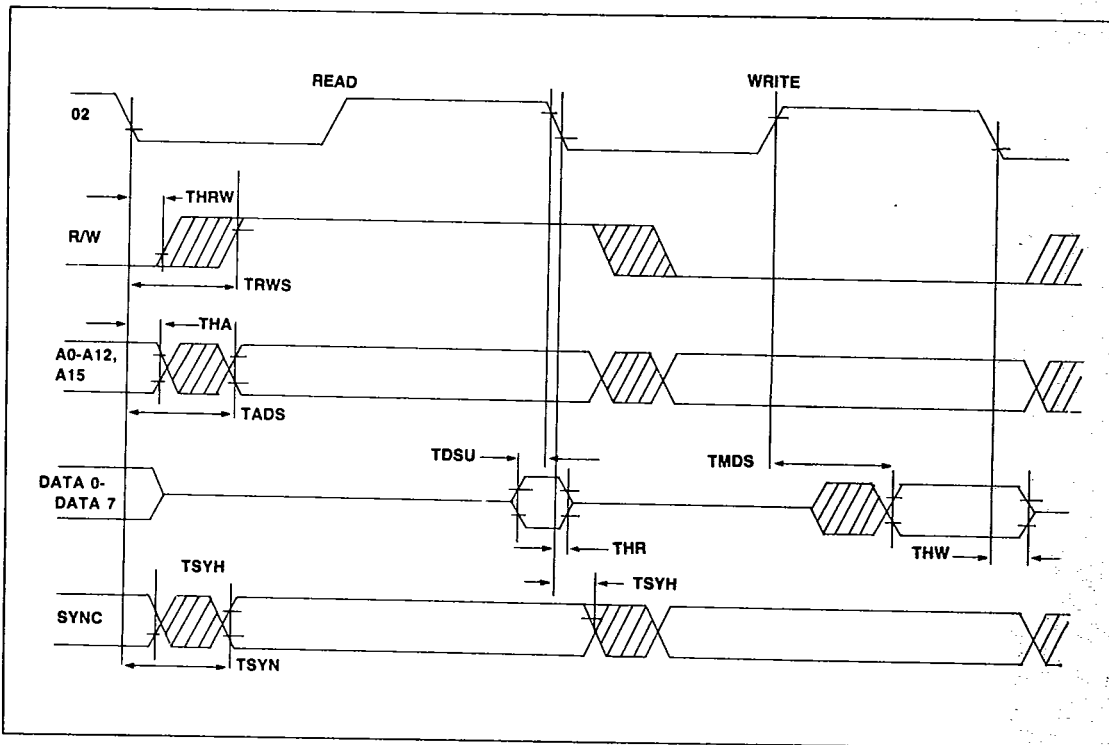
## PACKAGE DIMENSIONS

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### 64-PIN PLASTIC QUAD IN-LINE PACKAGE (QUIP)



| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 41.10 | 41.61 | 1.618 | 1.638 |
| B | 17.02 | 17.23 | 0.670 | 0.690 |
| C | 3.56 | 4.58 | 0.140 | 0.180 |
| D | 0.48 | 0.56 | 0.018 | 0.022 |
| E1 | 19.05 BSC | | 0.750 BSC | |
| E2 | 23.50 BSC | | 0.925 BSC | |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.18 | 0.33 | 0.007 | 0.013 |
| K1 | 2.92 | 3.18 | 0.115 | 0.125 |
| K2 | 4.83 | 5.34 | .0.190 | 0.210 |

R65012                                                    **One-Chip Microprocessor**
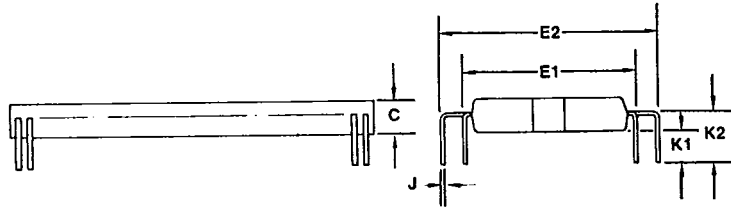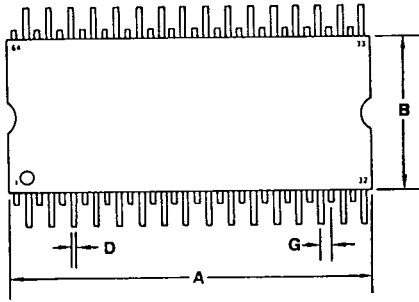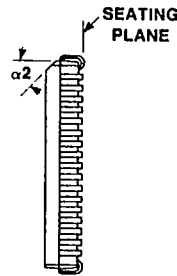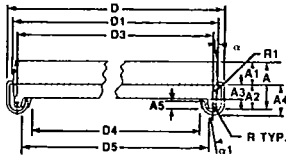
PACKAGE DIMENSIONS (CONT'D)                               T-49-17-06

## 68-PIN PLASTIC CHIP CARRIER (PCC)
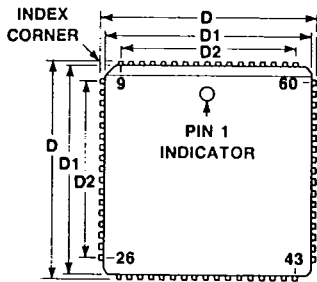


TOP VIEW

SIDE VIEW

SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)

CHAM. J × 45°
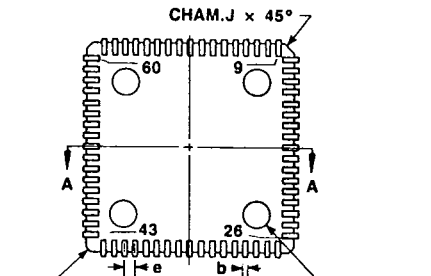
BOTTOM VIEW

CHAM.
h × 45°
3 PLCS

17 PINS
PER SIDE
EQUALLY
SPACES

EJECTOR PIN MARKS
4 PLCS BOTTOM OF
PACKAGE ONLY
(TYPICAL)

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 3.683 | 3.785 | .145 | .149 |
| A1 | 1.829 | 1.930 | .072 | .076 |
| A2 | 1.803 | 1.905 | .071 | .075 |
| A3 | 1.372 | 1.473 | .054 | .058 |
| A4 | 2.311 | 2.464 | .091 | .097 |
| A5 | 0.203 | 0.305 | .008 | .012 |
| b | 0.457 TYP | | .018 TYP | |
| D | 25.02 | 25.27 | .985 | .995 |
| D1 | 24.00 | 24.26 | .945 | .955 |
| D2 | 20.19 | 20.45 | .795 | .805 |
| D3 | 23.24 | 23.50 | .915 | .925 |
| D4 | 20.96 | 21.21 | .825 | .835 |
| D5 | 22.23 | 22.48 | .875 | .885 |
| e | 1.27 BSC | | .050 BSC | |
| h | 0.254 TYP | | .010 TYP | |
| J | 1.143 TYP | | .045 TYP | |
| α | 4° TYP | | 4° TYP | |
| α1 | 10° TYP | | 10° TYP | |
| α2 | 45° TYP | | 45° TYP | |
| R | 0.889 TYP | | .035 TYP | |
| R1 | 0.254 TYP | | .010 TYP | |