

HEX D-TYPE FLIP-FLOP WITH RESET; POSITIVE-EDGE TRIGGER

FEATURES

- Six edge-triggered D-type flip-flops
- Asynchronous master reset
- Output capability: standard
- I^{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT174 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT174 have six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the \overline{MR} input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n \overline{MR} to Q_n	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	17 13	18 17	ns ns
f_{max}	maximum clock frequency		99	69	MHz
C_i	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

GND = 0 V; $T_{amb} = 25 \text{ }^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

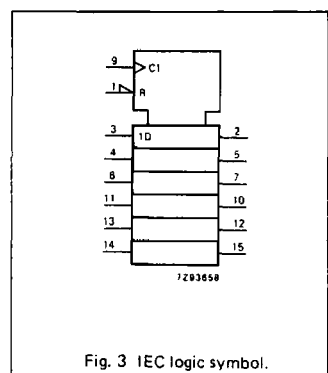
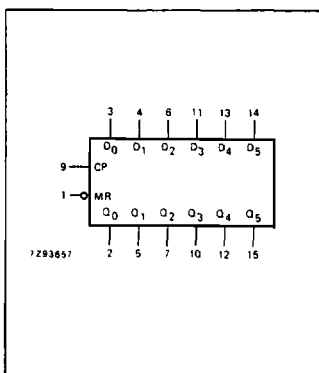
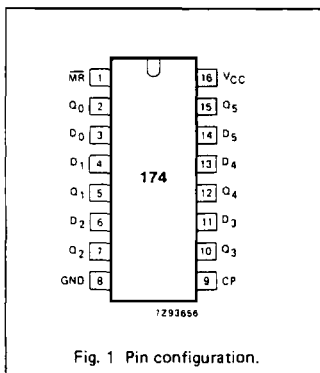
2. For HC the condition is $V_i = \text{GND to } V_{CC}$
 For HCT the condition is $V_i = \text{GND to } V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

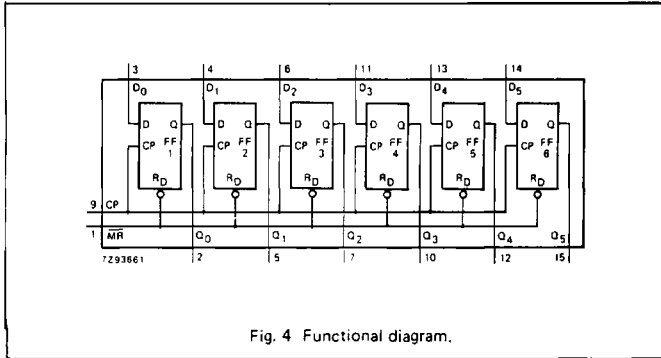
SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\overline{MR}	asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q_0 to Q_5	flip-flop outputs
3, 4, 6, 11, 13, 14	D_0 to D_5	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage



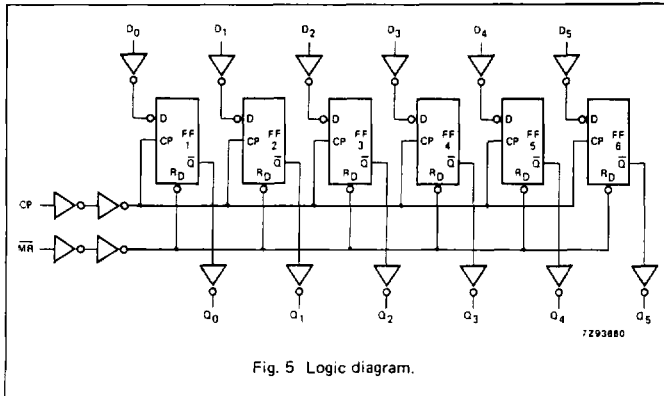
74HC/HCT174
MSI



FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	\overline{MR}	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition



DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		55 20 16	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig. 6
t _{PHL}	propagation delay MR to Q _n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t _W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t _W	master reset pulse width; LOW	80 16 14	12 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t _{rem}	removal time MR to CP	5 5 5	-11 -4 -3		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 7
t _{su}	set-up time D _n to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 8
t _h	hold time D _n to CP	3 3 3	-6 -2 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig. 8
f _{max}	maximum clock pulse frequency	6 30 35	30 90 107		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.25
CP	1.30
MR	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r - t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		21	35		44		53	ns	4.5	Fig. 6
t _{PHL}	propagation delay MR to Q _n		20	35		44		53	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t _W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t _W	master reset pulse width; LOW	20	7		25		30		ns	4.5	Fig. 7
t _{rem}	removal time MR to CP	12	-3		15		18		ns	4.5	Fig. 7
t _{su}	set-up time D _n to CP	16	4		20		24		ns	4.5	Fig. 8
t _h	hold time D _n to CP	5	-3		5		5		ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	30	63		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

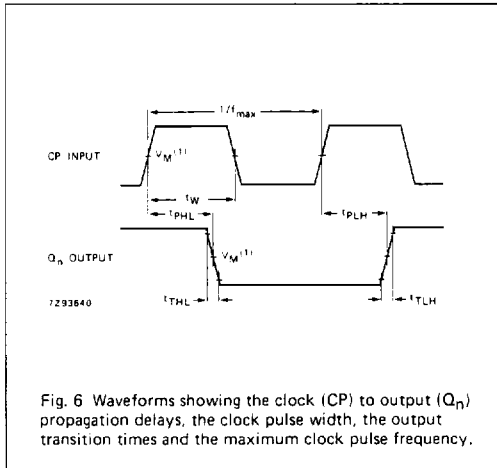


Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

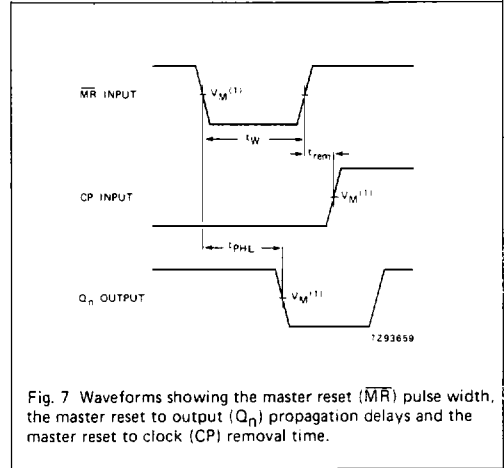


Fig. 7 Waveforms showing the master reset (\overline{MR}) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

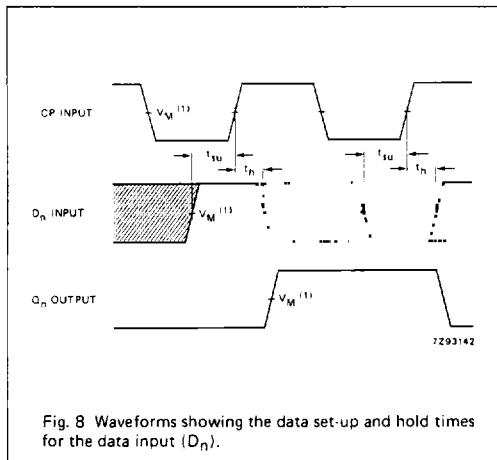


Fig. 8 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig. 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

- (1) HC : V_M = 50%; V_I = GND to V_{CC}.
- HCT: V_M = 1.3 V; V_I = GND to 3 V.