DATA SHEET

TEA1211TW
High efficiency auto-up/down DC-to-DC converter

Objective specification

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Philips
Semiconductors

PHILIPS

CONTENTS

High efficiency auto-up/down DC-to-DC converter

TEA1211TW

1 FEATURES

- I^2C-bus programmable output voltage range of 1.5 to 5.5 V
- Single inductor topology
- High efficiency up to 95% over wide load range
- Wide input voltage range; functional from 2.4 to 5.5 V
- 1.7 A maximum input/output current
- Low quiescent power consumption
- 600 kHz switching frequency
- Four integrated very low R_{DSon} power MOSFETs
- Synchronizable to external clock
- Externally adjustable current limit for protection and efficient battery use in case of dynamic loads
- Under-voltage lockout
- PWM-only option
- Shut-down current typical 1 μA
- Thermal protection
- 20-pin small outline HTSSOP20 package.

2 APPLICATIONS

- Stable output voltage from Lithium-Ion batteries
- Variable voltage source for Power Amplifier (PA) in cellular phones
- Wireless handsets
- Handheld instruments
- Portable computers.

3 GENERAL DESCRIPTION

The TEA1211TW is a fully integrated DC-to-DC auto-up/down converter circuit with an I^2C-bus interface. Efficient, compact and dynamic power conversion is achieved using a digitally controlled Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) like control concept, four integrated low R_{DSon} CMOS power switches with low parasitic capacitances, and fully synchronous rectification.

The combination of auto-up/down conversion, high efficiency and low switching noise makes the converter well suited to supply a power amplifier in a cellular phone. The output voltage can be programmed via the I^2C-bus to the exact voltage needed to achieve a certain output power level with optimal system efficiency, thus enhancing battery lifetime.

The TEA1211TW operates at 600 kHz switching frequency which enables the use of small-size external components. The switching frequency can be locked to an external high frequency clock. Deadlock is prevented by an on-chip undervoltage lockout circuit. An adjustable current limit enables efficient battery use even at high dynamic loads. Optionally, the device can be kept in Pulse Width Modulation mode regardless of the load applied.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1211TW	HTSSOP20	plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm	SOT527-1

5 QUICK REFERENCE DATA

T_{amb} = –40 to +85 °C; unless otherwise specified; all voltages with respect to ground; positive currents flow into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage levels						
V_o	output voltage		1.50	–	5.50	V
$V_{i(start)}$	start-up voltage	V_o = 3.5 V; I_L < 100 mA	2.30	2.40	2.50	V
V_i	input voltage		V_{start}	–	5.50	V
V_{uvlo}	undervoltage lockout level		–	V_{start} – 0.15	–	V
V_{fb}	feedback voltage level		1.20	1.25	1.30	V
V_{wdw}	output voltage window as % of V_o	PWM mode	1.5	2.0	3.0	%
Current levels						
I_q	quiescent current	no load	–	70	–	µA
I_{shdwn}	current in shut-down mode		–	1	2	µA
ΔI_{lim}	current limit deviation	I_{ILIM} = 1 A; note 1	–30	–	+30	%
$I_{i/o(max)}$	maximum continuous input/output current	T_{amb} < 20 °C	–	–	1.7	A
Power MOSFETs						
$R_{DSon(N)}$	drain-to-source on-state resistance NFETs	T_{amb} = 25 °C; V_i = 3.5 V	–	55	75	mΩ
$R_{DSon(P)}$	drain-to-source on-state resistance PFETs	T_{amb} = 25 °C; V_i = 3.5 V	–	55	75	mΩ
$R_{DSon(Pout)}$	drain-to-source on-state resistance between pins LXB and OUT	T_{amb} = 25 °C; V_o = 1.5 V	–	100	135	mΩ
Timing						
f_{sw}	switching frequency	PWM mode	450	600	750	kHz
$f_{i(sync)}$	sync input frequency		4.5	13	20	MHz
Digital levels						
V_{IL}	LOW-level input voltage pins SYNC/PWM, SHDWN, SCL and SDA		0	–	0.4	V
V_{IH}	HIGH-level input voltage pins SYNC/PWM, SHDWN, SCL and SDA	note 2	$0.6 \times V_i$	–	V_i + 0.3	V
Temperature						
T_{amb}	ambient temperature		–40	+25	+85	°C
T_{co}	internal cut-off temperature		120	135	150	°C

Notes

1. The current limit level is defined by the external R_{ILIM} resistor, see Chapter 11.
2. To avoid additional supply current, it is advised to use HIGH levels not lower than V_i – 0.5 V.

6 BLOCK DIAGRAM

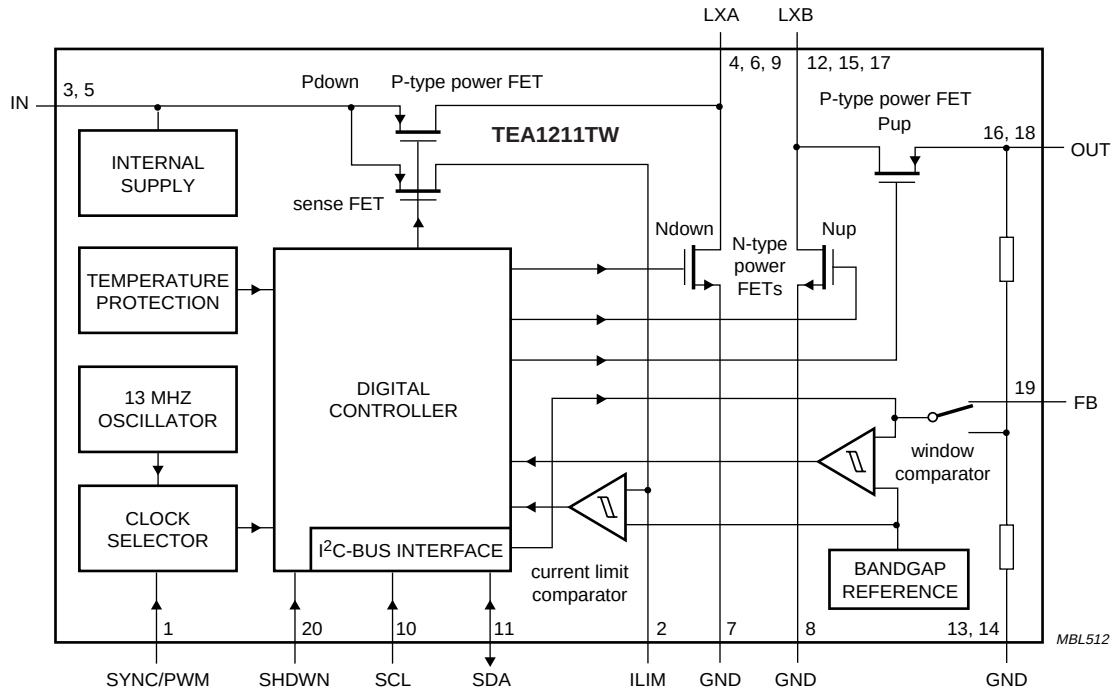


Fig.1 Block diagram.

7 PINNING INFORMATION

7.1 Pinning

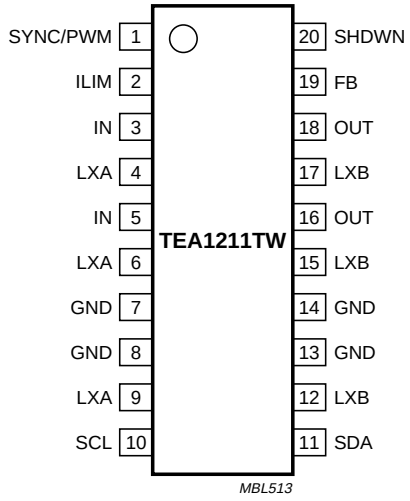


Fig.2 Pin configuration (Top view).

7.2 Pin description

Table 1 HTSSOP20 package

SYMBOL	PIN	DESCRIPTION
SYNC/PWM	1	synchronization clock input; PWM-only input
ILIM	2	current limit resistor connection
IN	3 and 5	input voltage
LXA	4, 6 and 9	inductor connection 1
GND	7, 8, 13 and 14	ground
SCL	10	I^{2}C-bus serial clock input
SDA	11	I^{2}C-bus serial data input/output
LXB	12, 15 and 17	inductor connection 2
OUT	16 and 18	output voltage
FB	19	feedback voltage input
SHDWN	20	shut-down input

8 FUNCTIONAL DESCRIPTION

8.1 Introduction

The TEA1211TW DC-to-DC converter can operate in PFM (discontinuous conduction) or PWM (continuous conduction) mode. All switching actions are determined by a digital control circuit which uses the output voltage level as its control input. This novel digital approach enables the use of a new pulse width and frequency modulation scheme, which ensures optimum power efficiency over the complete range of operation of the converter.

8.2 Control mechanism

Depending on load current and the V_i/V_o ratio, the controller chooses a mode of operation. When high output power is requested, the device will operate in PWM (continuous conduction) mode, which is a 2-phase cycle in Up mode as well as in Down mode. For small load currents the controller will switch over to PFM (discontinuous mode), which is either a 3 or 4-phase cycle depending on the input/output ratio (see Fig.3).

8.2.1 Pulse Width Modulation

Pulse Width Modulation results in minimum AC currents in the circuit components and hence optimum efficiency, cost, and EMC. In this mode, the output voltage is allowed to vary between two predefined voltage levels. As long as the output voltage stays within this so-called window, switching continues in a fixed pattern.

When the output voltage reaches one of the window borders, the digital controller immediately reacts by adjusting the duty cycle and inserting a current step in such a way that the output voltage stays within the window with higher or lower current capability. This approach enables very fast reaction to load variations.

Figure 4 shows the converter's response to a sudden load increase in the case of up-conversion. The upper trace shows the output voltage. The ripple on top of the DC level is a result of the current in the output capacitor, which changes in sign twice per cycle, times the capacitor's internal Equivalent Series Resistance (ESR).

After each ramp-down of the inductor current, for example, when the ESR effect increases the output voltage, the converter determines what to do in the next cycle. As soon as more load current is taken from the output the output voltage starts to decay. When the output voltage becomes lower than the low limit of the window, a corrective action is taken by a ramp-up of the inductor current during a much longer time. As a result, the DC current level is increased and normal PWM control can continue.

The output voltage (including ESR effect) is again within the predefined window.

8.2.2 Pulse Frequency Modulation

In low output power situations, the TEA1211TW will switch over to PFM (discontinuous conduction) mode operation in the event that PWM-only mode is not activated. In this mode, charge is transferred from the battery to the converter output in single pulses with a wait-phase in between. Regulation information from earlier PWM mode operation is used. This results in optimum inductor peak current levels in PFM mode, which are slightly larger than the inductor ripple current in PWM mode. As a result, the transition between PFM and PWM mode is optimal under all circumstances.

In PFM mode, TEA1211TW regulates the output voltage to the high window limit shown in Fig.5. Depending on the V_n/V_o ratio the controller decides for a 3 or 4-phase cycle, where the last phase is the wait-phase. When the input voltage almost equals the output voltage, one of the slopes of a 3-phase cycle will become so weak that the integral of the pulse (its charge) approaches zero, this means that no charge can be transferred. In this region the 4-phase cycle is used. See Fig.3.

8.2.3 Voltage window

Figure 5 depicts the spread of the output voltage window. The absolute value is mostly dependent on spread, while the actual window size is not affected. For one specific device, the output voltage will not vary more than 2% typically.

8.2.4 Switching Sequence

Refer to Fig.1. In Up mode the cycle starts by making Pdown and Nup conducting in the first phase. The second phase Nup opens and Pup starts conducting. In down-mode the cycle starts with in the first phase Pup and Pdown conducting. The second phase Pdown opens and Ndown starts conducting. In PFM these two phases are followed by a third or wait-phase that opens all switches except for Ndown, which is closed to prevent the coil from floating.

The stationary mode or 4-phase cycle, which only occurs in PFM, starts with in the first phase Pdown and Nup conducting. In the second phase Pdown and Pup conduct forming a short-cut from battery to output capacitor. In the third phase Pup and Ndown conduct. The fourth or wait-phase again opens all switches except for Ndown which is closed to prevent the coil from floating.

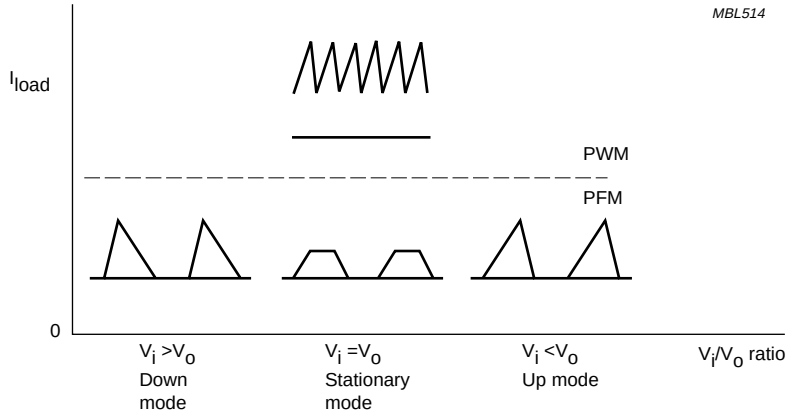


Fig.3 Waveform of I load coil current as a function of I_L and the V_i/V_o ratio.

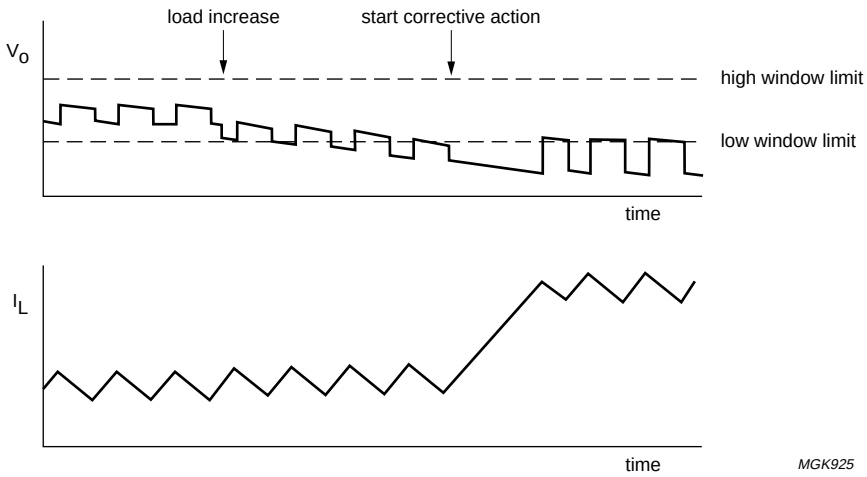


Fig.4 Response to load increase in Up mode.

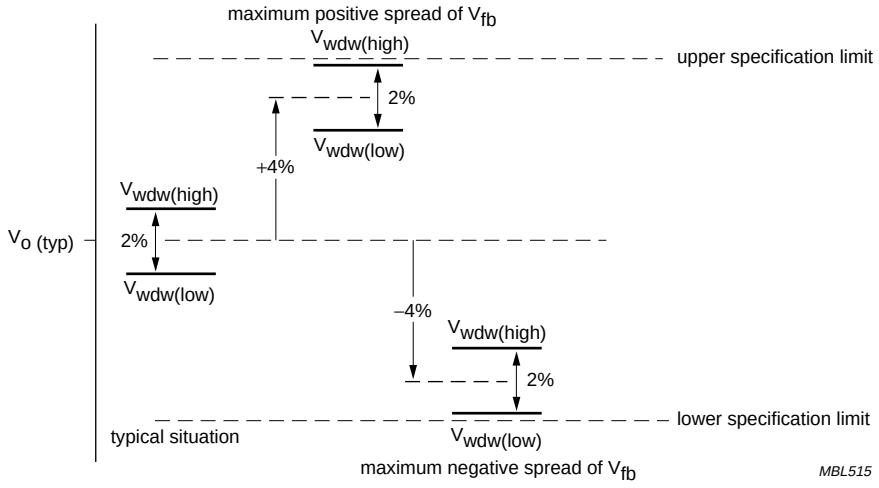


Fig.5 Output voltage window spread.

8.3 Adjustable output voltage

The output voltage of the up/down converter can be set to a fixed value by means of an external resistive divider. After start-up through this divider, dynamic control of the output voltage is made possible by use of the I^2C-bus. The output voltage can be programmed from 1.5 to 5.5 V in 40 increments, each of 0.1 V. For the power amplifiers, for example, the output voltage of the DC-to-DC converter can be adjusted to the output power to be transmitted by the power amplifier in order to obtain maximum system efficiency.

8.4 Start-up

If the input voltage exceeds the start voltage of 2.4 V the converter starts ramping-up the voltage at the output capacitor. Ramping stops when the desired level, set by the external resistors, is reached.

8.5 Undervoltage lockout

As a result of a too high load or disconnection of the input power source, the converter's input voltage can drop so low that normal regulation cannot be guaranteed. In that case, the device switches to a shut-down mode stopping the switching completely. Start-up is possible by crossing the start-up level again.

8.6 Shut-down

When the SHDWN pin is made HIGH, the converter disables all switches except for Ndown (see Fig.1) and power consumption is reduced to a few mA. Ndown is kept conducting to prevent the coil from floating.

8.7 Power switches

The power switches in the IC are two N-type and two P-type MOSFETs, having a typical pin-to-pin resistance of 85 mΩ. The maximum average current in the switches is 1.7 A at 70 °C ambient temperature.

8.8 Synchronous rectification

For optimal efficiency over the whole load range, synchronous rectifiers inside the TEA1211TW ensure that in PFM mode, during the phase when the coil current is decreasing, all inductor current will flow through the low-ohmic power MOSFETS. Special circuitry is included which detects when the inductor current reaches zero. Following this detection, the digital controller switches off the power MOSFET and proceeds with regulation. Negative currents are thus prevented.

8.9 PWM-only mode

When the SYNC/PWM pin is lifted HIGH, the TEA1211TW will use PWM regulation independent of the load applied. As a result, the switching frequency does not vary over the whole load range.

8.10 External synchronisation

If a high frequency clock is applied to the external synchronisation pin, the switching frequency in PWM mode will be exactly that frequency divided-by-22. PFM mode is no longer possible if an external clock is applied.

The quiescent current of the device increases when an external clock is applied. If no external synchronisation is necessary and the PWM-only option is not used, the SYNC/PWM pin must be connected to ground.

8.11 Current limiter

If the peak input current of the DC-to-DC converter exceeds its limit in PWM mode, current ramping is stopped immediately, and the next switching phase is entered. The current limitation protects the IC against overload conditions, inductor saturation, etc. The current limit level is user defined by the external resistor which must be connected between pin ILIM and pin GND.

8.12 Temperature protection

When the device operates in PWM mode, and the die temperature gets too high (typically 135 °C), the converter stops operating. It resumes operation when the device temperature falls below 135 °C again. As a result, low frequency cycling between the on and off-state will occur.

It should be noted that in the event of device temperatures around the temperature cut-off limit, the application exceeds the maximum specifications.

8.13 Serial interface (I^2C-bus)

The serial interface of the TEA1211TW is the I^2C-bus. A detailed description of the I^2C-bus specification, including applications, is given in the brochure: *"The I^2C-bus and how to use it"*, Philips order number: 9398 393 40011.

8.13.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, 2-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor (for best efficiency it is advised to use the input voltage of the converter). In bus configurations with ICs on different supply voltages, the pull-up resistors shall be connected to the highest supply voltage.

Data transfer may be initiated only when the bus is not busy.

The I²C-bus supports incremental addressing. This enables the system controller to read or write to multiple registers in only one I²C-bus action. The TEA1211TW supports the I²C-bus up to 400 kbits/s.

The I²C-bus system configuration is shown in Fig.6. A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’. The TEA1211TW is a slave only device.

8.13.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is inactive. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P); see Fig.7.

8.13.3 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal; see Fig.8.

8.13.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the receiver generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

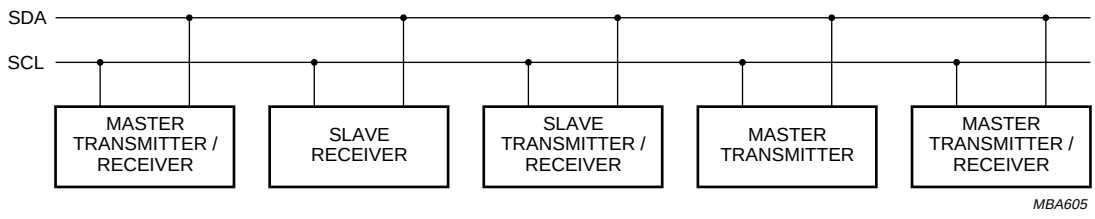


Fig.6 I²C-bus configuration.

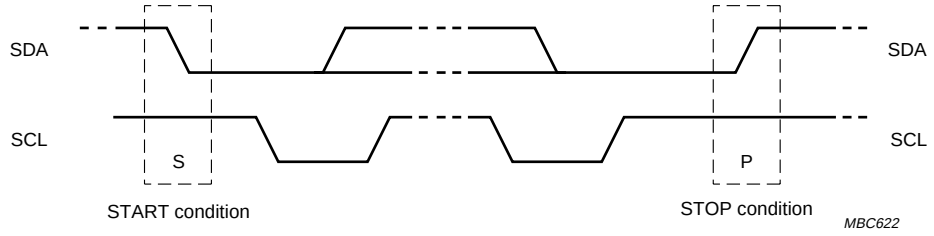


Fig.7 START and STOP conditions on the I²C-bus.

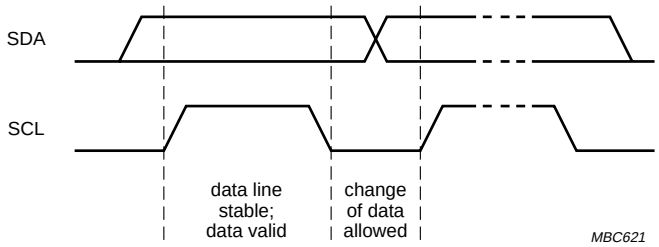


Fig.8 Bit transfer on the I²C-bus.

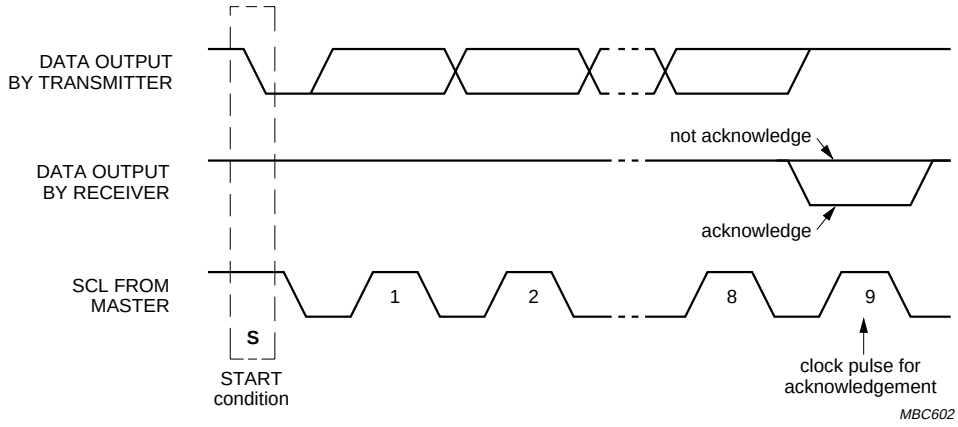


Fig.9 Acknowledge on the I²C-bus.

8.13.5 I²C-BUS PROTOCOL

8.13.5.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond, is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The (slave) address of the TEA1211TW is 0001 0000 (10H). The subaddress (or word address) is 0000 0000 (00H).

The TEA1211TW acts as a slave receiver only. Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line, enabling the TEA1211TW to send an acknowledge.

8.13.5.2 Data

The data is built-up of one byte.

Table 2 Data byte

SUBADDRESS	7	6	5	4	3	2	1	0
00H	0	0	CVLVL5	CVLVL4	CVLVL3	CVLVL2	CVLVL1	CVLVL0

Table 3 Description of the Data byte

BIT	SYMBOL	DESCRIPTION
7 and 6	–	These 2 bits must be logic 0.
5 to 0	CVLVL[5:0]	**Up/down converter output voltage level select.** These 6 bits are used to program the up/down converter output voltage level. The decimal value set by CVLVL[5:0] determines the number of 0.1 V increments that will be applied to the base voltage of 1.5 V. The valid range of CVLVL[5:0] is 0 to 40. The minimum voltage that can be selected is 1.5 V and the maximum voltage that can be selected is 5.5 V.

8.13.5.3 Write cycle

The I²C-bus configuration for the different TEA1211TW write cycles are shown in Fig.10. The word address is an 8-bit value that defines which register is to be accessed next.

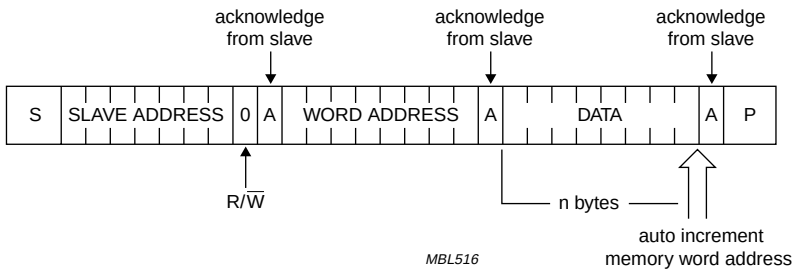


Fig.10 Master transmits to slave receiver (write mode).

9 LIMITING VALUES

In accordance with the Absolute Maximum Rate System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	voltage on any pin with respect to GND	shut-down mode	–0.5	+6.0	V
		operational mode	–0.5	+5.5	V
P_{tot}	total internal power dissipation		–	1000	mW
T_j	junction temperature		–40	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–40	+125	°C
V_{esd}	electrostatic discharge voltage	notes 1 and 2	class II	–	

Note

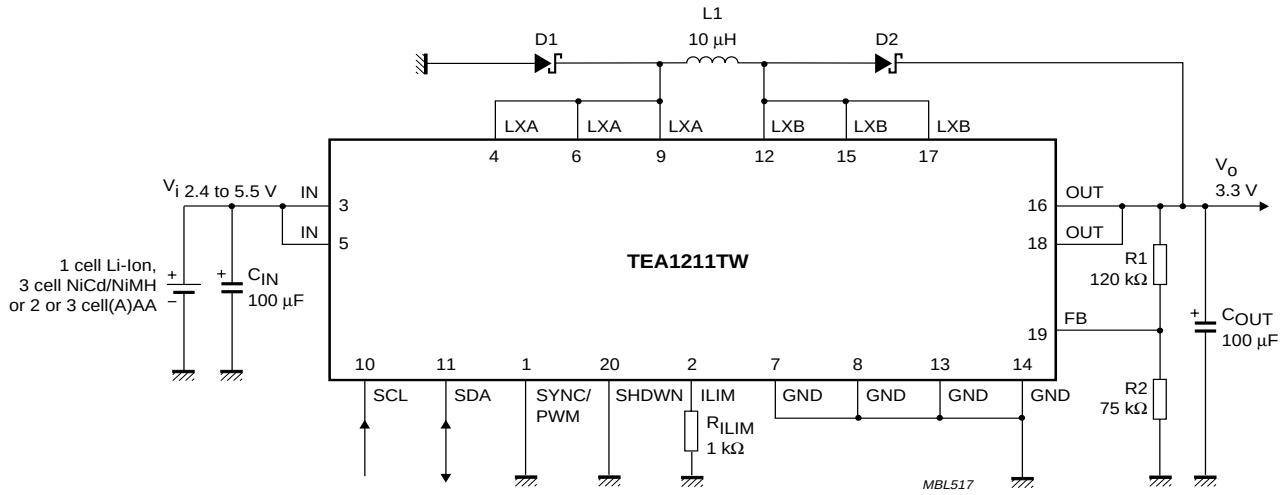
1. Human Body Model (HBM): equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor.
2. Machine Model (MM): equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	TYPE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	50	K/W

11 APPLICATION INFORMATION

11.1 Typical Li-Ion, 2 or 3 cell application with I²C-bus programming



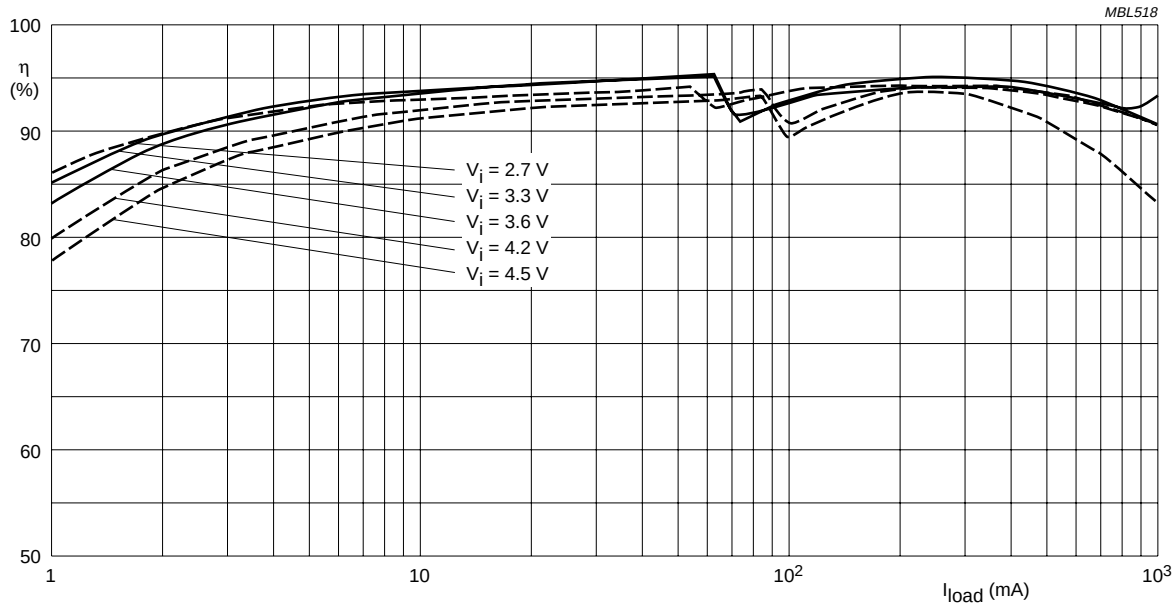
The combination of the feedback resistances R1 and R2 in parallel should be approximately 50 kΩ.

When the I²C-bus interface is used for programming the output voltage, the SCL and SDA pins must be connected to a positive supply using pull-up resistors (see Section 8.13.1). Note the V_{IH} level (see Chapter 5). If the I²C-bus interface is not used, connect pins SCL and SDA to ground.

No external clock is applied.

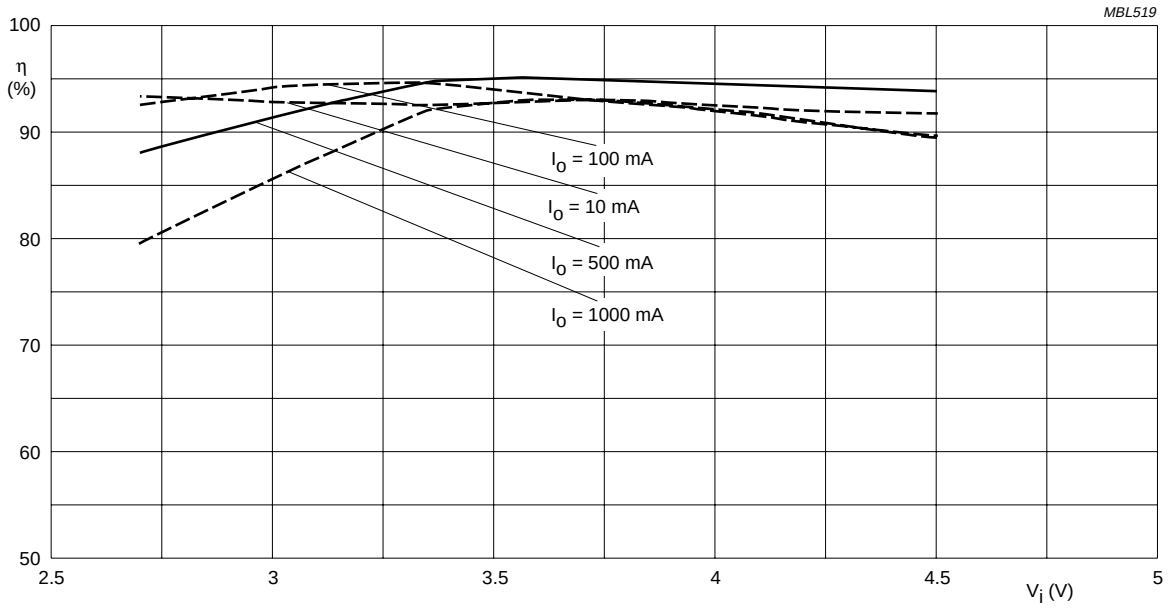
Pins should never be left open-circuit.

Fig.11 Typical auto-up/down converter application.



V_o = 3.3 V
L1 = 10 µH (TDK SLF7032 series)

Fig.12 Efficiency versus load current.



V_o = 3.3 V
L1 = 10 µH (TDK SLF7032 series)

Fig.13 Efficiency versus input voltage.

11.2 Component selection

11.2.1 INDUCTOR

The inductor should have a low ESR to reduce losses and must be able to handle the peak currents without saturating.

Table 4 Inductor selection

COMPONENT	VALUE	TYPE	SUPPLIER
L1	6.8 μH	DO3316-682	Coilcraft
	10 μH	SLF7032T-100M1R4	TDK

11.2.2 CAPACITOR

For the output capacitor, Equivalent Series Resistance (ESR) is critical. The output voltage ripple is determined by the product of the current through the output capacitor and its ESR. The lower the ESR, the smaller the ripple. A too low ESR however could result in unstable operation.

Table 5 Capacitor selection

COMPONENT	VALUE	TYPE	SUPPLIER
C_{IN} or C_{OUT}	100 μF/10 V	TPS-series	AVX
		594D-series	Vishay/Sprague

If the I^2C-bus interface is used to program large voltage steps at the output, it is preferable to increase the value of the input capacitor. This will prevent the undervoltage lockout level being triggered because of the large current peaks drawn from this capacitor.

Table 6 Input capacitor selection when the I^2C-bus is used

COMPONENT	VALUE	TYPE	SUPPLIER
C_{IN}	470 μF/10 V	TPS-series	AVX
		594D-series	Vishay/Sprague

11.2.3 SCHOTTKY DIODES

The Schottky diodes provide a lower voltage drop during the break-before-make time of the internal power FETs. It is advised to use Schottky diodes with fast recovery times.

Table 7 Schottky diode selection

COMPONENT	TYPE	SUPPLIER
D1 or D2	PRLL5819	Philips

11.2.4 Feedback resistors

The feedback resistors (R1 and R2) are used to set the fixed output voltage. Even if the I^2C-bus is used for programming the output voltage, external resistors are required for start-up. The ratio of the two resistors can be calculated by:

$$\frac{R1}{R2} = \frac{V_o}{V_{ref}} - 1 \text{ ; where } V_{ref} = V_{fb} \text{ (see Chapter 5)}$$

The two resistors in parallel should have a value of approximately 50 kΩ.

$$\frac{1}{R1} + \frac{1}{R2} = \frac{1}{50\ k\Omega}$$

11.2.5 Current Limiter

The maximum input peak current can be set by the current limiter as follows:

$$R_{ILIM} = \frac{1250}{I_{i(max)(pk)}}$$

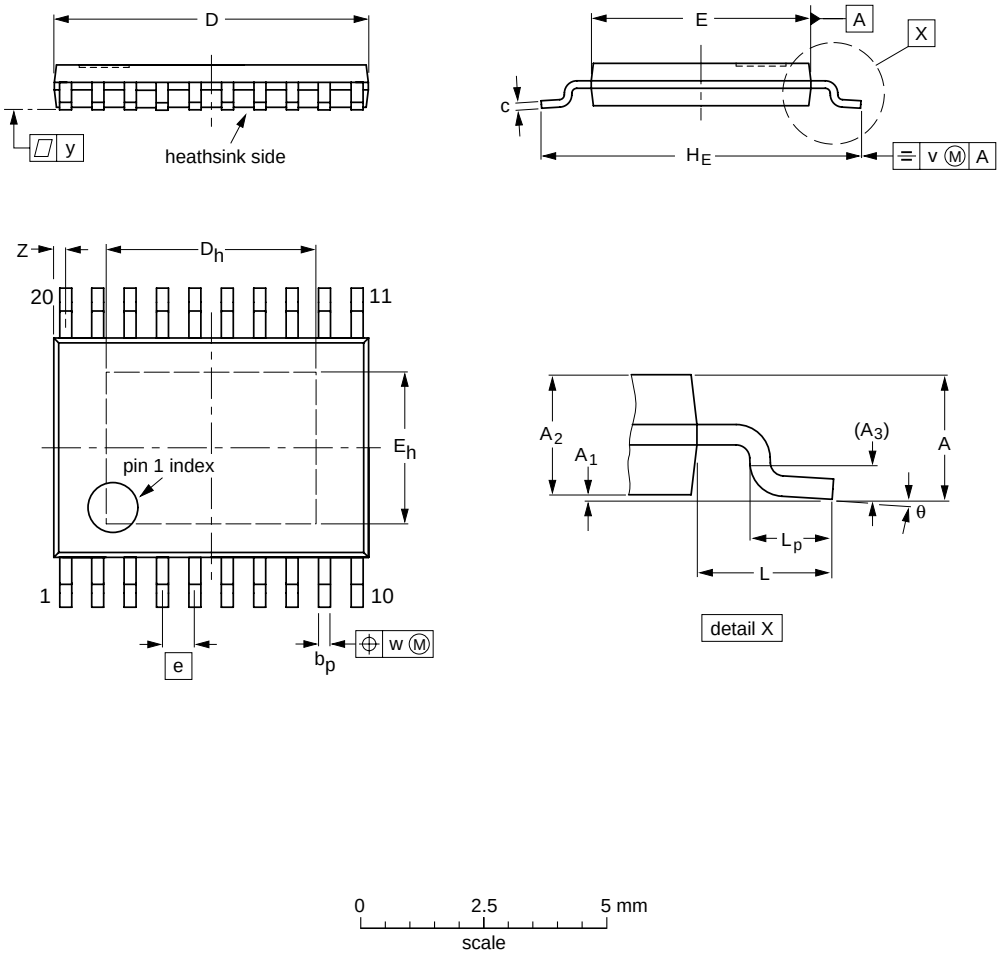
Note: The output current is not limited; in the event of down-conversion, the output current will be higher than the input current, while the maximum continuous output current is not allowed to exceed 1.7 A (rms) at 70 °C.

Table 8 Resistor selection

COMPONENT	VALUE	TYPE
R1, R2	V_o dependent	SMD 1% tolerance
R_{ILIM}	I_{ILIM} dependent	SMD 1% tolerance
R3, R4	10 kΩ	SMD

12 PACKAGE OUTLINE

HTSSOP20: plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm **SOT527-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.20 0.09	6.6 6.4	4.3 4.1	4.5 4.3	3.1 2.9	0.65	6.6 6.2	1.0	0.75 0.50	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT527-1						~~99-11-12~~ 00-07-12

13 SOLDERING

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

14 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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