PLESSEY Semiconductors — ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV4330 MV4332

CMOS/LSI 30/32-BIT STATIC SHIFT REGISTERS WITH PARALLEL TRUE/COMPLEMENT OUTPUTS

The MV4330 and MV4332 are CMOS/LSI 30 and 32-bit static shift registers incorporating selectable true/complement outputs for each bit. These devices are well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. One of these devices can drive four 7-segment displays or two 14-segment alpha-numeric displays plus decimal points or two 16-segment alpha-numeric displays directly.

The devices are available in 40-pin plastic DIL (DP) package.

FEATURES

- Direct LCD Drive
- CMOS Low Power (1 μA)
- 3 to 18 Volt Operation
- On-Chip Wave-Shaping
- High Speed (Typ. 3 MHz) Shift Register

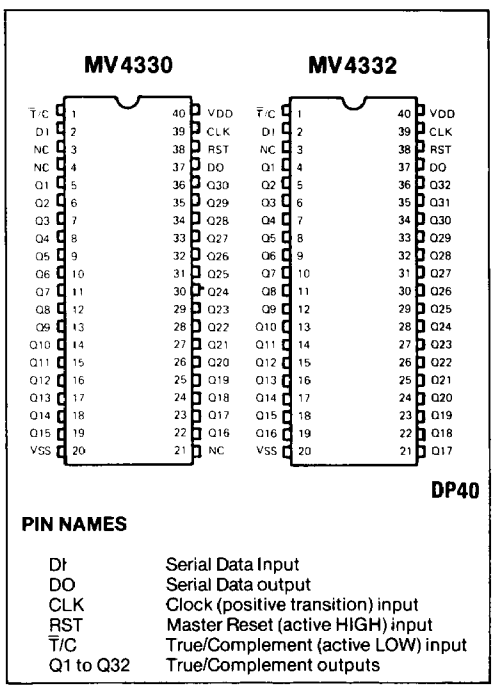

Fig.1 Pin connections (top view)

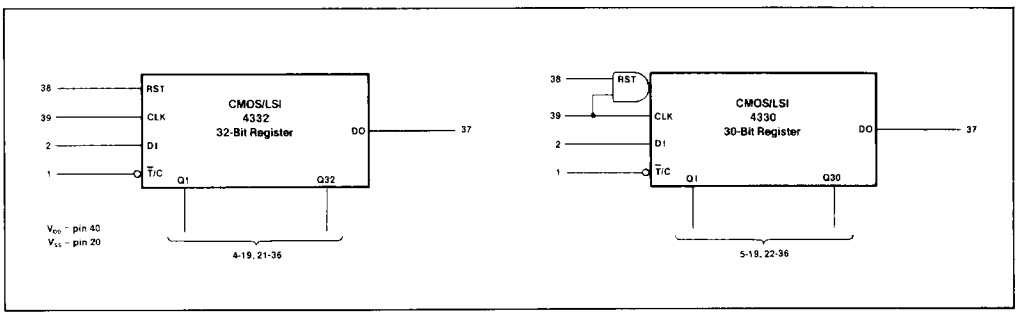

Fig.2 Block diagrams

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	VO Volts	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Quiescent Device Current		I_L			5	–	0.5	50	uA
					10	–	1	100	
Output Voltage — Low-Level		V_{OL}			5	–	0	0.01	V
					10	–	0	0.01	
Output Voltage — High-Level		V_{OH}			5	4.99	5	–	
					10	9.99	10	–	
Noise Immunity (Any Input)		V_{NL}		0.8	5	1.5	2.25	–	V
				1.0	10	3	4.5	–	
		V_{NH}		4.2	5	1.5	2.25	–	
				9.0	10	3	4.5	–	
Output Drive Current	D OUT	I_{DN}	N-Channel	0.5	5	0.8	1.7	–	mA
				0.5	10	1.0	3.0	–	
		I_{DP}	P-Channel	4.5	5	−0.35	−0.9	–	
				9.5	10	−0.8	−1.9	–	
	Q OUT	I_{DN}	N-Channel	0.5	10	50	250	–	uA
		I_{DP}	P-Channel	9.5	10	−50	−250	–	
Input Current		I_I				–	10	–	pA

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $C_L = 50pF$
All input rise and fall times = 20ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Propagation Delay Time	t_{PHL} t_{PLH}		10	–	300	–	ns
Transition Time	t_{THL}	D OUT (CL=50pF)	10	–	70	130	ns
	t_{TLH}	Q OUT (CL=15pF)	10	–	300	–	ns
Maximum Clock Frequency	f_{CL}		10	1.0	3.0	–	MHz
Minimum Clock Pulse Width	t_{WL} t_{WH}		10	–	200	–	ns
Minimum Reset Pulse Width	$t_{WH(R)}$		10	–	200	–	ns
Input Capacitance	CI	Any Input		–	5	–	pF

Note 1.Voltages with respect to V_{SS}
Note 2.Typical temperature coefficient for all values = 0.3%/°C