



**128K x 36, 256K x 18,
3.3V Synchronous ZBT™ SRAMs
2.5V I/O, Burst Counter,
Flow-Through Outputs**

**IDT71V2557S
IDT71V2559S
IDT71V2557SA
IDT71V2559SA**

Features

- ◆ 128K x 36, 256K x 18 memory configurations
- ◆ Supports high performance system speed - 100 MHz (7.5 ns Clock-to-Data Access)
- ◆ ZBT™ Feature - No dead cycles between write and read cycles
- ◆ Internally synchronized output buffer enable eliminates the need to control \overline{OE}
- ◆ Single R/\overline{W} (READ/WRITE) control pin
- ◆ 4-word burst capability (Interleaved or linear)
- ◆ Individual byte write (\overline{BW}_1 - \overline{BW}_4) control (May tie active)
- ◆ Three chip enables for simple depth expansion
- ◆ 3.3V power supply ($\pm 5\%$), 2.5V ($\pm 5\%$) I/O Supply (V_{DDO})
- ◆ Optional-Boundary Scan JTAG Interface (IEEE 1149.1 complaint)
- ◆ Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TOFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA)

Description

The IDT71V2557/59 are 3.3V high-speed 4,718,592-bit (4.5 Mega-bit) synchronous SRAMs organized as 128K x 36 / 256K x 18. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and on the next clock cycle the associated data cycle occurs, be

it read or write.

The IDT71V2557/59 contain address, data-in and control signal registers. The outputs are flow-through (no output data register). Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable (\overline{CEN}) pin allows operation of the IDT71V2557/59 to be suspended as long as necessary. All synchronous inputs are ignored when (\overline{CEN}) is high and the internal device registers will hold their previous values.

There are three chip enable pins (\overline{CE}_1 , CE_2 , \overline{CE}_2) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/\overline{LD} is low, no new memory operation can be initiated. However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state one cycle after the chip is deselected or a write is initiated.

The IDT71V2557/59 have an on-chip burst counter. In the burst mode, the IDT71V2557/59 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the \overline{LBO} input pin. The \overline{LBO} pin selects between linear and interleaved burst sequence. The ADV/\overline{LD} signal is used to load a new external address ($ADV/\overline{LD} = \text{LOW}$) or increment the internal burst counter ($ADV/\overline{LD} = \text{HIGH}$).

The IDT71V2557/59 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TOFP) as well as a 119 ball grid array (BGA) and a 165 fine pitch ball grid array (fBGA).

Pin Description Summary

A ₀ -A ₁₇	Address Inputs	Input	Synchronous
\overline{CE}_1 , CE_2 , \overline{CE}_2	Chip Enables	Input	Synchronous
\overline{OE}	Output Enable	Input	Asynchronous
R/\overline{W}	Read/Write Signal	Input	Synchronous
\overline{CEN}	Clock Enable	Input	Synchronous
\overline{BW}_1 , \overline{BW}_2 , \overline{BW}_3 , \overline{BW}_4	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
ADV/\overline{LD}	Advance burst address / Load new address	Input	Synchronous
\overline{LBO}	Linear / Interleaved Burst Order	Input	Static
TMS	Test Mode Select	Input	Synchronous
TDI	Test Data Input	Input	Synchronous
TCK	Test Clock	Input	N/A
TDO	Test Data Output	Output	Synchronous
\overline{TRST}	JTAG Reset (Optional)	Input	Asynchronous
ZZ	Sleep Mode	Input	Synchronous
I/O ₀ -I/O ₃₁ , I/OP ₁ -I/OP ₄	Data Input / Output	I/O	Synchronous
V _{DD} , V _{DDO}	Core Power, I/O Power	Supply	Static
V _{SS}	Ground	Supply	Static

4878 tbl 01

OCTOBER 2004

Pin Definitions⁽¹⁾

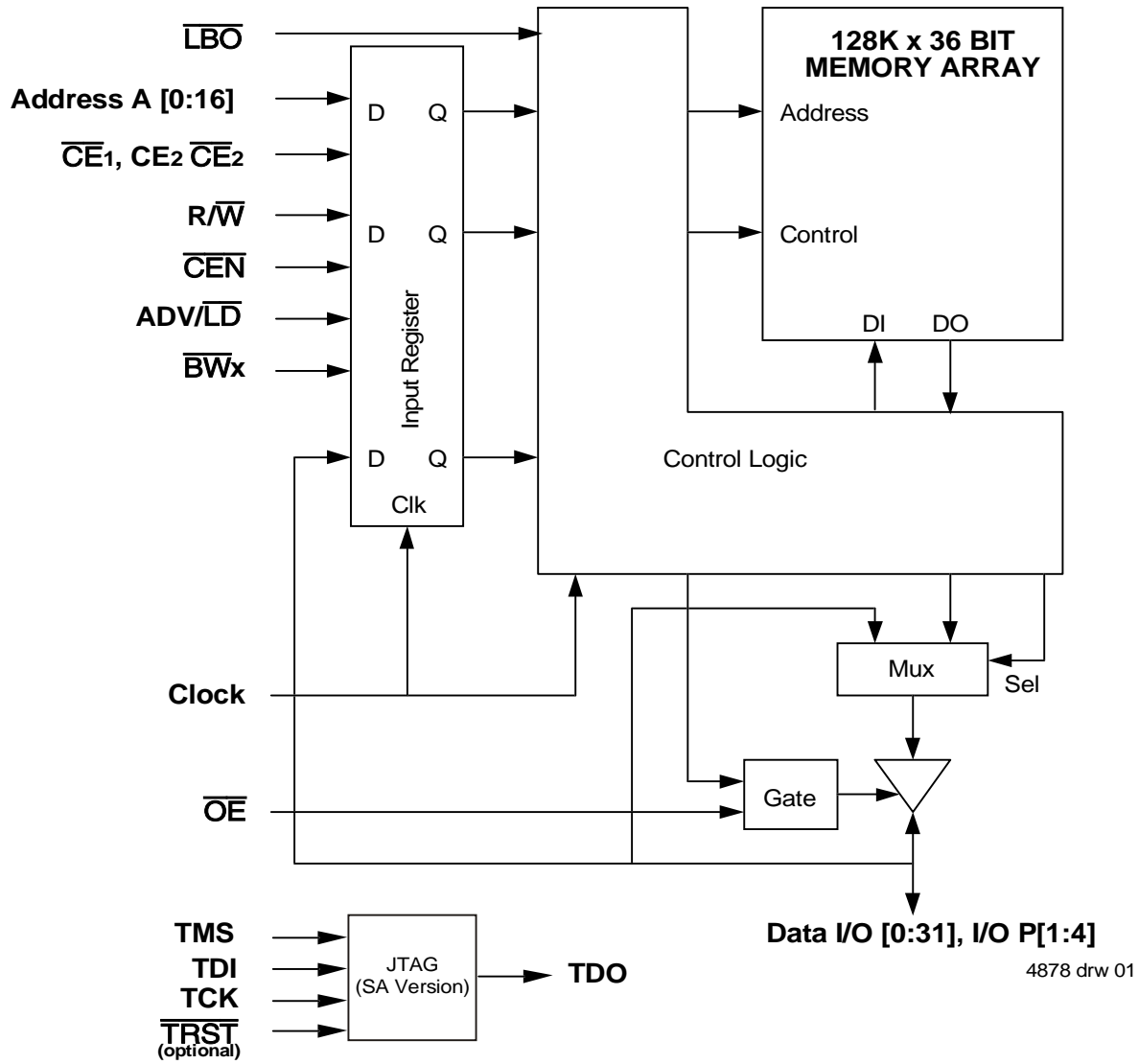
Symbol	Pin Function	I/O	Active	Description
A0-A17	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/LD low, \overline{CEN} low, and true chip enables.
ADV/LD	Advance / Load	I	N/A	ADV/LD is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/LD is low with the chip deselected, any burst in progress is terminated. When ADV/LD is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/LD is sampled high.
R/W	Read / Write	I	N/A	R/W signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place one clock cycle later.
\overline{CEN}	Clock Enable	I	LOW	Synchronous Clock Enable Input. When \overline{CEN} is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of \overline{CEN} sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, \overline{CEN} must be sampled low at rising edge of clock.
$\overline{BW1}$ - $\overline{BW4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. Each 9-bit byte has its own active low byte write enable. On load write cycles (When R/W and ADV/LD are sampled low) the appropriate byte write signal ($\overline{BW1}$ - $\overline{BW4}$) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/W is sampled high. The appropriate byte(s) of data are written into the device one cycle later. $\overline{BW1}$ - $\overline{BW4}$ can all be tied low if always doing write to the entire 36-bit word.
$\overline{CE1}$, $\overline{CE2}$	Chip Enables	I	LOW	Synchronous active low chip enable. $\overline{CE1}$ and $\overline{CE2}$ are used with CE2 to enable the IDT71V2557/59. ($\overline{CE1}$ or $\overline{CE2}$ sampled high or CE2 sampled low) and ADV/LD low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a one cycle deselect, i.e., the data bus will tri-state one clock cycle after deselect is initiated.
CE2	Chip Enable	I	HIGH	Synchronous active high chip enable. CE2 is used with $\overline{CE1}$ and $\overline{CE2}$ to enable the chip. CE2 has inverted polarity but otherwise identical to $\overline{CE1}$ and $\overline{CE2}$.
CLK	Clock	I	N/A	This is the clock input to the IDT71V2557/59. Except for \overline{OE} , all timing references for the device are made with respect to the rising edge of CLK.
I/O0-I/O31 I/OP1-I/OP4	Data Input/Output	I/O	N/A	Data input/output (I/O) pins. The data input path is registered, triggered by the rising edge of CLK. The data output path is flow-through (no output register).
\overline{LBO}	Linear Burst Order	I	LOW	Burst order selection input. When \overline{LBO} is high the Interleaved burst sequence is selected. When \overline{LBO} is low the Linear burst sequence is selected. \overline{LBO} is a static input, and it must not change during device operation..
\overline{OE}	Output Enable	I	LOW	Asynchronous output enable. \overline{OE} must be low to read data from the 71V2557/59. When \overline{OE} is HIGH the I/O pins are in a high-impedance state. \overline{OE} does not need to be actively controlled for read and write cycles. In normal operation, \overline{OE} can be tied low.
TMS	Test Mode Select	I	N/A	Gives input command for TAP controller. Sampled on rising edge of TDK. This pin has an internal pullup.
TDI	Test Data Input	I	N/A	Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup.
TCK	Test Clock	I	N/A	Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK. This pin has an internal pullup.
TDO	Test Data Output	O	N/A	Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.
\overline{TRST}	JTAG Reset (Optional)	I	LOW	Optional Asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used \overline{TRST} can be left floating. This pin has an internal pullup.
ZZ	Sleep Mode	I	HIGH	Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V2557/2559 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown
VDD	Power Supply	N/A	N/A	3.3V core power supply.
VDDQ	Power Supply	N/A	N/A	2.5V I/O Supply.
VSS	Ground	N/A	N/A	Ground.

NOTE:

1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

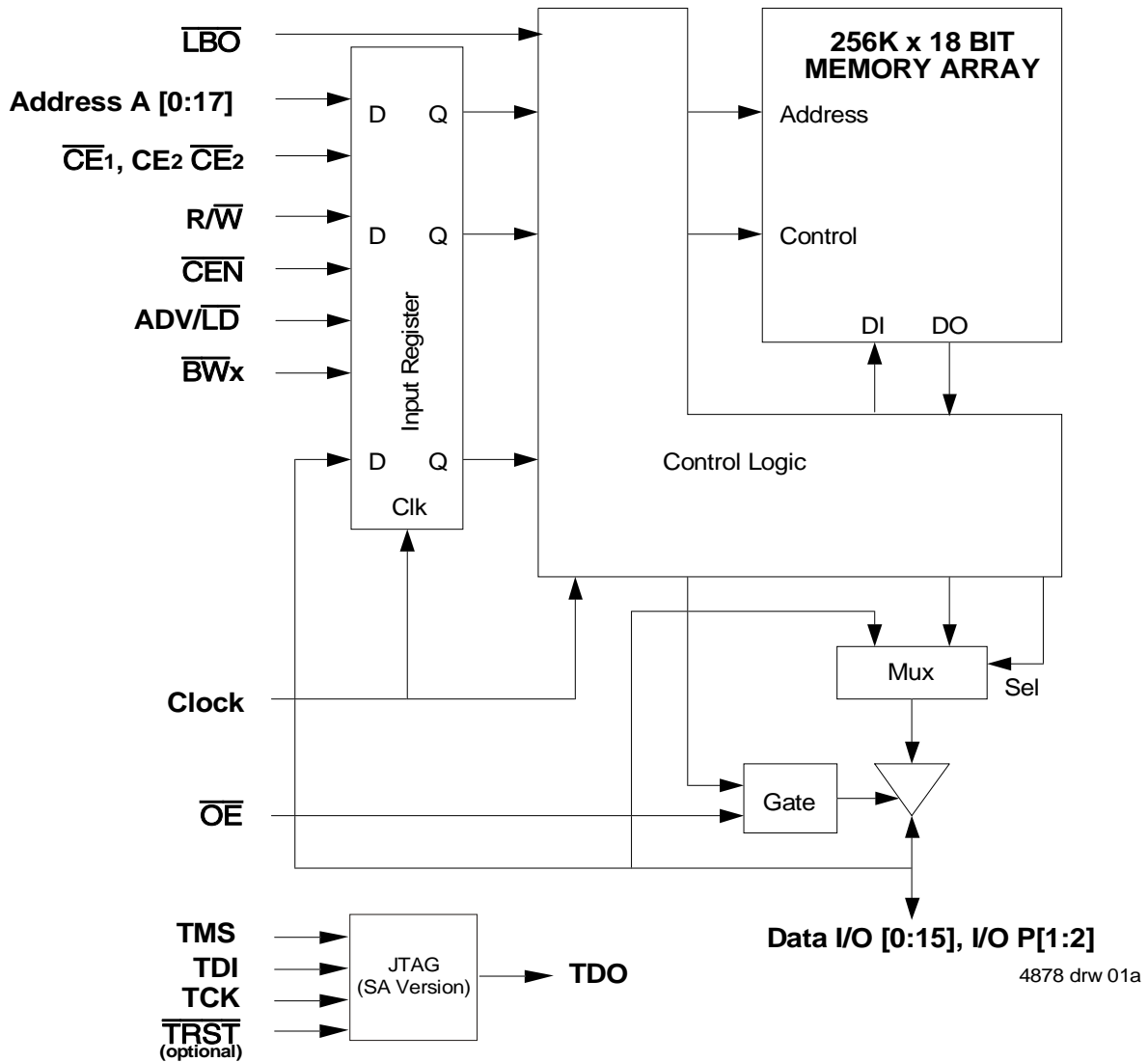
4878 tbl 02

Functional Block Diagram — 128K x 36



4878 drw 01

Functional Block Diagram — 256K x 18



Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V _{DDQ}	I/O Supply Voltage	2.375	2.5	2.625	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage - Inputs	1.7	—	V _{DD} + 0.3	V
V _{IH}	Input High Voltage - I/O	1.7	—	V _{DDQ} + 0.3 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

4878 tbl 03

NOTES:

- V_{IL} (min.) = -1.0V for pulse width less than t_{cy}/2, once per cycle.
- V_{IH} (max.) = +6.0V for pulse width less than t_{cy}/2, once per cycle.

Recommended Operating Temperature and Supply Voltage

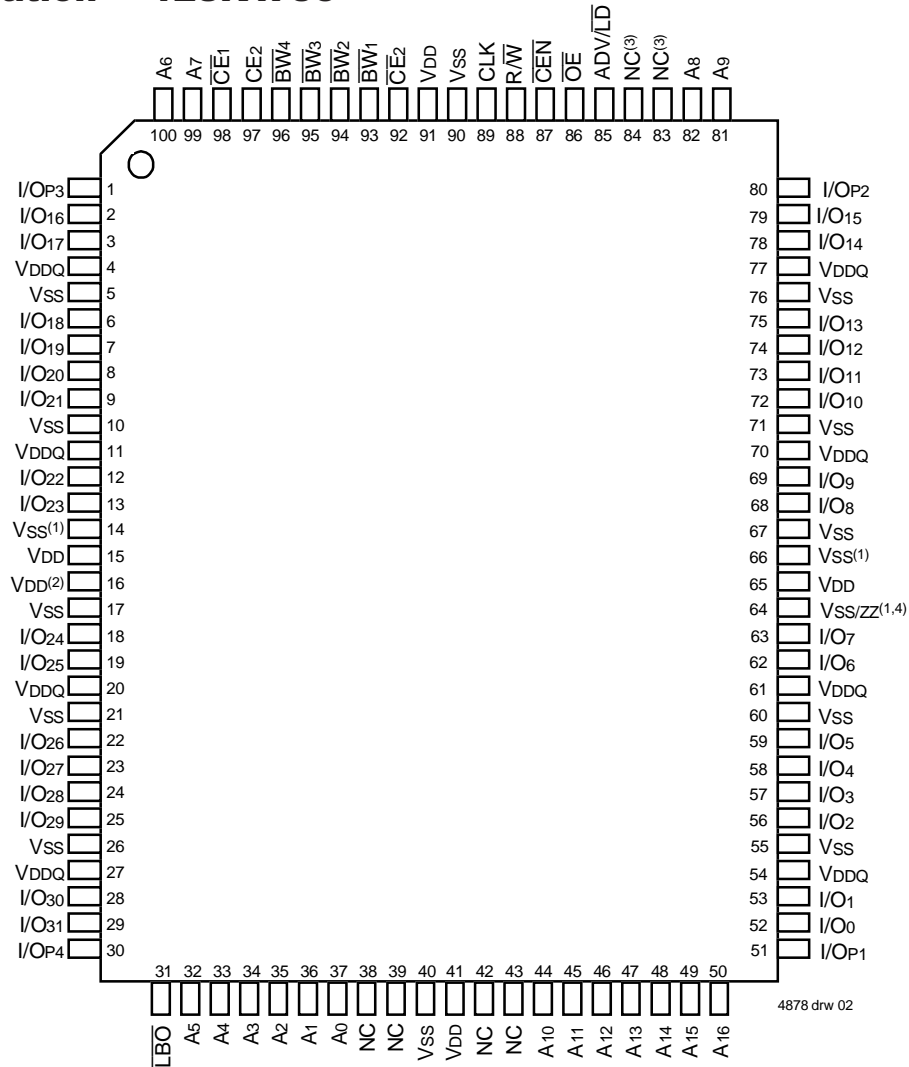
Grade	Temperature ⁽¹⁾	V _{SS}	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	2.5V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	2.5V±5%

NOTE:

4878 tbl 05

1. T_A is the "instant on" case temperature.

Pin Configuration — 128K x 36

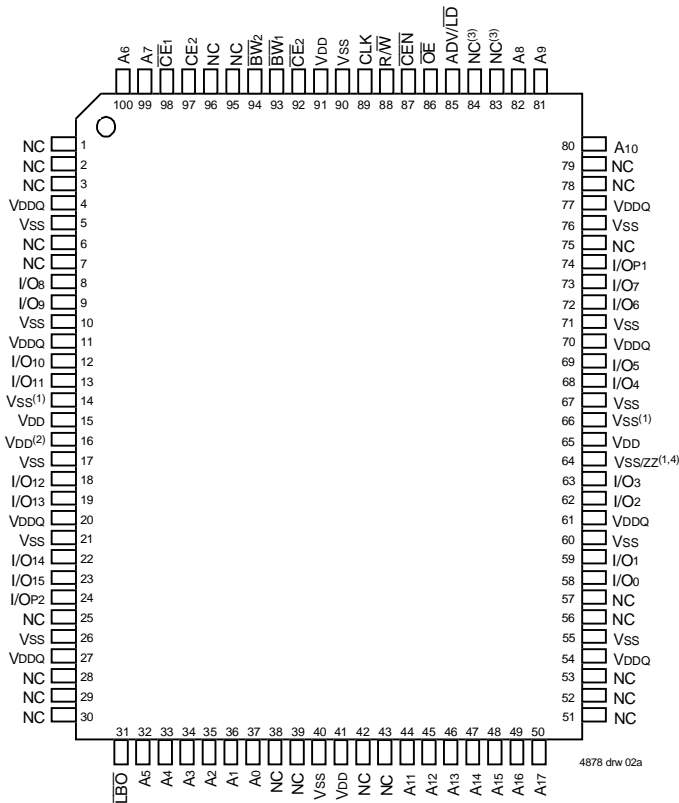


Top View 100 TQFP

NOTES:

1. Pins 14, 64, and 66 do not have to be connected directly to V_{SS} as long as the input voltage is $\leq V_{IL}$.
2. Pin 16 does not have to be connected directly to V_{DD} as long as the input voltage is $\geq V_{IH}$.
3. Pins 83 and 84 are reserved for future 8M and 16M respectively.
4. Pin 64 supports ZZ (sleep mode) on the latest die revision.

Pin Configuration — 256K x 18



Top View 100 TQFP

NOTES:

1. Pins 14, 64, and 66 do not have to be connected directly to VSS as long as the input voltage is $\leq V_{IL}$.
2. Pin 16 does not have to be connected directly to VDD as long as the input voltage is $\geq V_{IH}$.
3. Pins 83 and 84 are reserved for future 8M and 16M respectively.
4. Pin 64 supports ZZ (sleep mode) on the latest die revision.

100 TQFP Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	5	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 3dV	7	pF

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165 fBGA Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	TBD	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 3dV	TBD	pF

4878 tbl 07b

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial Value	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V _{TERM} ^(3,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DD}	V
V _{TERM} ^(4,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DD} + 0.5	V
V _{TERM} ^(5,6)	Terminal Voltage with Respect to GND	-0.5 to V _{DDQ} + 0.5	V
T _A ⁽⁷⁾	Commercial Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	2.0	W
I _{OUT}	DC Output Current	50	mA

4878 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

119 BGA Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	7	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 3dV	7	pF

4878 tbl 07a

Pin Configuration — 128K x 36, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC(3)	A8	A16	VDDQ
B	NC	CE2	A3	ADV/LD	A9	CE2	NC
C	NC	A7	A2	VDD	A12	A15	NC
D	I/O16	I/OP3	VSS	NC	VSS	I/OP2	I/O15
E	I/O17	I/O18	VSS	CE1	VSS	I/O13	I/O14
F	VDDQ	I/O19	VSS	OE	VSS	I/O12	VDDQ
G	I/O20	I/O21	BW3	NC(3)	BW2	I/O11	I/O10
H	I/O22	I/O23	VSS	R/W	VSS	I/O9	I/O8
J	VDDQ	VDD	VDD(2)	VDD	VSS(1)	VDD	VDDQ
K	I/O24	I/O26	VSS	CLK	VSS	I/O6	I/O7
L	I/O25	I/O27	BW4	NC	BW1	I/O4	I/O5
M	VDDQ	I/O28	VSS	CEN	VSS	I/O3	VDDQ
N	I/O29	I/O30	VSS	A1	VSS	I/O2	I/O1
P	I/O31	I/OP4	VSS	A0	VSS	I/OP1	I/O0
R	NC	A5	LBO	VDD	VSS(1)	A13	NC
T	NC	NC	A10	A11	A14	NC	NC/ZZ(6)
U	VDDQ	NC/TMS(4)	NC/TDI(4)	NC/TCK(4)	NC/TDO(4)	NC/TRST(4,5)	VDDQ

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Top View

Pin Configuration — 256K x 18, 119 BGA

	1	2	3	4	5	6	7
A	VDDQ	A6	A4	NC(3)	A8	A16	VDDQ
B	NC	CE2	A3	ADV/LD	A9	CE2	NC
C	NC	A7	A2	VDD	A13	A17	NC
D	I/O8	NC	VSS	NC	VSS	I/OP1	NC
E	NC	I/O9	VSS	CE1	VSS	NC	I/O7
F	VDDQ	NC	VSS	OE	VSS	I/O6	VDDQ
G	NC	I/O10	BW2	NC(3)	VSS	NC	I/O5
H	I/O11	NC	VSS	R/W	VSS	I/O4	NC
J	VDDQ	VDD	VDD(2)	VDD	VSS(1)	VDD	VDDQ
K	NC	I/O12	VSS	CLK	VSS	NC	I/O3
L	I/O13	NC	VSS	NC	BW1	I/O2	NC
M	VDDQ	I/O14	VSS	CEN	VSS	NC	VDDQ
N	I/O15	NC	VSS	A1	VSS	I/O1	NC
P	NC	I/OP2	VSS	A0	VSS	NC	I/O0
R	NC	A5	LBO	VDD	VSS(1)	A12	NC
T	NC	A10	A15	NC	A14	A11	NC/ZZ(6)
U	VDDQ	NC/TMS(4)	NC/TDI(4)	NC/TCK(4)	NC/TDO(4)	NC/TRST(4,5)	VDDQ

4878 drw 13B

Top View

NOTES:

1. R5 and J5 do not have to be directly connected to VSS as long as the input voltage is $\leq V_{IL}$.
2. J3 does not have to be directly connected to VDD as long as the input voltage is $\geq V_{IH}$.
3. G4 and A4 are reserved for future 8M and 16M respectively.
4. These pins are NC for the "S" version or the JTAG signal listed for the "SA" version.
5. TRST is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.
6. Pin T7 supports ZZ (sleep mode) on the latest die revision.

Pin Configuration — 128K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽³⁾	A7	\overline{CE}_1	\overline{BW}_3	\overline{BW}_2	\overline{CE}_2	\overline{CEN}	ADV/LD	NC ⁽³⁾	A8	NC
B	NC	A6	CE2	\overline{BW}_4	\overline{BW}_1	CLK	R/W	\overline{OE}	NC ⁽³⁾	A9	NC ⁽³⁾
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VSS ⁽¹⁾	VDD ⁽²⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	NC/ZZ ⁽⁶⁾
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	NC/TRST ^(4,5)	NC	VSS ⁽¹⁾	VSS	VDDQ	NC	I/OP1
P	NC	NC ⁽³⁾	A5	A2	NC/TDI ⁽⁴⁾	A1	NC/TDO ⁽⁴⁾	A10	A13	A14	NC
R	\overline{LBO}	NC ⁽³⁾	A4	A3	NC/TMS ⁽⁴⁾	A0	NC/TCK ⁽⁴⁾	A11	A12	A15	A16

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Pin Configuration - 256K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC ⁽³⁾	A7	\overline{CE}_1	\overline{BW}_2	NC	\overline{CE}_2	\overline{CEN}	ADV/LD	NC ⁽³⁾	A8	A10
B	NC	A6	CE2	NC	\overline{BW}_1	CLK	R/W	\overline{OE}	NC ⁽³⁾	A9	NC ⁽³⁾
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VSS ⁽¹⁾	VDD ⁽²⁾	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	NC/ZZ ⁽⁶⁾
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	NC/TRST ^(4,5)	NC	VSS ⁽¹⁾	VSS	VDDQ	NC	NC
P	NC	NC ⁽³⁾	A5	A2	NC/TDI ⁽⁴⁾	A1	NC/TDO ⁽⁴⁾	A11	A14	A15	NC
R	\overline{LBO}	NC ⁽³⁾	A4	A3	NC/TMS ⁽⁴⁾	A0	NC/TCK ⁽⁴⁾	A12	A13	A16	A17

4878 tbl 25a

NOTES:

- H1 and N7 do not have to be directly connected to VSS as long as the input voltage is $\leq V_{IL}$.
- H2 does not have to be directly connected directly to VDD as long as the input voltage is $\geq V_{IH}$.
- A9, B9, B11, A1, R2, and P2 are reserved for future 9M, 18M, 36M, 72M, 144M, and 288M respectively.
- These pins are NC for the "S" version or the JTAG signal listed for the "SA" version.
- TRST is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to VDD.
- Pin H11 supports ZZ (sleep mode) on the latest die revision.

Synchronous Truth Table (1)

\overline{CEN}	R/W	\overline{CE}_1 , $\overline{CE}_2^{(6)}$	ADV/LD	\overline{BW}_x	ADDRESS USED	PREVIOUS CYCLE	CURRENT CYCLE	I/O (One cycle later)
L	L	L	L	Valid	External	X	LOAD WRITE	D ⁽⁷⁾
L	H	L	L	X	External	X	LOAD READ	Q ⁽⁷⁾
L	X	X	H	Valid	Internal	LOAD WRITE / BURST WRITE	BURST WRITE (Advance burst counter) ⁽²⁾	D ⁽⁷⁾
L	X	X	H	X	Internal	LOAD READ / BURST READ	BURST READ (Advance burst counter) ⁽²⁾	Q ⁽⁷⁾
L	X	H	L	X	X	X	DESELECT or STOP ⁽³⁾	HIZ
L	X	X	H	X	X	DESELECT / NOOP	NOOP	HIZ
H	X	X	X	X	X	X	SUSPEND ⁽⁴⁾	Previous Value

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NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- When ADV/LD signal is sampled high, the internal burst counter is incremented. The R/W signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/W signal when the first address is loaded at the beginning of the burst cycle.
- Deselect cycle is initiated when either (\overline{CE}_1 , or \overline{CE}_2 is sampled high or CE2 is sampled low) and ADV/LD is sampled low at rising edge of clock. The data bus will tri-state one cycle after deselect is initiated.
- When \overline{CEN} is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
- To select the chip requires $\overline{CE}_1 = L$, $\overline{CE}_2 = L$ and CE2 = H on these chip enable pins. The chip is deselected if any one of the chip enables is false.
- Device Outputs are ensured to be in High-Z during device power-up.
- Q - data read from the device, D - data written to the device.

Partial Truth Table for Writes (1)

OPERATION	R/W	\overline{BW}_1	\overline{BW}_2	$\overline{BW}_3^{(9)}$	$\overline{BW}_4^{(9)}$
READ	H	X	X	X	X
WRITE ALL BYTES	L	L	L	L	L
WRITE BYTE 1 (I/O[0:7], I/Op1) ⁽²⁾	L	L	H	H	H
WRITE BYTE 2 (I/O[8:15], I/Op2) ⁽²⁾	L	H	L	H	H
WRITE BYTE 3 (I/O[16:23], I/Op3) ^(2,3)	L	H	H	L	H
WRITE BYTE 4 (I/O[24:31], I/Op4) ^(2,3)	L	H	H	H	L
NO WRITE	L	H	H	H	H

4878 tbl 09

NOTES:

- L = V_{IL}, H = V_{IH}, X = Don't Care.
- Multiple bytes may be selected during the same cycle.
- N/A for x18 configuration.

Interleaved Burst Sequence Table ($\overline{LBO} = V_{DD}$)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	1	0	0	1	0	0

4878 tbl 10

NOTE:

- Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Linear Burst Sequence Table ($\overline{LBO}=V_{SS}$)

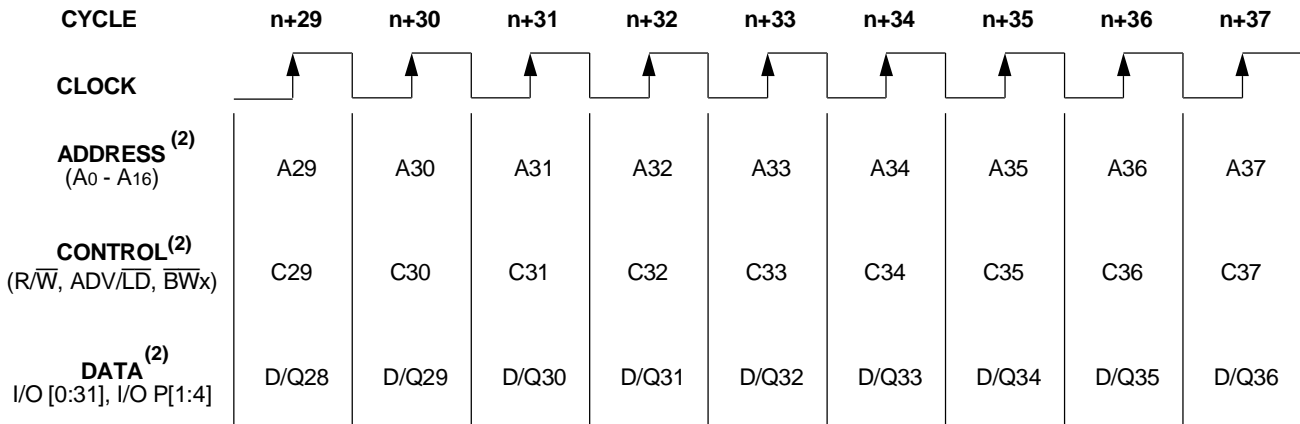
	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address ⁽¹⁾	1	1	0	0	0	1	1	0

4878 tbl 11

NOTE:

1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

Functional Timing Diagram (1)



4878 drw 03

NOTES:

1. This assumes \overline{CEN} , $\overline{CE1}$, $CE2$ and $\overline{CE2}$ are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.

Device Operation - Showing Mixed Load, Burst, Deselection NOOP Cycles⁽²⁾

Cycle	Address	R/ \bar{W}	ADV/ \bar{LD}	$\bar{CE}_1^{(1)}$	\bar{CEN}	\bar{BW}_x	\bar{OE}	I/O	Comments
n	A0	H	L	L	L	X	X	D1	Load read
n+1	X	X	H	X	L	X	L	Q0	Burst read
n+2	A1	H	L	L	L	X	L	Q0+1	Load read
n+3	X	X	L	H	L	X	L	Q1	Deselect or STOP
n+4	X	X	H	X	L	X	X	Z	NOOP
n+5	A2	H	L	L	L	X	X	Z	Load read
n+6	X	X	H	X	L	X	L	Q2	Burst read
n+7	X	X	L	H	L	X	L	Q2+1	Deselect or STOP
n+8	A3	L	L	L	L	L	X	Z	Load write
n+9	X	X	H	X	L	L	X	D3	Burst write
n+10	A4	L	L	L	L	L	X	D3+1	Load write
n+11	X	X	L	H	L	X	X	D4	Deselect or STOP
n+12	X	X	H	X	L	X	X	Z	NOOP
n+13	A5	L	L	L	L	L	X	Z	Load write
n+14	A6	H	L	L	L	X	X	D5	Load read
n+15	A7	L	L	L	L	L	L	Q6	Load write
n+16	X	X	H	X	L	L	X	D7	Burst write
n+17	A8	H	L	L	L	X	X	D7+1	Load read
n+18	X	X	H	X	L	X	L	Q8	Burst read
n+19	A9	L	L	L	L	L	L	Q8+1	Load write

4878 tbl 12

NOTES:

- \bar{CE}_2 timing transition is identical to \bar{CE}_1 signal. \bar{CE}_2 timing transition is identical but inverted to the \bar{CE}_1 and \bar{CE}_2 signals.
- H = High; L = Low; X = Don't Care; Z = High Impedence.

Read Operation (1)

Cycle	Address	R \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}_1^{(2)}$	$\bar{C}\bar{E}\bar{N}$	$\bar{B}\bar{W}x$	$\bar{O}\bar{E}$	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	X	X	X	X	L	Q ₀	Contents of Address A ₀ Read Out

4878 tbl 13

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{C}\bar{E}_2$ timing transition is identical to $\bar{C}\bar{E}_1$ signal. $\bar{C}\bar{E}_2$ timing transition is identical but inverted to the $\bar{C}\bar{E}_1$ and $\bar{C}\bar{E}_2$ signals.

Burst Read Operation (1)

Cycle	Address	R \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}_1^{(2)}$	$\bar{C}\bar{E}\bar{N}$	$\bar{B}\bar{W}x$	$\bar{O}\bar{E}$	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address and Control meet setup
n+1	X	X	H	X	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+2	X	X	H	X	L	X	L	Q ₀₊₁	Address A ₀₊₁ Read Out, Inc. Count
n+3	X	X	H	X	L	X	L	Q ₀₊₂	Address A ₀₊₂ Read Out, Inc. Count
n+4	X	X	H	X	L	X	L	Q ₀₊₃	Address A ₀₊₃ Read Out, Load A ₁
n+5	A ₁	H	L	L	L	X	L	Q ₀	Address A ₀ Read Out, Inc. Count
n+6	X	X	H	X	L	X	L	Q ₁	Address A ₁ Read Out, Inc. Count
n+7	A ₂	H	L	L	L	X	L	Q ₁₊₁	Address A ₁₊₁ Read Out, Load A ₂

4878 tbl 14

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{C}\bar{E}_2$ timing transition is identical to $\bar{C}\bar{E}_1$ signal. $\bar{C}\bar{E}_2$ timing transition is identical but inverted to the $\bar{C}\bar{E}_1$ and $\bar{C}\bar{E}_2$ signals.

Write Operation (1)

Cycle	Address	R \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}_1^{(2)}$	$\bar{C}\bar{E}\bar{N}$	$\bar{B}\bar{W}x$	$\bar{O}\bar{E}$	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	X	X	D ₀	Write to Address A ₀

4878 tbl 15

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{C}\bar{E}_2$ timing transition is identical to $\bar{C}\bar{E}_1$ signal. $\bar{C}\bar{E}_2$ timing transition is identical but inverted to the $\bar{C}\bar{E}_1$ and $\bar{C}\bar{E}_2$ signals.

Burst Write Operation (1)

Cycle	Address	R \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}_1^{(2)}$	$\bar{C}\bar{E}\bar{N}$	$\bar{B}\bar{W}x$	$\bar{O}\bar{E}$	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address and Control meet setup
n+1	X	X	H	X	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+2	X	X	H	X	L	L	X	D ₀₊₁	Address A ₀₊₁ Write, Inc. Count
n+3	X	X	H	X	L	L	X	D ₀₊₂	Address A ₀₊₂ Write, Inc. Count
n+4	X	X	H	X	L	L	X	D ₀₊₃	Address A ₀₊₃ Write, Load A ₁
n+5	A ₁	L	L	L	L	L	X	D ₀	Address A ₀ Write, Inc. Count
n+6	X	X	H	X	L	L	X	D ₁	Address A ₁ Write, Inc. Count
n+7	A ₂	L	L	L	L	L	X	D ₁₊₁	Address A ₁₊₁ Write, Load A ₂

4878 tbl 16

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. $\bar{C}\bar{E}_2$ timing transition is identical to $\bar{C}\bar{E}_1$ signal. $\bar{C}\bar{E}_2$ timing transition is identical but inverted to the $\bar{C}\bar{E}_1$ and $\bar{C}\bar{E}_2$ signals.

Read Operation with Clock Enable Used ⁽¹⁾

Cycle	Address	R/W	ADV/LD	$\overline{CE}_1^{(2)}$	\overline{CEN}	BWx	\overline{OE}	I/O	Comments
n	A ₀	H	L	L	L	X	X	X	Address A ₀ and Control meet setup
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored
n+2	A ₁	H	L	L	L	X	L	Q ₀	Address A ₀ Read out, Load A ₁
n+3	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+4	X	X	X	X	H	X	L	Q ₀	Clock Ignored. Data Q ₀ is on the bus.
n+5	A ₂	H	L	L	L	X	L	Q ₁	Address A ₁ Read out, Load A ₂
n+6	A ₃	H	L	L	L	X	L	Q ₂	Address A ₂ Read out, Load A ₃
n+7	A ₄	H	L	L	L	X	L	Q ₃	Address A ₃ Read out, Load A ₄

4878 tbl 17

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Write Operation with Clock Enable Used ⁽¹⁾

Cycle	Address	R/W	ADV/LD	$\overline{CE}_1^{(2)}$	\overline{CEN}	BWx	\overline{OE}	I/O	Comments
n	A ₀	L	L	L	L	L	X	X	Address A ₀ and Control meet setup.
n+1	X	X	X	X	H	X	X	X	Clock n+1 Ignored.
n+2	A ₁	L	L	L	L	L	X	D ₀	Write data D ₀ , Load A ₁ .
n+3	X	X	X	X	H	X	X	X	Clock Ignored.
n+4	X	X	X	X	H	X	X	X	Clock Ignored.
n+5	A ₂	L	L	L	L	L	X	D ₁	Write Data D ₁ , Load A ₂
n+6	A ₃	L	L	L	L	L	X	D ₂	Write Data D ₂ , Load A ₃
n+7	A ₄	L	L	L	L	L	X	D ₃	Write Data D ₃ , Load A ₄

4878 tbl 18

NOTES:

1. H = High; L = Low; X = Don't Care; Z = High Impedance.
2. \overline{CE}_2 timing transition is identical to \overline{CE}_1 signal. \overline{CE}_2 timing transition is identical but inverted to the \overline{CE}_1 and \overline{CE}_2 signals.

Read Operation With Chip Enable Used (1)

Cycle	Address	R \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}_1^{(2)}$	$\bar{C}\bar{E}N$	B $\bar{W}x$	$\bar{O}\bar{E}$	I/O ⁽³⁾	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A ₀	H	L	L	L	X	X	Z	Address A ₀ and Control meet setup.
n+3	X	X	L	H	L	X	L	Q ₀	Address A ₀ read out, Deselected.
n+4	A ₁	H	L	L	L	X	X	Z	Address A ₁ and Control meet setup.
n+5	X	X	L	H	L	X	L	Q ₁	Address A ₁ read out, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A ₂	H	L	L	L	X	X	Z	Address A ₂ and Control meet setup.
n+8	X	X	L	H	L	X	L	Q ₂	Address A ₂ read out, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

4878 tbl 19

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\bar{C}\bar{E}_2$ timing transition is identical to $\bar{C}\bar{E}_1$ signal. CE₂ timing transition is identical but inverted to the $\bar{C}\bar{E}_1$ and $\bar{C}\bar{E}_2$ signals.
3. Device outputs are ensured to be in High-Z during device power-up.

Write Operation with Chip Enable Used (1)

Cycle	Address	R \bar{W}	ADV/ $\bar{L}\bar{D}$	$\bar{C}\bar{E}_1^{(2)}$	$\bar{C}\bar{E}N$	B $\bar{W}x$	$\bar{O}\bar{E}$	I/O ⁽³⁾	Comments
n	X	X	L	H	L	X	X	?	Deselected.
n+1	X	X	L	H	L	X	X	Z	Deselected.
n+2	A ₀	L	L	L	L	L	X	Z	Address A ₀ and Control meet setup
n+3	X	X	L	H	L	X	X	D ₀	Data D ₀ Write In, Deselected.
n+4	A ₁	L	L	L	L	L	X	Z	Address A ₁ and Control meet setup
n+5	X	X	L	H	L	X	X	D ₁	Data D ₁ Write In, Deselected.
n+6	X	X	L	H	L	X	X	Z	Deselected.
n+7	A ₂	L	L	L	L	L	X	Z	Address A ₂ and Control meet setup
n+8	X	X	L	H	L	X	X	D ₂	Data D ₂ Write In, Deselected.
n+9	X	X	L	H	L	X	X	Z	Deselected.

4878 tbl 20

NOTES:

1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance.
2. $\bar{C}\bar{E} = L$ is defined as $\bar{C}\bar{E}_1 = L$, $\bar{C}\bar{E}_2 = L$ and CE₂ = H. $\bar{C}\bar{E} = H$ is defined as $\bar{C}\bar{E}_1 = H$, $\bar{C}\bar{E}_2 = H$ or CE₂ = L.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _{LI}	Input Leakage Current	V _{DD} = Max., V _{IN} = 0V to V _{DD}	—	5	μA
I _{LI}	$\overline{\text{LBO}}$, JTAG and ZZ Input Leakage Current ⁽¹⁾	V _{DD} = Max., V _{IN} = 0V to V _{DD}	—	30	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC}	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = +6mA, V _{DD} = Min.	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -6mA, V _{DD} = Min.	2.0	—	V

4878 tbl 21

NOTE:

1. The $\overline{\text{LBO}}$, TMS, TDI, TCK and $\overline{\text{TRST}}$ pins will be internally pulled to V_{DD} and ZZ will be internally pulled to V_{SS} if it is not actively driven in the application.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ⁽¹⁾ (V_{DD} = 3.3V +/-5%)

Symbol	Parameter	Test Conditions	7.5ns	8ns		8.5ns		Unit
			Com'l Only	Com'l	Ind	Com'l	Ind	
I _{DD}	Operating Power Supply Current	Device Selected, Outputs Open, ADV/ $\overline{\text{LD}}$ = X, V _{DD} = Max., V _{IN} ≥ V _H or ≤ V _L , f = f _{MAX} ⁽²⁾	275	250	260	225	235	mA
ISB1	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V _{DD} = Max., V _{IN} ≥ V _{HD} or ≤ V _{LD} , f = 0 ^(2,3)	40	40	45	40	45	mA
ISB2	Clock Running Power Supply Current	Device Deselected, Outputs Open, V _{DD} = Max., V _{IN} ≥ V _{HD} or ≤ V _{LD} , f = f _{MAX} ^(2,3)	105	100	110	95	105	mA
ISB3	Idle Power Supply Current	Device Selected, Outputs Open, $\overline{\text{CEN}}$ ≥ V _H , V _{DD} = Max., V _{IN} ≥ V _{HD} or ≤ V _{LD} , f = f _{MAX} ^(2,3)	40	40	45	40	45	mA

4878 tbl 22

NOTES:

- All values are maximum guaranteed values.
- At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/tcyc; f=0 means no input lines are changing.
- For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Loads

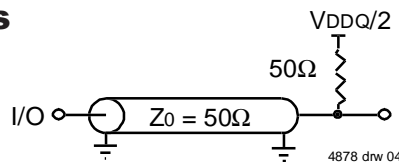


Figure 1. AC Test Load

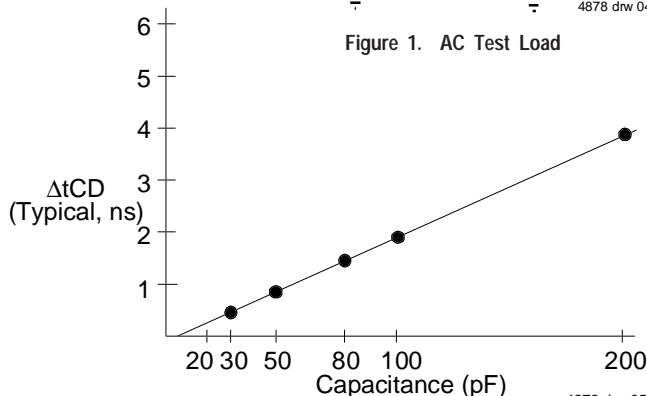


Figure 2. Lumped Capacitive Load, Typical Derating

AC Test Conditions (V_{DDQ} = 2.5V)

Input Pulse Levels	0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	(V _{DDQ} /2)
Output Reference Levels	(V _{DDQ} /2)
Output Load	Figure 1

4878 tbl 23

AC Electrical Characteristics (VDD = 3.3V +/-5%, Commercial and Industrial Temperature Ranges)

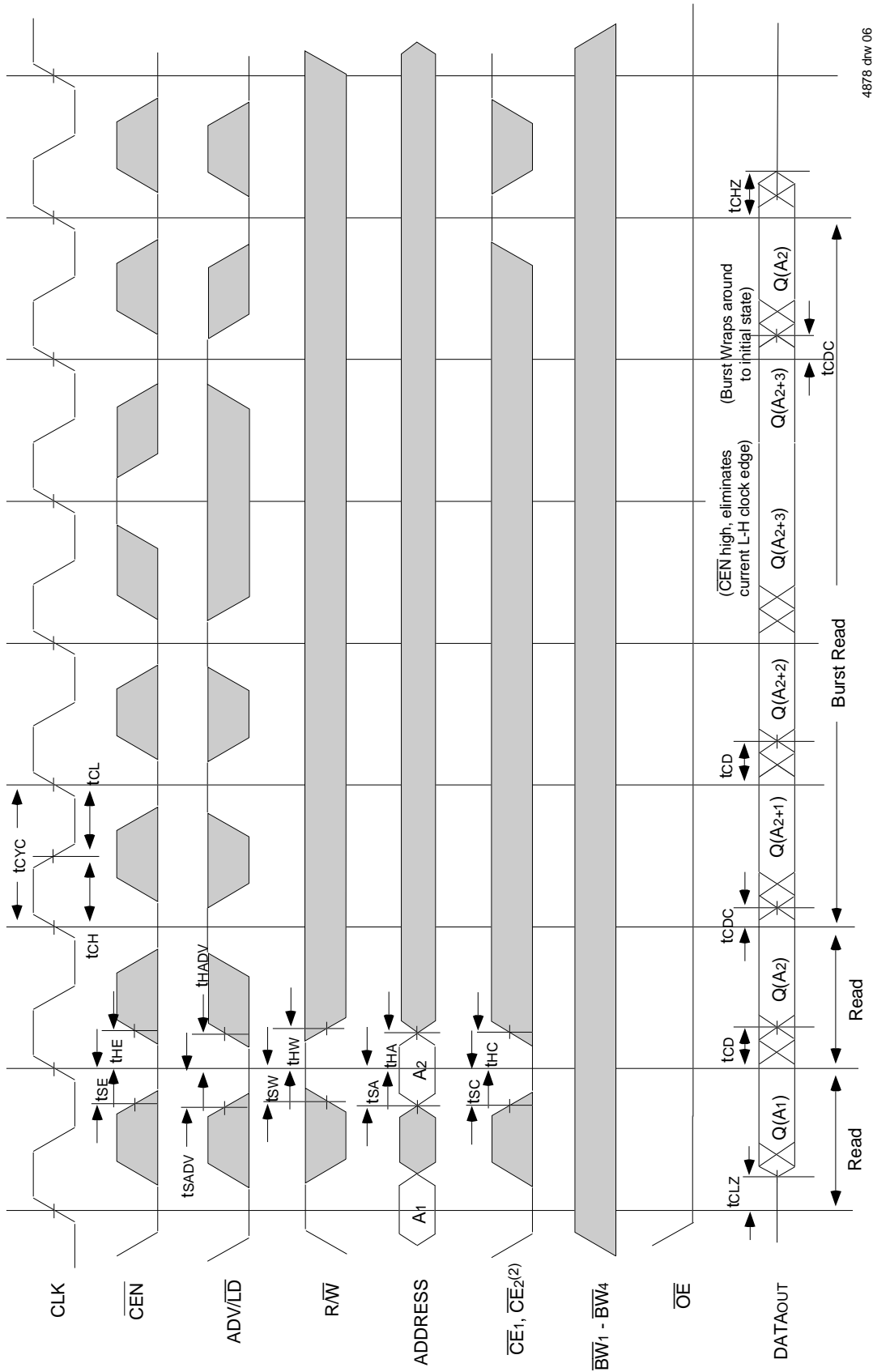
Symbol	Parameter	7.5ns ⁽⁵⁾		8ns		8.5ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	10	—	10.5	—	11	—	ns
t _{CH} ⁽¹⁾	Clock High Pulse Width	2.5	—	2.7	—	3.0	—	ns
t _{CL} ⁽¹⁾	Clock Low Pulse Width	2.5	—	2.7	—	3.0	—	ns
Output Parameters								
t _{CD}	Clock High to Valid Data	—	7.5	—	8	—	8.5	ns
t _{CDc}	Clock High to Data Change	2	—	2	—	2	—	ns
t _{CLZ} ^(2,3,4)	Clock High to Output Active	3	—	3	—	3	—	ns
t _{CHZ} ^(2,3,4)	Clock High to Data High-Z	—	5	—	5	—	5	ns
t _{OE}	Output Enable Access Time	—	5	—	5	—	5	ns
t _{OLZ} ^(2,3)	Output Enable Low to Data Active	0	—	0	—	0	—	ns
t _{OHZ} ^(2,3)	Output Enable High to Data High-Z	—	5	—	5	—	5	ns
Set Up Times								
t _{SE}	Clock Enable Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SA}	Address Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SD}	Data In Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SW}	Read/Write ($\overline{R\overline{W}}$) Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{ADV}	Advance/Load ($\overline{ADV/\overline{LD}}$) Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SC}	Chip Enable/Select Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{SB}	Byte Write Enable ($\overline{B\overline{Wx}}$) Setup Time	2.0	—	2.0	—	2.0	—	ns
Hold Times								
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HW}	Read/Write ($\overline{R\overline{W}}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HADV}	Advance/Load ($\overline{ADV/\overline{LD}}$) Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HC}	Chip Enable/Select Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HB}	Byte Write Enable ($\overline{B\overline{Wx}}$) Hold Time	0.5	—	0.5	—	0.5	—	ns

NOTES:

4878 tbl 24

1. Measured as HIGH above 0.6V_{DD0} and LOW below 0.4V_{DD0}.
2. Transition is measured ±200mV from steady-state.
3. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
4. To avoid bus contention, the output buffers are designed such that t_{CHZ} (device turn-off) is about 1ns faster than t_{CLZ} (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because t_{CLZ} is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 3.465V) than t_{CHZ}, which is a Max. parameter (worse case at 70 deg. C, 3.135V).
5. Commercial temperature range only.

Timing Waveform of Read Cycle (1,2,3,4)

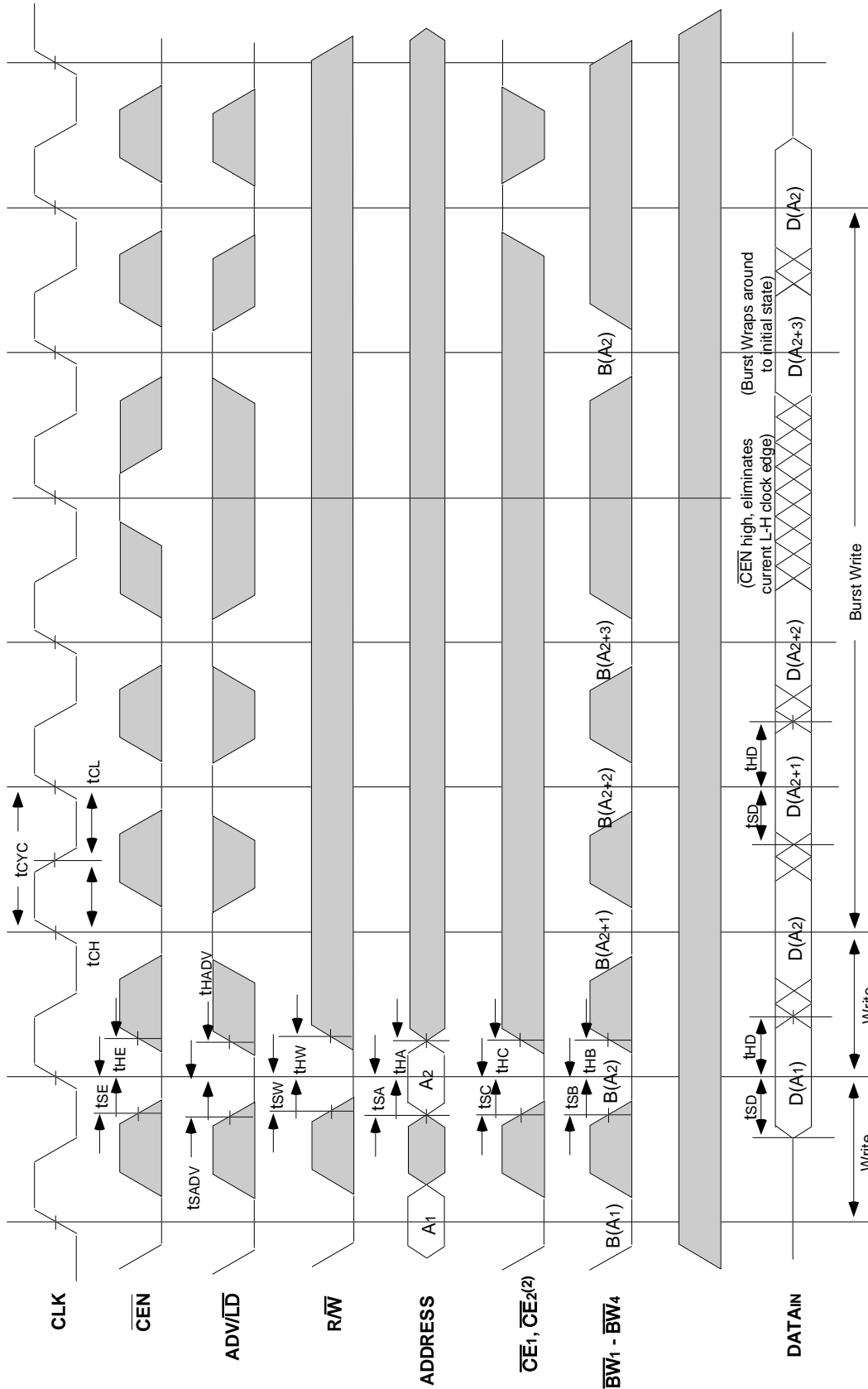


4878 drw 06

NOTES:

1. Q(A1) represents the first output from the external address A1. Q(A2) represents the first output from the external address A2; Q(A2+1) represents the next output data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CEz timing transitions are identical but inverted to CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE1 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. RW is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the RW signal when new address and control are loaded into the SRAM.

Timing Waveform of Write Cycles (1,2,3,4,5)

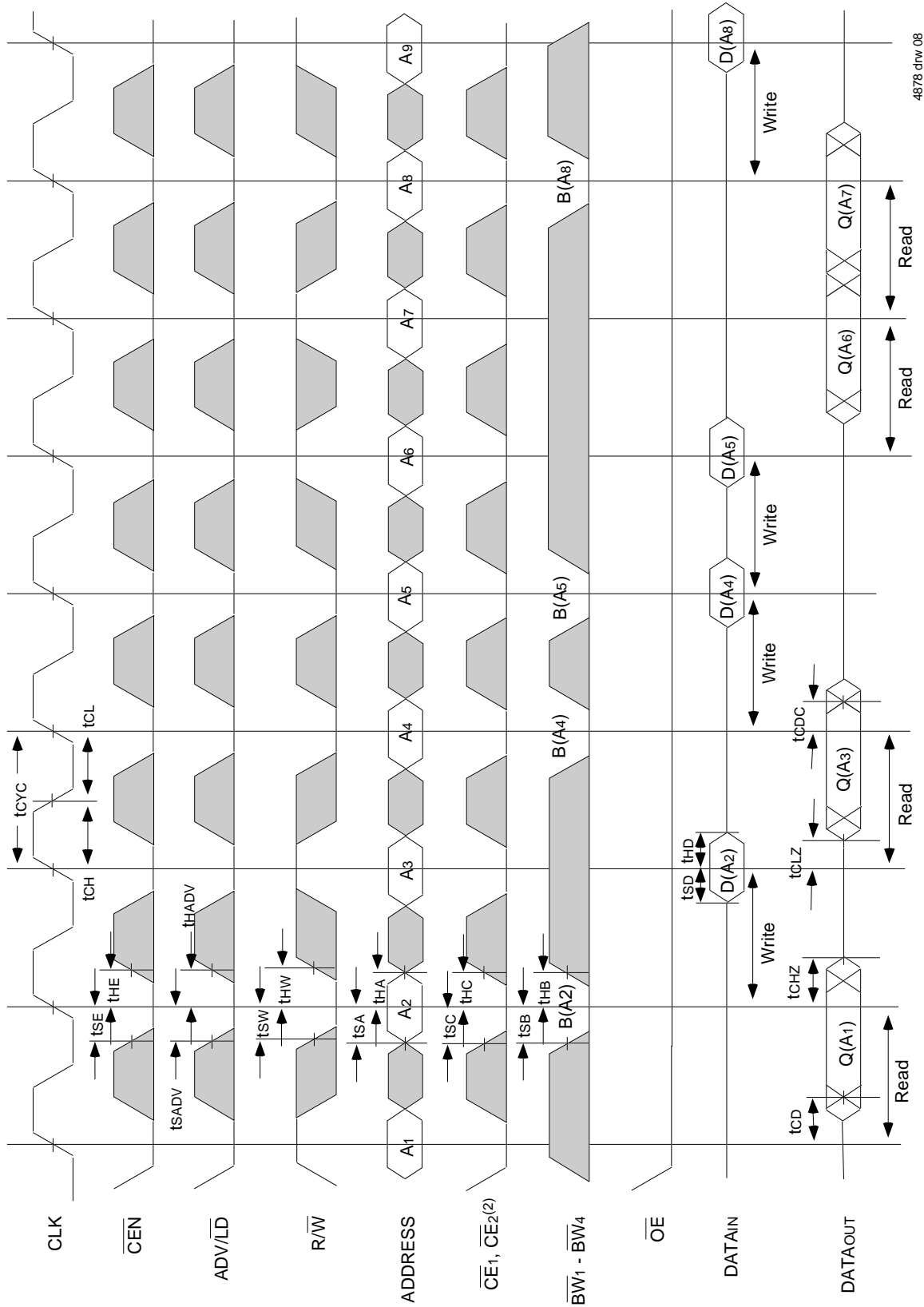


4878 drw 07

NOTES:

1. D(A1) represents the first input to the external address A1. D(A2) represents the first input to the external address A2; D(A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/LD LOW.
4. RW is don't care when the SRAM is bursting (ADV/LD sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the RW signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when RW signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of Combined Read and Write Cycles (1,2,3)

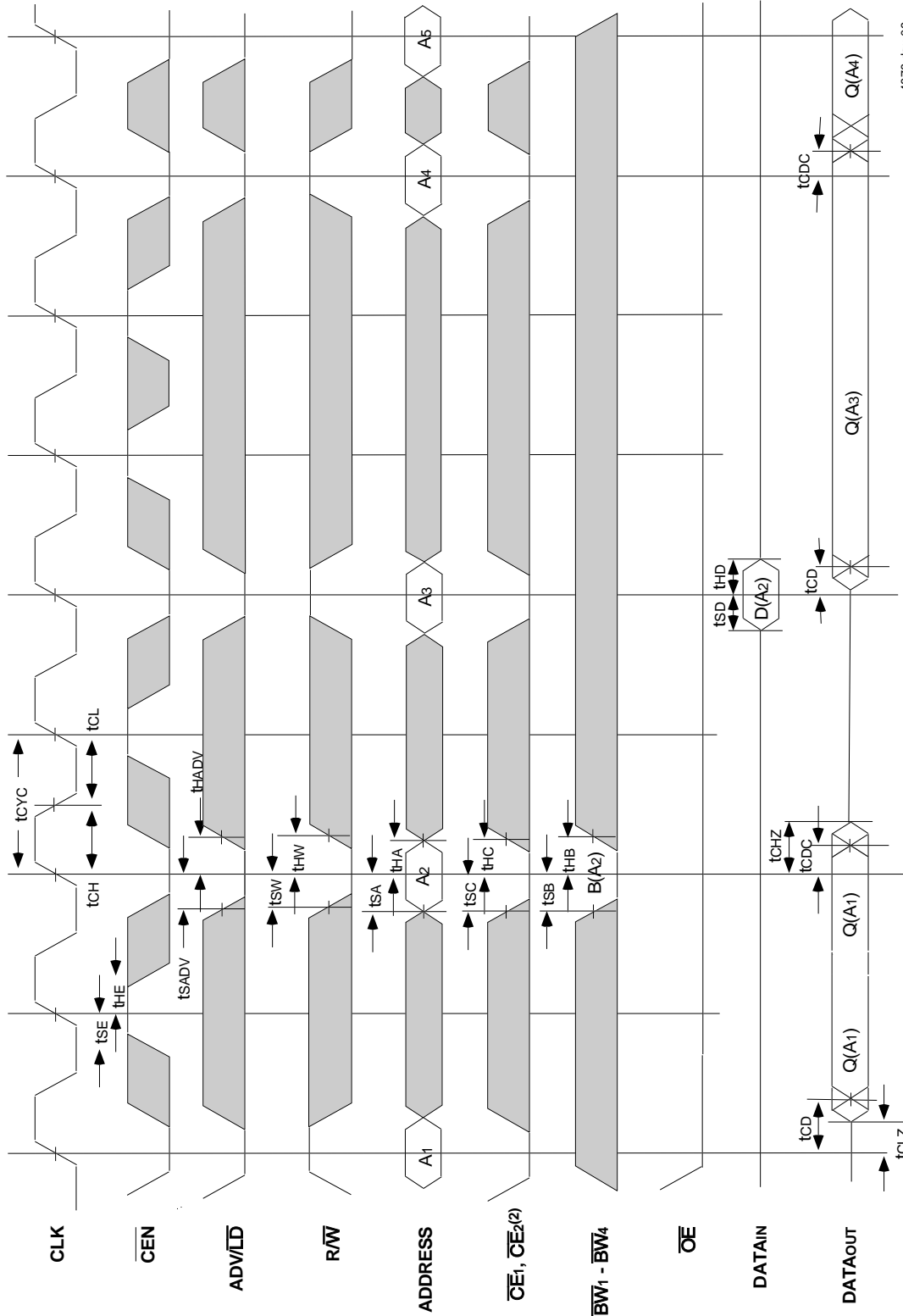


4878 clw 08

NOTES:

1. Q(A1) represents the first output from the external address A1. D(A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when RW signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of $\overline{\text{CEN}}$ Operation (1,2,3,4)

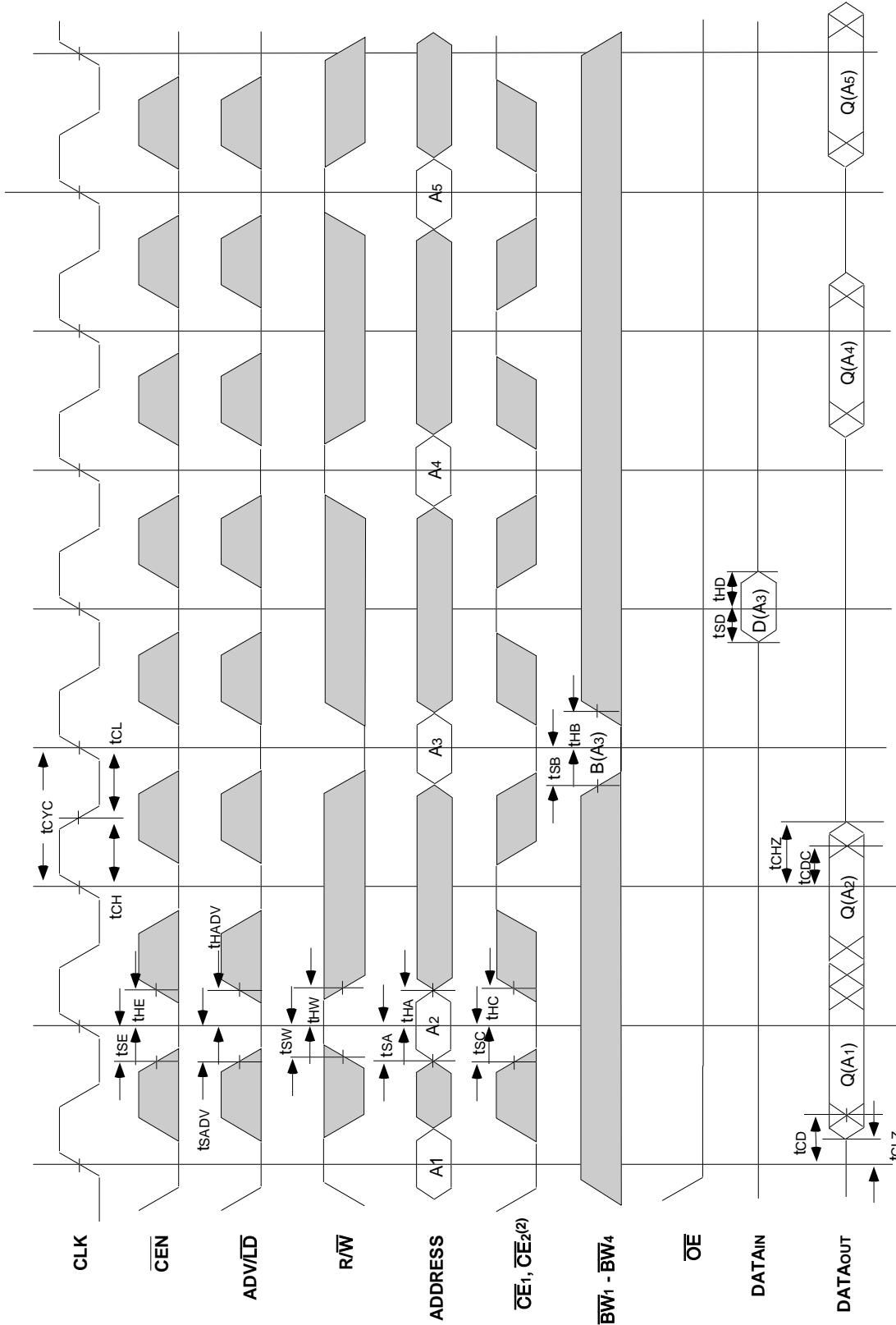


4878 drw 09

NOTES:

1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. $\overline{\text{CE2}}$ limiting transitions are identical but inverted to the $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ signals. For example, when $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are LOW on this waveform, $\overline{\text{CE2}}$ is HIGH.
3. $\overline{\text{CEN}}$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($\overline{\text{BWx}}$) must be valid on all write and burst-write cycles. A write cycle is initiated when $\overline{\text{R/W}}$ signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Timing Waveform of \overline{CS} Operation (1,2,3,4)

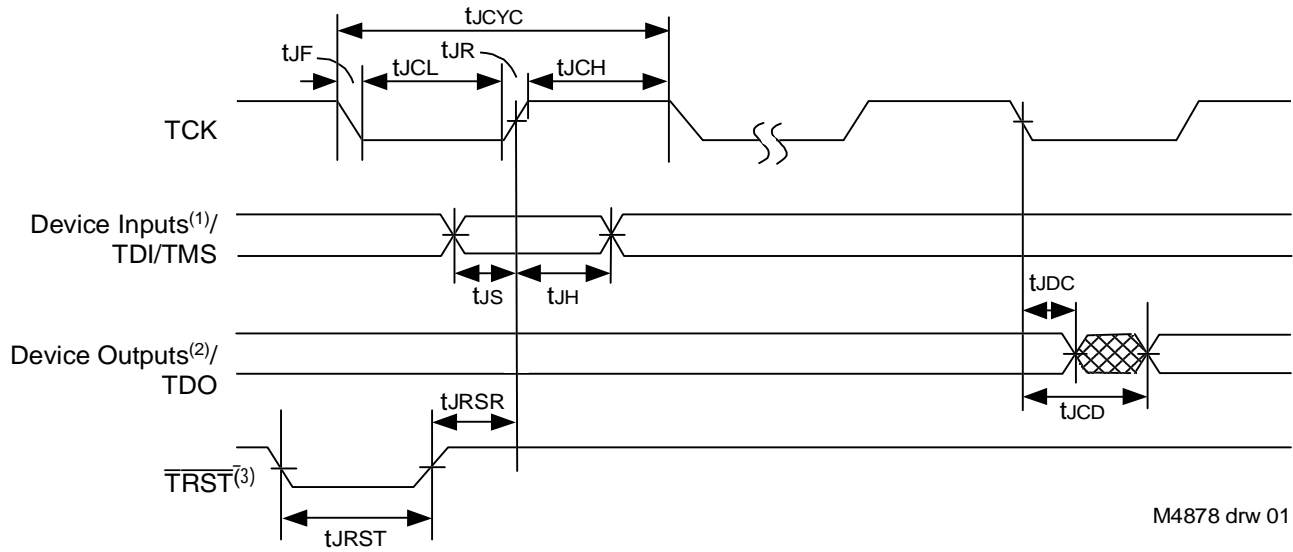


4878 drw 10

NOTES:

1. Q(A1) represents the first output from the external address A1. D(A3) represents the input data to the SRAM corresponding to address A3 etc.
2. CE2 timing transitions are identical but inverted to the $\overline{CE1}$ and $\overline{CE2}$ signals. For example, when $\overline{CE1}$ and $\overline{CE2}$ are LOW on this waveform, CE2 is HIGH.
3. When either one of the Chip enables ($\overline{CE1}$, CE2, $\overline{CE2}$) is sampled inactive at the rising clock edge, a deselect cycle is initiated. The data-bus tri-states one cycle after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.
4. Individual Byte Write signals (\overline{BWx}) must be valid on all write and burst-write cycles. A write cycle is initiated when \overline{RW} signal is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

JTAG Interface Specification (SA Version only)



NOTES:

1. Device inputs = All device inputs except TDI, TMS and \overline{TRST} .
2. Device outputs = All device outputs except TDO.
3. During power up, \overline{TRST} could be driven low or not be used since the JTAG circuit resets automatically. \overline{TRST} is an optional JTAG reset.

JTAG AC Electrical Characteristics^(1,2,3,4)

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	5 ⁽¹⁾	ns
t_{JF}	JTAG Clock Fall Time	—	5 ⁽¹⁾	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	20	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	25	—	ns
t_{JH}	JTAG Hold	25	—	ns

M4878 tbl 01

NOTES:

1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
JTAG Identification (JIDR)	32
Boundary Scan (BSR)	Note (1)

M4878 tbl 03

NOTE:

1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

JTAG Identification Register Definitions (SA Version only)

Instruction Field	Value	Description
Revision Number (31:28)	0x2	Reserved for version number.
IDT Device ID (27:12)	0x211, 0x213	Defines IDT part number 71V2557SA and 71V2559SA, respectively.
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT.
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register.

I4878 tbl 02

Available JTAG Instructions

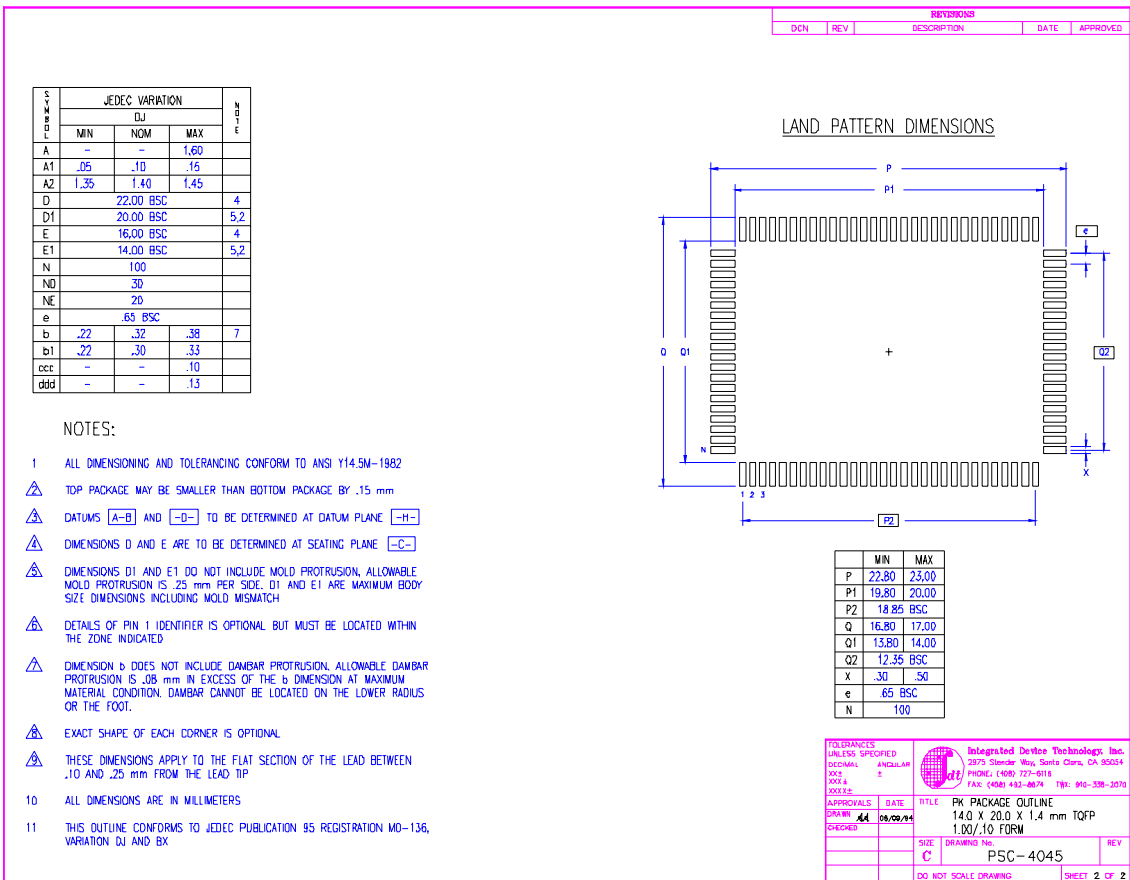
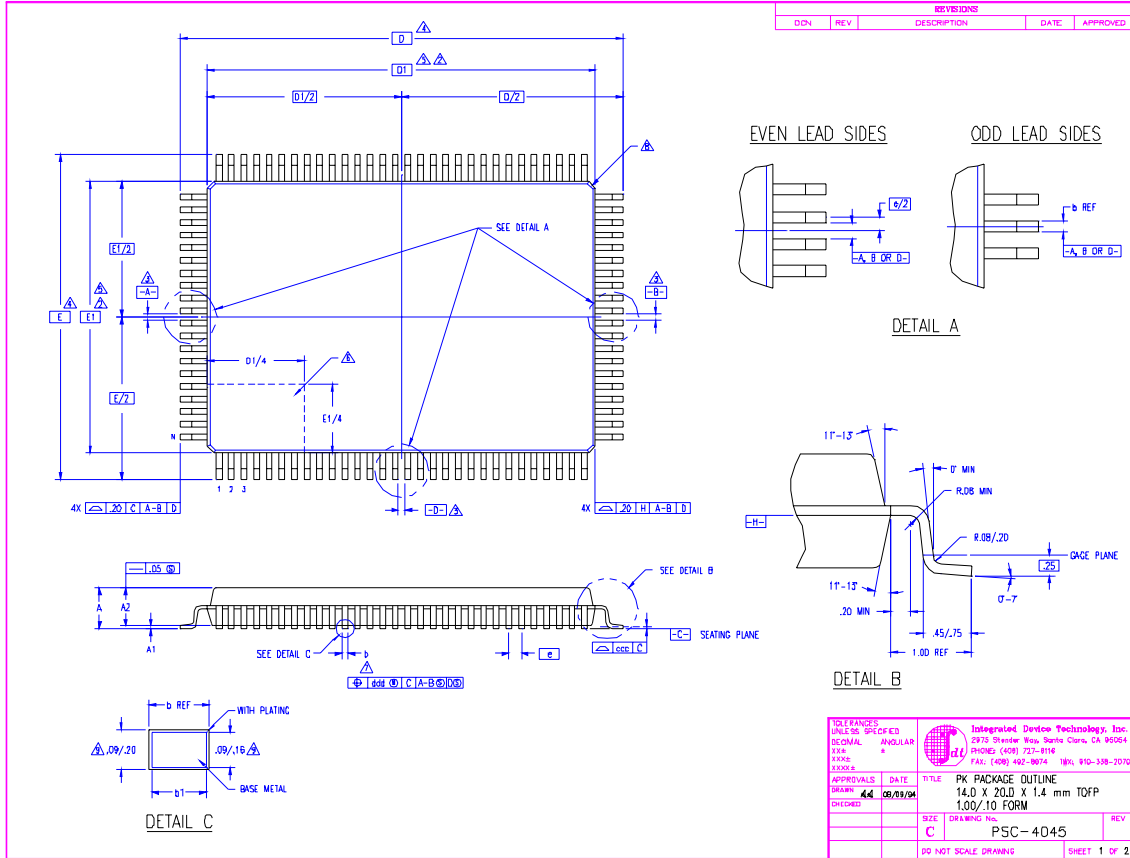
Instruction	Description	OPCODE
EXTEST	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.	0000
SAMPLE/PRELOAD	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ and outputs ⁽¹⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.	0001
DEVICE_ID	Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO.	0010
HIGHZ	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.	0011
RESERVED	Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions.	0100
RESERVED		0101
RESERVED		0110
RESERVED		0111
CLAMP	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.	1000
RESERVED	Same as above.	1001
RESERVED		1010
RESERVED		1011
RESERVED		1100
VALIDATE	Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification.	1101
RESERVED	Same as above.	1110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	1111

I4878 tbl 04

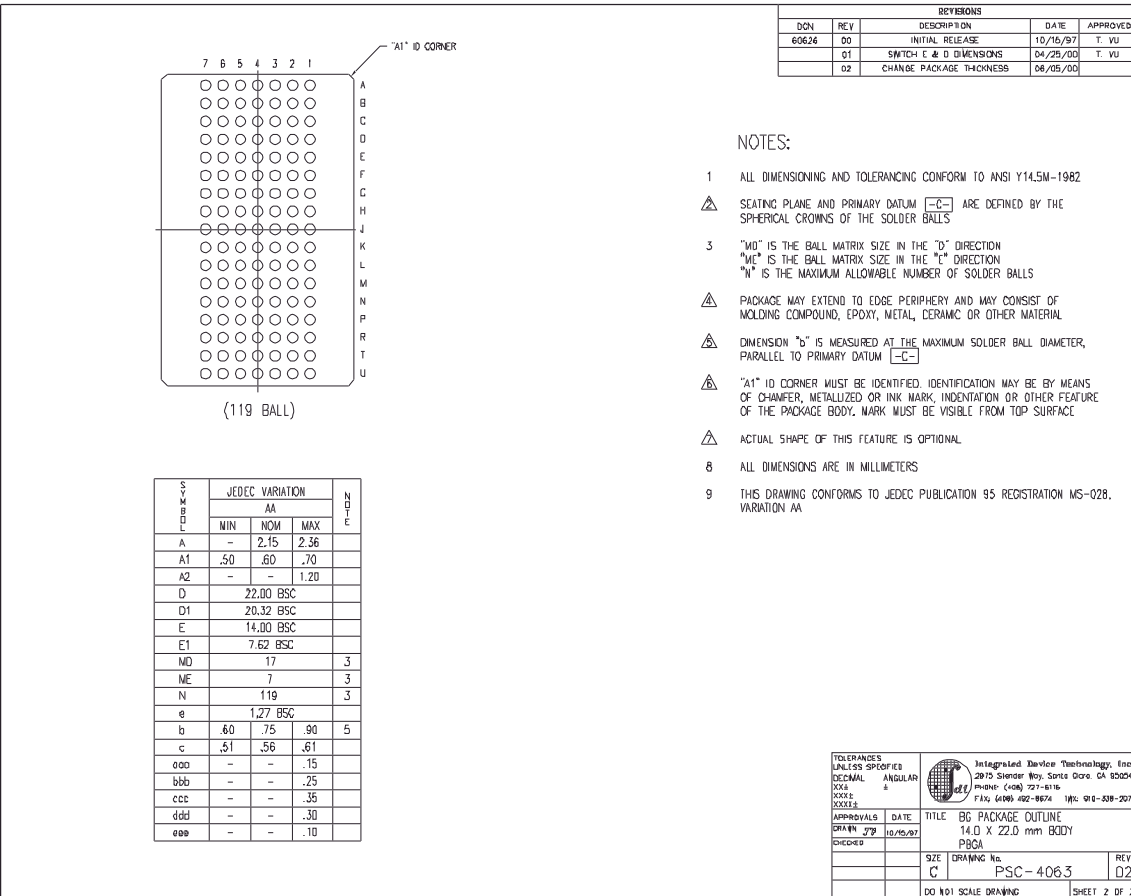
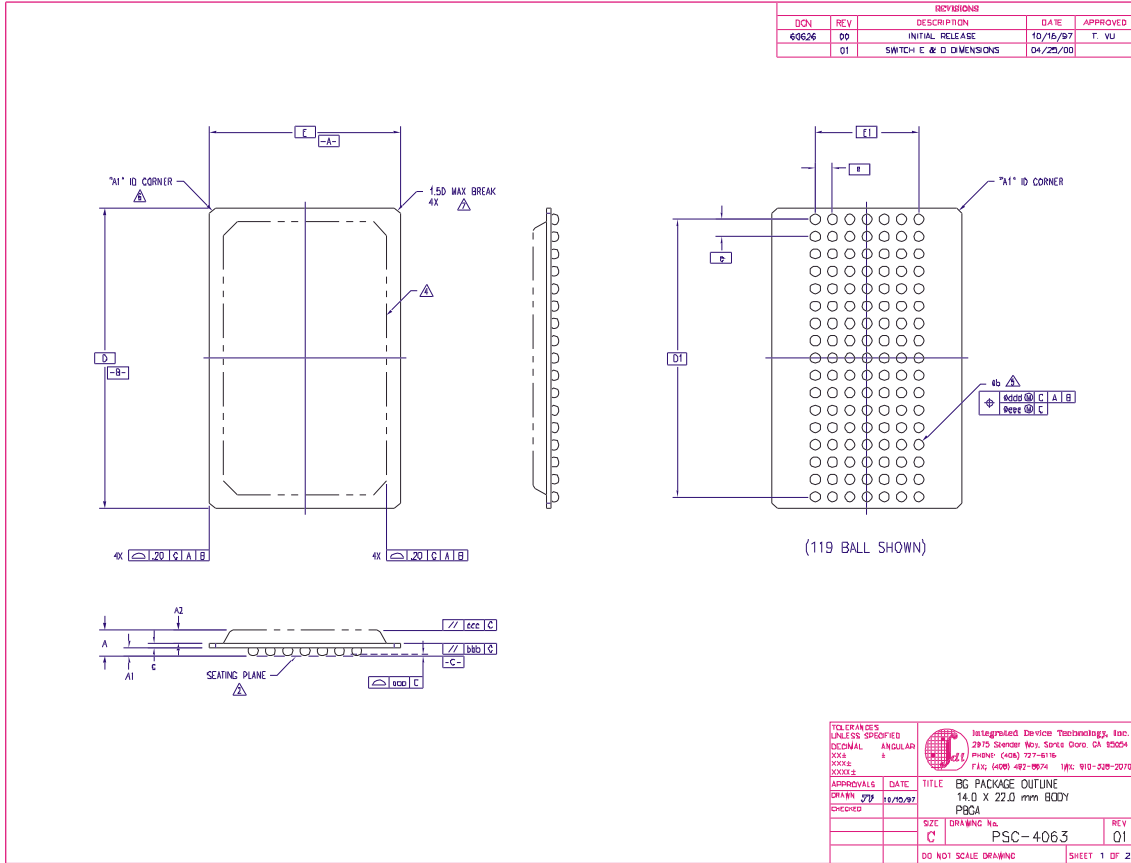
NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.

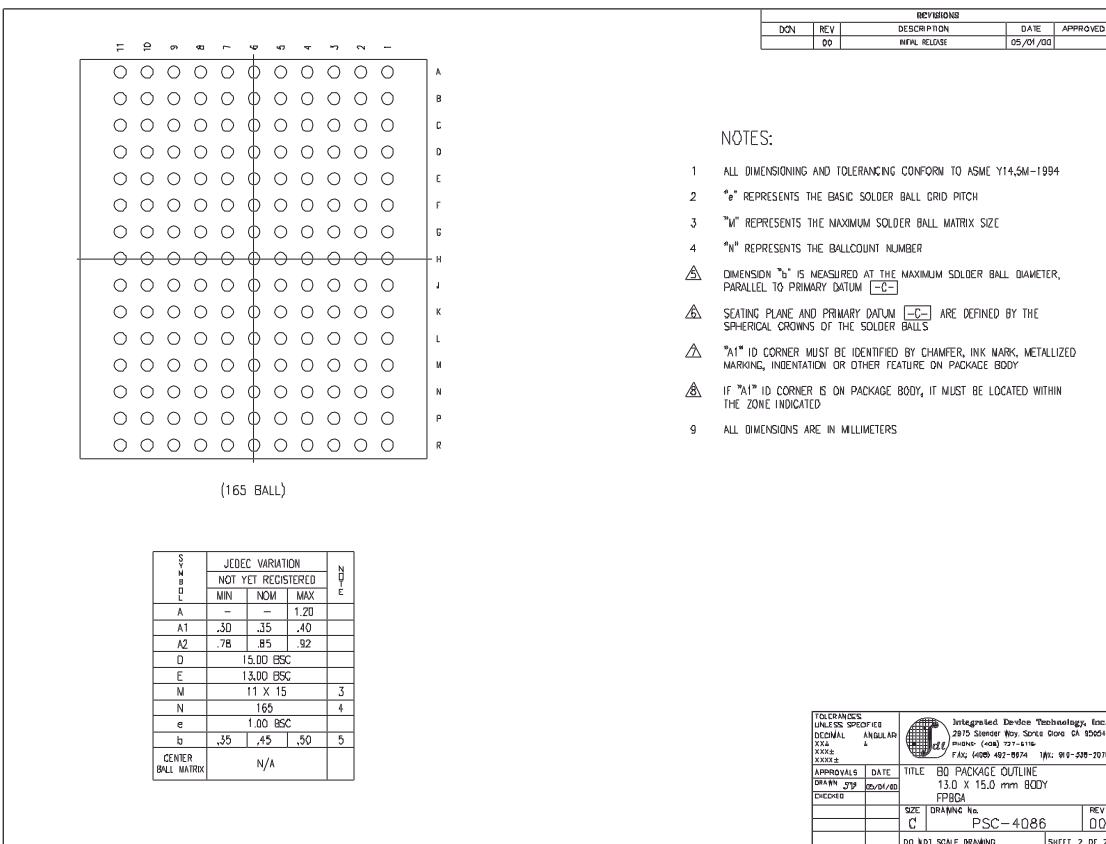
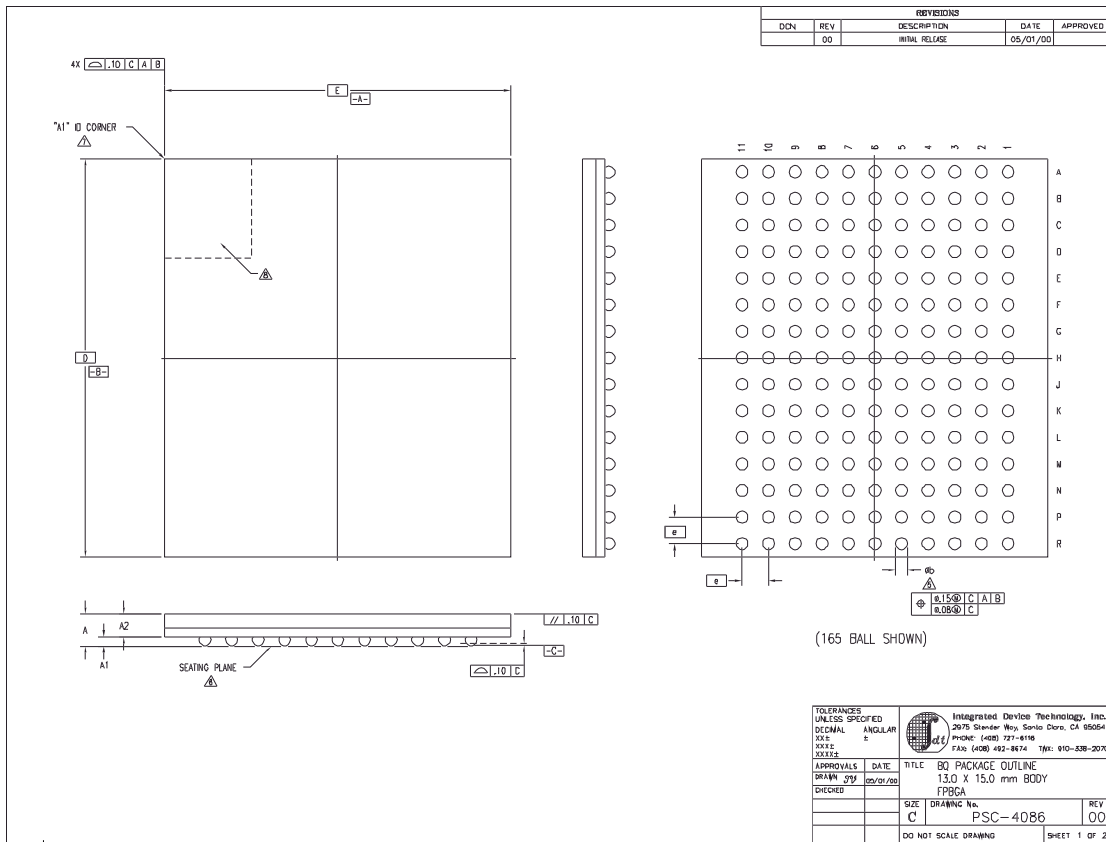
100-Pin Thin Quad Plastic Flatpack (TQFP) Package Diagram Outline



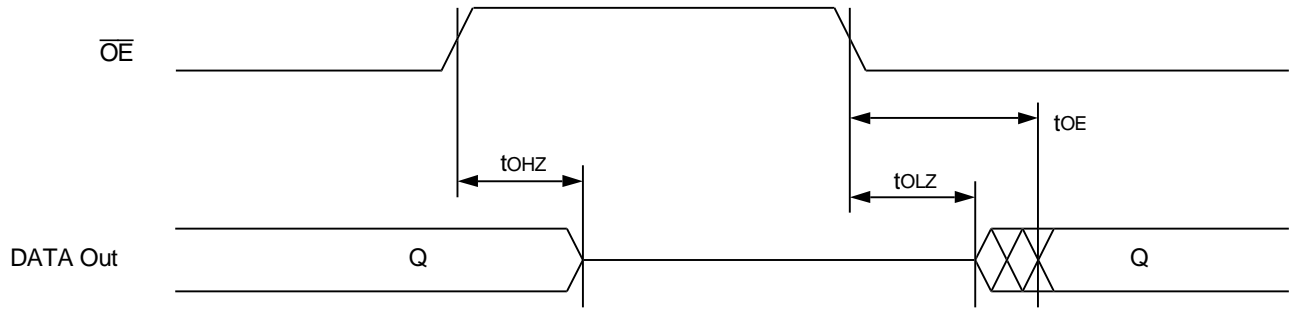
119 Ball Grid Array (BGA) Package Diagram Outline



165 Fine Pitch Ball Grid Array (fBGA) Package Diagram Outline



Timing Waveform of \overline{OE} Operation (1)

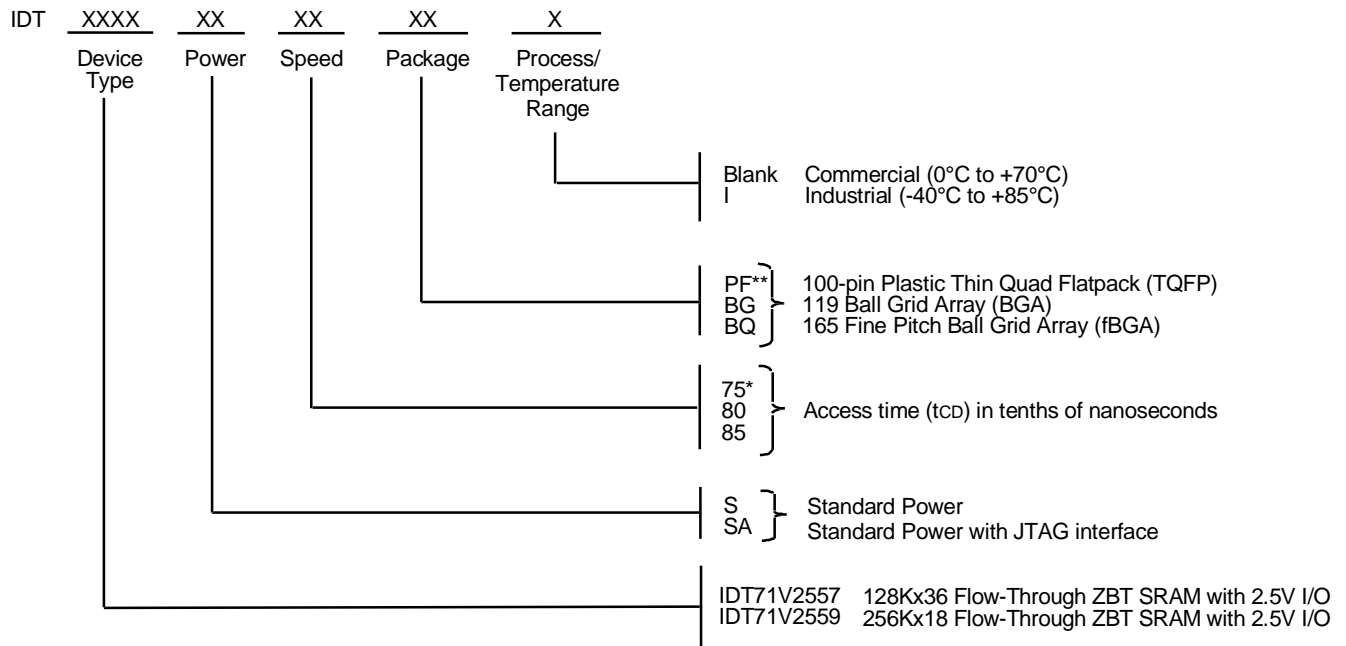


4878 drw 11

NOTE:

1. A read operation is assumed to be in progress.

Ordering Information



* Commercial temperature range only.

**JTAG (SA version) is not available with 100-pin TQFP package

4878 drw 12

Datasheet Document History

6/30/99		Updated to new format
8/23/99	Pg. 5, 6	Added Pin 64 to Note 1 and changed Pins 38, 42, and 43 to DNU
	Pg. 7	Changed U2–U6 to DNU
	Pg. 15	Improved t _{CH} , t _{CL} ; revised t _{CLZ}
	Pg. 21	Added BGA package diagrams
	Pg. 23	Added Datasheet Document History
12/31/99	Pg. 5, 14, 15, 22	Added Industrial Temperature Range offerings
05/02/00	Pg. 5, 6	Insert clarification note to Recommended Operating Temperature and Absolute Max Ratings tables
	Pg. 5, 6, 7	Clarify note to TQFP and BGA pin configuration; corrected typo in pinout
	Pg. 6	Add BGA capacitance
	Pg. 21	Add TQFP Package Diagram Outline
05/26/00		Add new package offering, 13 x 15mm 165 fBGA
	Pg. 23	Correct 119 BGA Package Diagram Outline
07/26/00	Pg. 5-7	Add ZZ, sleep mode reference note to TQFP, BG119, and BQ 165 pinouts
	Pg. 8	Update BQ165 pinout
	Pg. 23	Update BG119 package diagram dimensions
10/25/00		Remove Preliminary Status
	Pg. 8	Add reference note to pin N5 on BQ165 pinout, reserved for JTAG $\overline{\text{TRST}}$
05/20/02	Pg. 1-8, 15, 22, 23, 27	Added JTAG "SA" version functionality and updated ZZ pin descriptions and notes
10/15/04	Pg. 7	Updated pin configuration for the 119 BGA - reordered I/O signals on P6, P7 (128K x 36) and P7, N6, L6, K7, H6, G7, F6, E7, D6 (256K x 18).



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