

The documentation and process conversion measures necessary to comply with this document shall be completed by 5 September 2007.

INCH-POUND

MIL-PRF-19500/350K  
5 June 2007  
SUPERSEDING  
MIL-PRF-19500/350J  
10 April 2006

## PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, PNP, SILICON, LOW POWER  
TYPES 2N3867, 2N3867S, 2N3867U4, 2N3868, 2N3868S, AND 2N3868U4,  
JAN, JANTX, JANTXV, JANS, JANHCA, JANHCB, JANKCA, AND JANKCB

This specification is approved for use by all Departments  
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of  
this specification sheet and MIL-PRF-19500.

### 1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, switching transistor. Four levels of product assurance are provided for each encapsulated device type and two levels of product assurance are provided for each unencapsulated device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (TO- 5, TO-39), figure 2 (for encapsulated devices), figure 3, and figure 4 (for unencapsulated devices).

1.3 Maximum ratings. Unless otherwise specified,  $T_A = +25^\circ\text{C}$ .

Types	$P_T (1)$ $T_A =$ $+25^\circ\text{C}$	$P_T (1)$ $T_{PCB} =$ $+25^\circ\text{C}$	$P_T (2)$ $T_C =$ $+25^\circ\text{C}$	$R_{\theta JA}$	$R_{\theta PCB}$	$R_{\theta JC}$	$V_{CBO}$	$V_{CEO}$	$V_{EBO}$	$I_C$	$T_J$ and $T_{STG}$
	<u>W</u>	<u>W</u>	<u>W</u>	<u><math>^\circ\text{C/W}</math></u>	<u><math>^\circ\text{C/W}</math></u>	<u><math>^\circ\text{C/W}</math></u>	<u>V dc</u> Min	<u>V dc</u> Min	<u>V dc</u>	<u>A dc</u>	<u><math>^\circ\text{C}</math></u>
2N3867, S	1.0		10	175		17.5	40	40	4.0	3.0	-65 to +200
2N3868, S	1.0		10	175		17.5	60	60	4.0	3.0	-65 to +200
2N3867U4		1.0	35		175	5	40	40	4.0	3.0	-65 to +200
2N3868U4		1.0	35		175	5	60	60	4.0	3.0	-65 to +200

(1) For derating, see figure 5, 6, 7 and 8.

(2) For thermal curves, see figures 9, 10, 11 and 12.

Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dsc.dla.mil](mailto:Semiconductor@dsc.dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

## 1.4 Primary electrical characteristics.

	$h_{FE}$				$C_{obo}$ $I_E = 0$	$ h_{fe} $ $I_C = 100 \text{ mA dc}$	$I_C = 1.5 \text{ A dc}$		$V_{CE(sat)2}$ $I_C = 1.5 \text{ A dc}$
	$I_C = 1.5 \text{ A dc}$ $V_{CE} = 2 \text{ V dc}$		$I_C = 3.0 \text{ A dc}$ $V_{CE} = 5 \text{ V dc}$		$V_{CB} = 10 \text{ V dc}$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	$V_{CE} = 5 \text{ V dc}$ $f = 20 \text{ MHz}$	$I_B = 150 \text{ mA dc}$		$I_B = 150 \text{ mA dc}$
							$t_{on}$	$t_{off}$	
	2N3867 2N3867S 2N3867U4	2N3868 2N3868S 2N3868U4	2N3867 2N3867S 2N3867U4	2N3868 2N3968S 2N3968U4	pF		ns max	ns max	V dc
Min	40	30	20	20		3			
Max	200	150			120	12	100	600	0.75

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

## DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

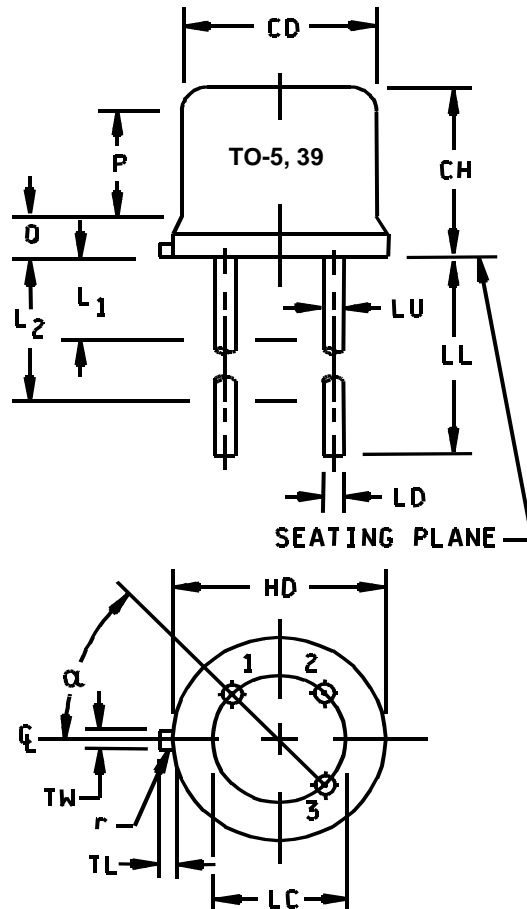
## DEPARTMENT OF DEFENSE STANDARD

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	5, 6
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	4, 5
LC	.200 TP		5.08 TP		7
LD	.016	.019	0.41	0.48	8,9
LL	See note 8, 14				
LU	.016	.019	0.41	0.48	8,9
L1		.050		1.27	8,9
L2	.250		6.35		8,9
P	.100		2.54		7
Q		.030		0.76	5
TL	.029	.045	0.74	1.14	3,4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
$\alpha$	45° TP		45° TP		7
1, 2, 10, 12, 13, 14					

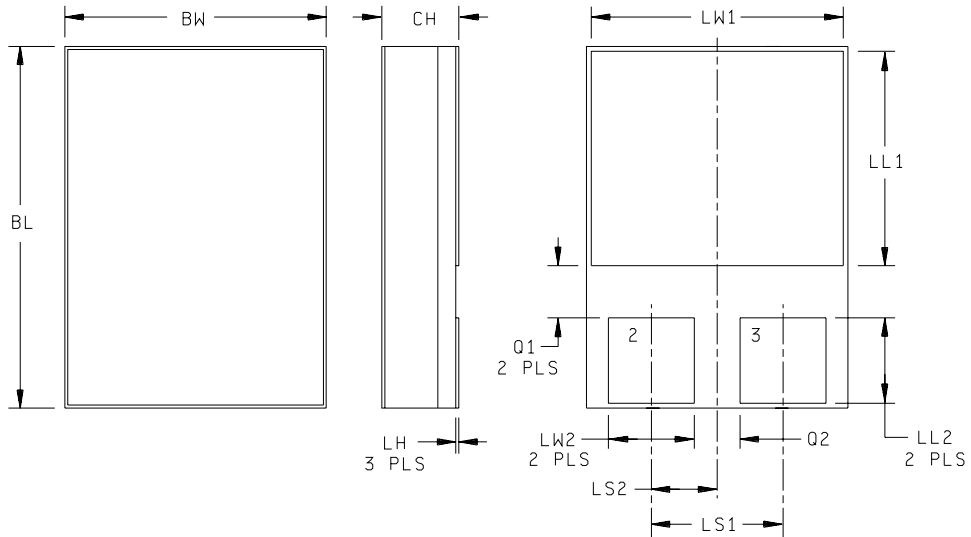


NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
8. Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in and beyond LL minimum.
9. All three leads.
10. The collector shall be internally connected to the case.
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
14. For non-S-suffix devices (TO-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For S-suffix types (TO-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

FIGURE 1. Physical dimensions (similar to TO-5, TO-39).

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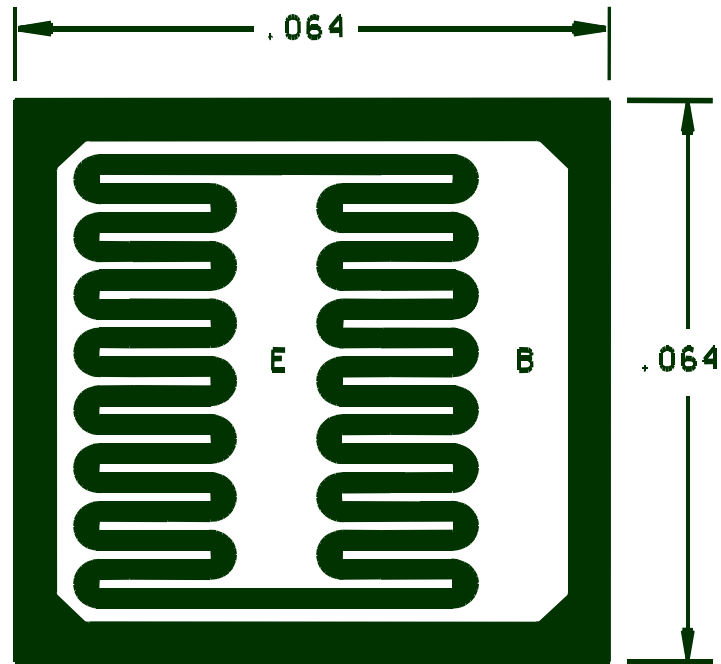


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.215	.225	5.46	5.72
BW	.145	.155	3.68	3.94
CH	.050	.070	1.27	1.77
LH		.020		0.50
LW1	.135	.145	3.43	3.68
LW2	.047	.057	1.19	1.45
LL1	.085	.125	2.16	3.17
LL2	.045	.075	1.14	1.91
LS1	.065	.095	1.65	2.41
LS2	.033	.048	.838	1.21
Q1	.045	.070	1.14	1.78
Q2	.025	.048	.635	1.22
TERM 1	Collector			
TERM 2	Base			
TERM 3	Emitter			

NOTES:

1. Dimensions are in inches.
2. Millimeter equivalents are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.

FIGURE 2. Physical dimensions and configuration (SMD.22, U4).

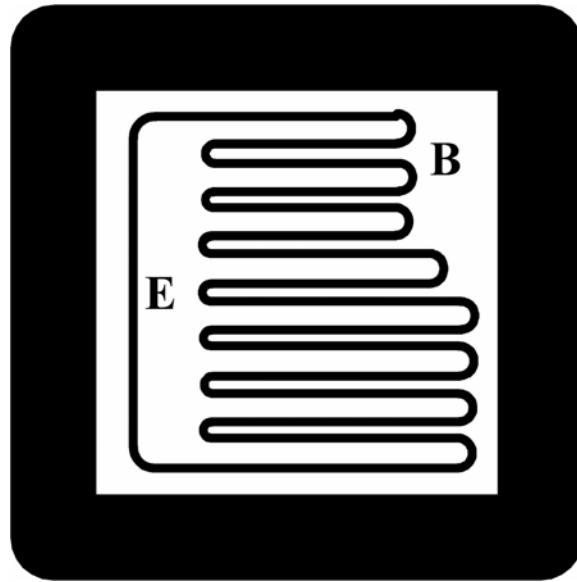


A version

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Unless otherwise specified, tolerance is  $\pm .005$  inch (0.13 mm).
4. The physical characteristics of the die are:
  - Thickness: .008 inch (0.20 mm) minimum, .012 inch (0.30 mm) maximum.
  - Top metal: Aluminum 25,000 Å nominal.
  - Back metal: Gold 2,500 Å minimum, 3,000 Å nominal.
  - Back side: Collector; Bonding pad: B = .045 inch (1.14 mm) x .008 inch (0.20 mm).  
E = .039 inch (0.99 mm) x .008 inch (0.20 mm).

FIGURE 3. JANHCA and JANKCA die dimensions.



B version

1. Chip size: .075 x .075 inch  $\pm$ .002 inch (1.905 x 1.905 mm  $\pm$ 0.051 mm).
2. Chip thickness: .010  $\pm$ .0015 inch nominal (0.254  $\pm$ 0.0381 mm).
3. Top metal: Aluminum 30,000 Å minimum, 33,000 Å nominal.
4. Back metal:
  - A. Al/Ti/Ni/Ag 15kÅ/3kÅ/7kÅ/7kÅ min., 18kÅ/5kÅ/10kÅ/10kÅ nom.
  - B. Gold 3,500Å minimum, 5,000Å nominal.
5. Backside: Collector.
6. Bonding pad: B = .023 x .008 inch (0.5842 x 0.2032 mm), E = .049 x .008 inch (1.2446 x 0.2032 mm).

\* FIGURE 4. JANHCB and JANKCB die dimensions.

### 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1, 2, 3, and 4 herein.

3.4.1 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

\* 4.3 Screening (JANS, JANTXV, and JANTX levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3)	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.3)
9	$I_{CEX1}$ and $h_{FE2}$	Not applicable
10	24 hours minimum	24 hours minimum
11	$I_{CEX1}$ ; $h_{FE2}$ ; $\Delta I_{CEX1}$ = 100 percent of initial value or 200 nA dc, whichever is greater; $\Delta h_{FE2}$ = $\pm 15$ percent of initial value.	$I_{CEX1}$ ; $h_{FE2}$
12	See 4.3.2	See 4.3.2
13	Subgroup 2 and 3 of table I herein; $\Delta I_{CEX1}$ = 100 percent of initial value or 200 nA dc, whichever is greater; $\Delta h_{FE2}$ = $\pm 15$ percent of initial value.	Subgroup 2 of table I herein; $\Delta I_{CEX1}$ = 100 percent of initial value or 200 nA dc, whichever is greater; $\Delta h_{FE2}$ = $\pm 15$ percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500, "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.2 Power burn-in conditions. Power burn-in conditions are as follows:  $V_{CB} = 10 - 30$  V dc. Power shall be applied to achieve  $T_J = +135^\circ\text{C}$  minimum using a minimum  $P_D = 75$  percent of  $P_T$  maximum rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions,  $T_J$ , and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{MD}$  (and  $V_C$  where appropriate). See table II, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of subgroup 1 and 2 of table I herein, inspection only (table E-VIb, group B, subgroup 1 is not required to be performed since solderability and resistance to solvents testing is performed in table I herein).



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4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in E-VIa (JANS) and 4.4.2.1 herein. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and table III herein. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with table I, subgroup 2 and table III herein.

4.4.2.1 Group B inspection, appendix E, table E-VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$V_{CB} = 10$ V dc; 2,000 cycles adjust device current, or power, to achieve a minimum $\Delta T_J$ of $+100^\circ\text{C}$ .
B5	1027	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) $V_{CB} = 10$ V dc, $P_D \geq 100$ percent of maximum rated $P_T$ (see 1.3).  Option 1: For 96 hours minimum sample size in accordance with table VIa of MIL-PRF-19500, adjust $T_A$ or $P_D$ to achieve $T_J = +275^\circ\text{C}$ minimum.  Option 2: For 216 hours minimum, sample size = 45, $c = 0$ ; adjust $T_A$ or $P_D$ to achieve $T_J = +225^\circ\text{C}$ minimum.
B6	3131	For TO-5 and TO-39 use $R_{\theta JA}$ , for U4 use $R_{\theta JC}$ , see 1.3.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated $P_T$ as defined in 1.3. $n = 45$ devices, $c = 0$ . The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, $T_A = +150^\circ\text{C}$ , $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$ .
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$ . $n = 22$ , $c = 0$ .

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.
- b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

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4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with table I, subgroup 2 and table III herein.

4.4.3.1 Group C inspection, table VII (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, not applicable for U4 devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and 4.3.3) and in accordance with thermal impedance curves.
C6	1026	1,000 hours at $V_{CB} = 10$ V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 75$ percent of maximum rated $P_T$ as defined in 1.3 $n = 45$ , $c = 0$ . The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection, table VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, not applicable for U4 devices..
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and 4.3.3) and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes group A tests for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

\* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) and delta measurements shall be in accordance with the applicable steps of table I, subgroup 2; and table III herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvent <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Temperature cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>5/</u>	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Electrical measurements <u>4/</u>		Table I, subgroup 2				
Bond strength <u>3/ 4/</u>	2037	Precondition T <sub>A</sub> = +250°C at t = 24 hrs or T <sub>A</sub> = +300°C at t = 2 hrs, n = 11 wires, c = 0.				
Decap internal visual (design verification) <u>4/</u>	2075	n = 4 devices, c = 0.				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.3	Z <sub>θJX</sub>			°C/W
Collector to base cutoff current	3036		I <sub>CBO1</sub>			
2N3867, 2N3867S, 2N3867U4		V <sub>CB</sub> = 40 V dc		100		μA dc
2N3868, 2N3868S, 2N3868U4		V <sub>CB</sub> = 60 V dc		100		μA dc
Emitter to base cutoff current	3061	Bias condition D; V <sub>EB</sub> = 4 V dc	I <sub>EBO1</sub>	100		μA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I <sub>C</sub> = 20 mA dc; pulsed (see 4.5.1)	V <sub>(BR)CEO</sub>			
2N3867, 2N3867S, 2N3867U4				40		V dc
2N3868, 2N3868S, 2N3868U4				60		V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> – Continued						
Collector to emitter cutoff current	3041	Bias condition A; $V_{EB} = 2.0$ V dc	$I_{CEX1}$		1.0	$\mu$ A dc
2N3867, 2N3867S, 2N3867U4 2N3868, 2N3868S, 2N3868U4		$V_{CE} = 40$ V dc, $V_{CE} = 60$ V dc				
Forward-current transfer ratio	3076	$V_{CE} = 1.0$ V dc, $I_C = 500$ mA dc, pulsed (see 4.5.1)	$h_{FE1}$			
2N3867, 2N3867S, 2N3867U4 2N3868, 2N3868S, 2N3868U4				50 35		
Forward-current transfer ratio	3076	$V_{CE} = 2.0$ V dc, $I_C = 1.5$ A dc, pulsed (see 4.5.1)	$h_{FE2}$			
2N3867, 2N3867S, 2N3867U4 2N3868, 2N3868S, 2N3868U4				40 30	200 150	
Forward-current transfer ratio	3076	$V_{CE} = 3.0$ V dc, $I_C = 2.5$ A dc, pulsed (see 4.5.1)	$h_{FE3}$			
2N3867, 2N3867S, 2N3867U4 2N3868, 2N3868S, 2N3868U4				25 20		
Forward-current transfer ratio	3076	$V_{CE} = 5.0$ V dc, $I_C = 3.0$ A dc, pulsed (see 4.5.1)	$h_{FE4}$	20		
Collector to emitter voltage (saturated)	3071	$I_C = 500$ mA dc; $I_B = 50$ mA dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.5	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 1.5$ A dc; $I_B = 150$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		0.75	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 2.5$ A dc; $I_B = 250$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)3}$		1.5	V dc
Base emitter voltage (saturated)	3066	Test condition A; $I_C = 500$ mA dc; $I_B = 50$ mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.0	V dc
Base emitter voltage (saturated)	3066	Test condition A; $I_C = 1.5$ A dc; $I_B = 150$ mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$			
2N3867, 2N3867S, 2N3868, 2N3868S 2N3867U4, 2N3868U4				0.9 0.85	1.4 1.4	V dc V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - continued.						
Base emitter voltage (saturated)	3066	Test condition A; $I_C = 2.5$ A dc; $I_B = 250$ mA dc;pulsed (see 4.5.1)	$V_{BE(sat)3}$		2.0	V dc
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +150^\circ\text{C}$				
Collector to emitter cutoff current	3041	Bias condition A, $V_{EB} = 2.0$ V dc	$I_{CEX2}$		50	$\mu\text{A}$ dc
2N3867, 2N3867S, 2N3867U4 2N3868, 2N3868S, 2N3868U4		$V_{CE} = 40$ V dc $V_{CE} = 60$ V dc				
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 1.0$ V dc, $I_C = 500$ mA dc, pulsed (see 4.5.1)	$h_{FE5}$			
2N3867, 2N3867S, 2N3867U4 2N3868, 2N3868S, 2N3868U4				25 17		
<u>Subgroup 4</u>						
Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 5$ V dc, $I_C = 100$ mA dc, $f = 20$ MHz	$ h_{fe} $	3	12	
Open circuit output capacitance	3236	$V_{CB} = 10$ V dc, $I_E = 0$ , $100$ kHz $\leq f \leq 1$ MHz	$C_{obo}$		120	pF
Input capacitance (output open-circuited)	3240	$V_{EB} = 3.0$ V dc, $I_C = 0$ , $100$ kHz $\leq f \leq 1$ MHz	$C_{ibo}$		800	pF
<u>Subgroup 5</u>						
Pulse response	3251	Test condition A				
Delay time		$V_{CC} = -30$ V dc, $V_{EB} = 0$ , $I_C = 1.5$ A dc, $I_{B1} = 150$ mA dc, See figure 13	$t_d$		35	ns

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> - Continued						
Pulse response	3251	Test condition A				
Rise time		$V_{CC} = -30$ V dc, $V_{EB} = 0$ V dc, $I_C = 1.5$ A dc, $I_{B1} = 150$ mA dc, See figure 13	$t_r$		65	ns
Storage time		$V_{CC} = -30$ V dc, $V_{EB} = 0$ V dc, $I_C = 1.5$ A dc, $I_{B1} = I_{B2} = 150$ mA dc, See figure 14	$t_s$		500	ns
Fall time		$V_{CC} = -30$ V dc, $V_{EB} = 0$ V dc, $I_C = 1.5$ A dc, $I_{B1} = I_{B2} = 150$ mA dc, See figure 14	$t_f$		100	ns
SOA (continuous dc)	3051	$T_C = +25^\circ\text{C}$ , 1 cycle, $t = 1.0$ s, (see figure 15)				
<u>Test 1</u>		$V_{CE} = 3.33$ V dc, $I_C = 3$ A dc				
<u>Test 2</u>						
2N3867, 2N3867S, 2N3867U4		$V_{CE} = 40$ V dc, $I_C = 160$ mA dc				
2N3868, 2N3868S, 2N3868U4		$V_{CE} = 60$ V dc, $I_C = 80$ mA dc				
Electrical measurements		See table III, steps 1 and 2.				

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for JANS devices.

5/ Not required for laser marked devices.

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TABLE II. Group E inspection (all quality levels) - for qualification and re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I, subgroup 2 and table III herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	V <sub>CB</sub> = 10 V dc, 6,000 cycles, adjust device current, or power, to achieve a minimum $\Delta T_J$ of +100°C. Forced air cooling allowed on cooling cycle only.	
Electrical measurements		See table I, subgroup 2 and table III herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See MIL-PRF-19500.	Sample size N/A
<u>Subgroups 5</u>			
Not applicable			
<u>Subgroup 6</u>			3 devices c = 0
ESD	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	

TABLE III. Delta requirements.

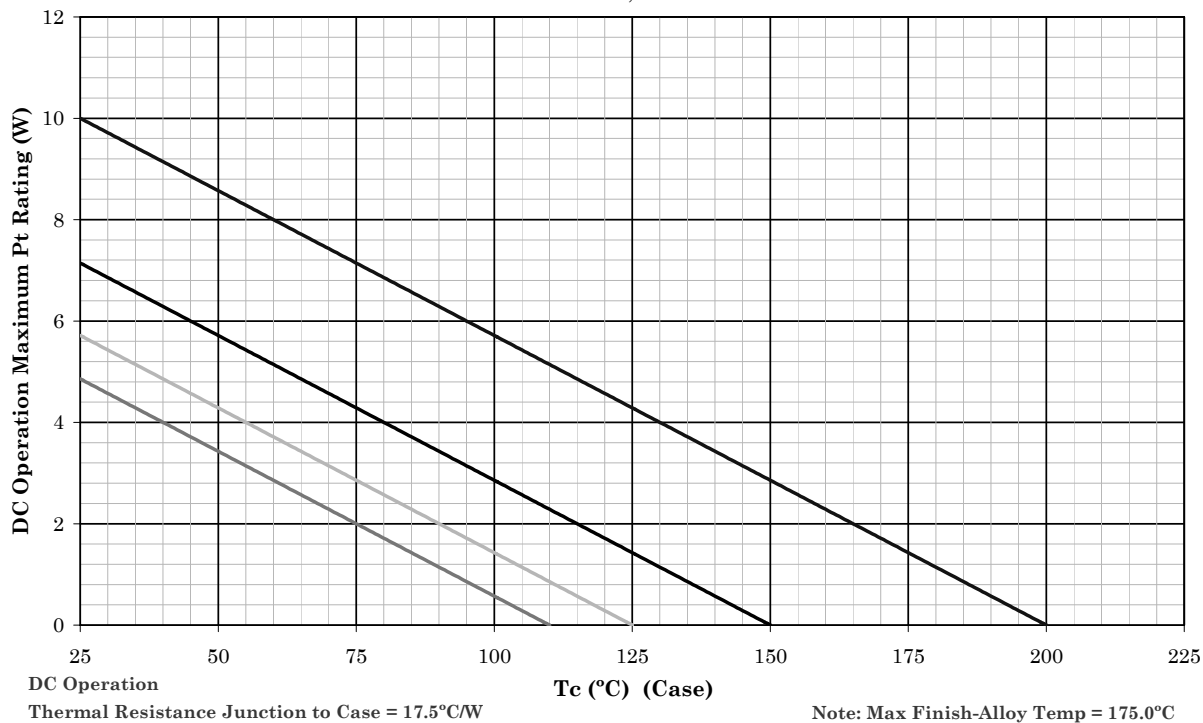
Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current  2N3867, 2N3867S 2N3868, 2N3868S	3041	Bias condition A, $V_{EB} = 2.0$ V dc  $V_{CE} = 40$ V dc $V_{CE} = 60$ V dc	$\Delta I_{CEX1}$ <u>1/</u>	100 percent of initial value or 200 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	$V_{CE} = 2$ V dc; $I_C = 1.5$ A dc; pulsed see 4.5.1	$\Delta h_{FE2}$ <u>1/</u>	15 percent change from initial reading.	

1/ Devices which exceed the table I limits for this test shall not be accepted.



### Temperature-Power Derating Curve

TC=25°C 2N3867, 2N3868



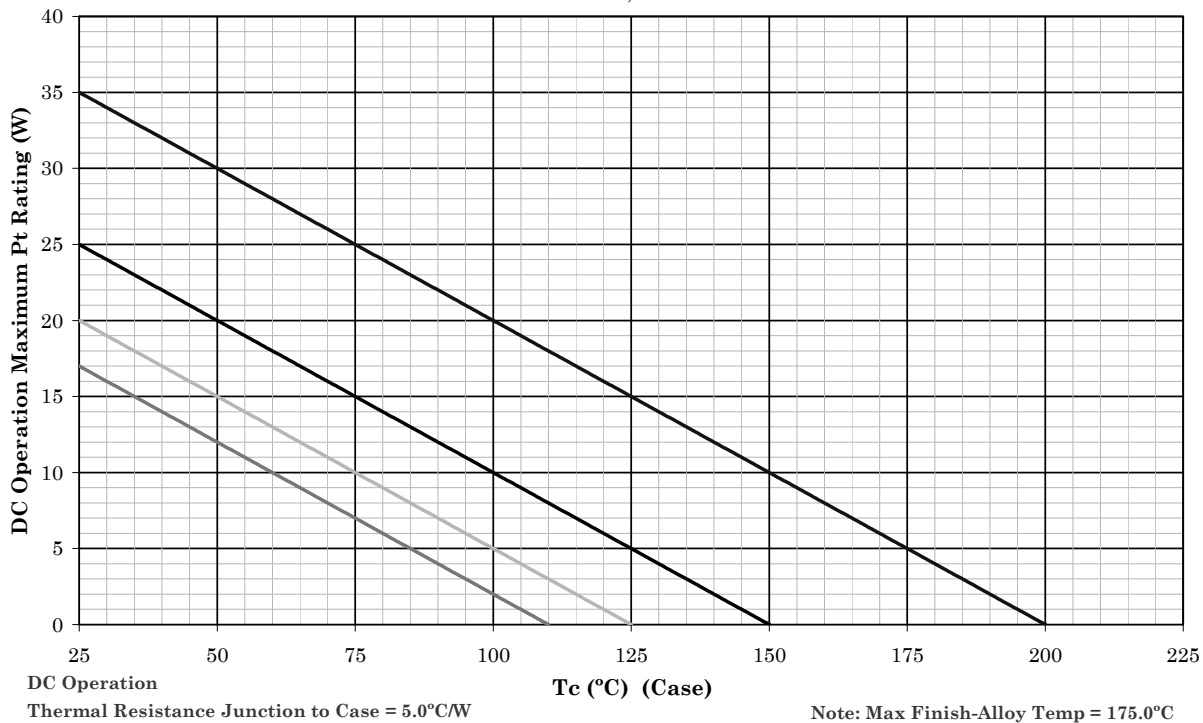
**NOTES:**

1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 5. Derating for 2N3867, 2N3868 (TO-5, TO-39).

### Temperature-Power Derating Curve

TC=25°C 2N3867U4, 2N3868U4



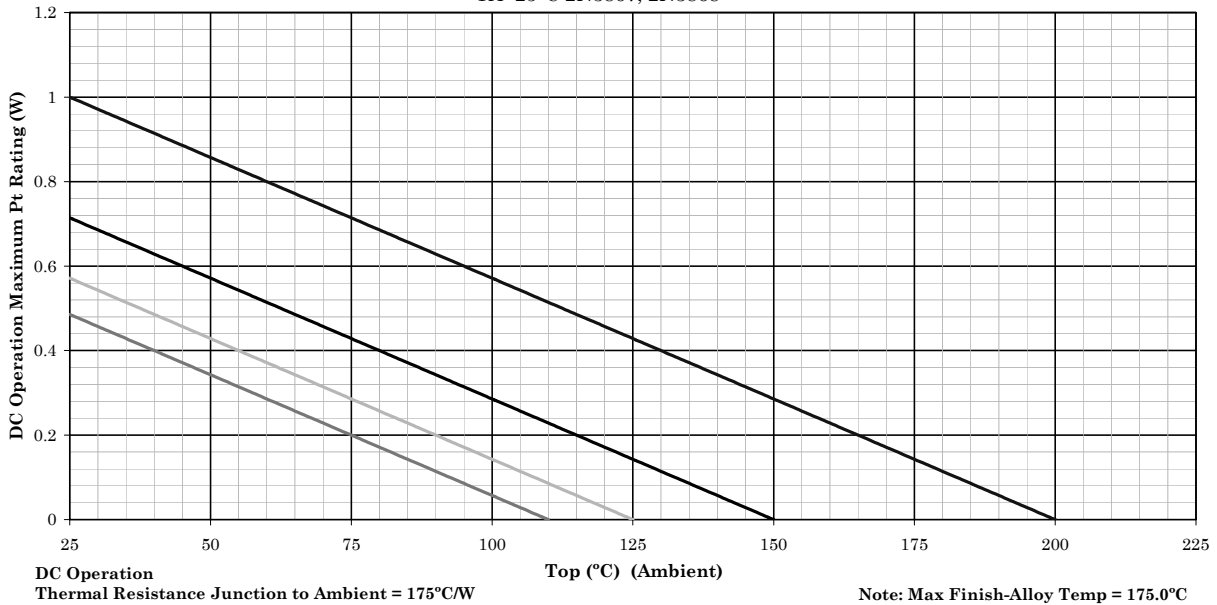
**NOTES:**

1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 6. Derating for 2N3867U4, 2N3868U4.

## Temperature-Power Derating Curve

TA=25°C 2N3867, 2N3868



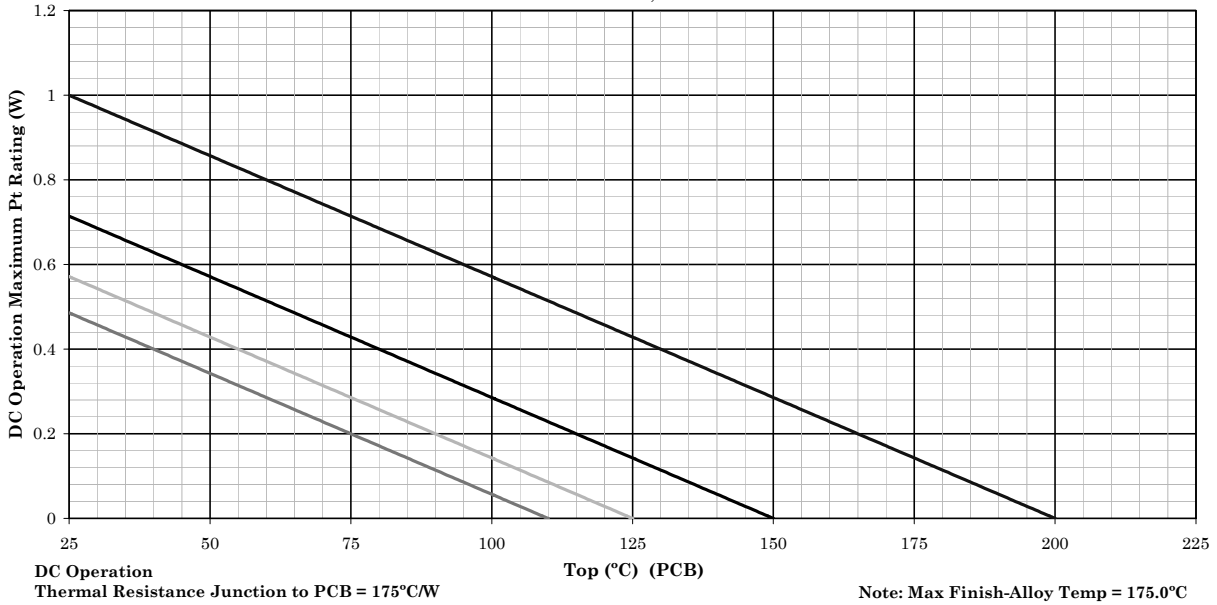
### NOTES:

1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 7. Derating for 2N3867, 2N3868.

### Temperature-Power Derating Curve

TPCB=25°C 2N3867U4, 2N3868U4



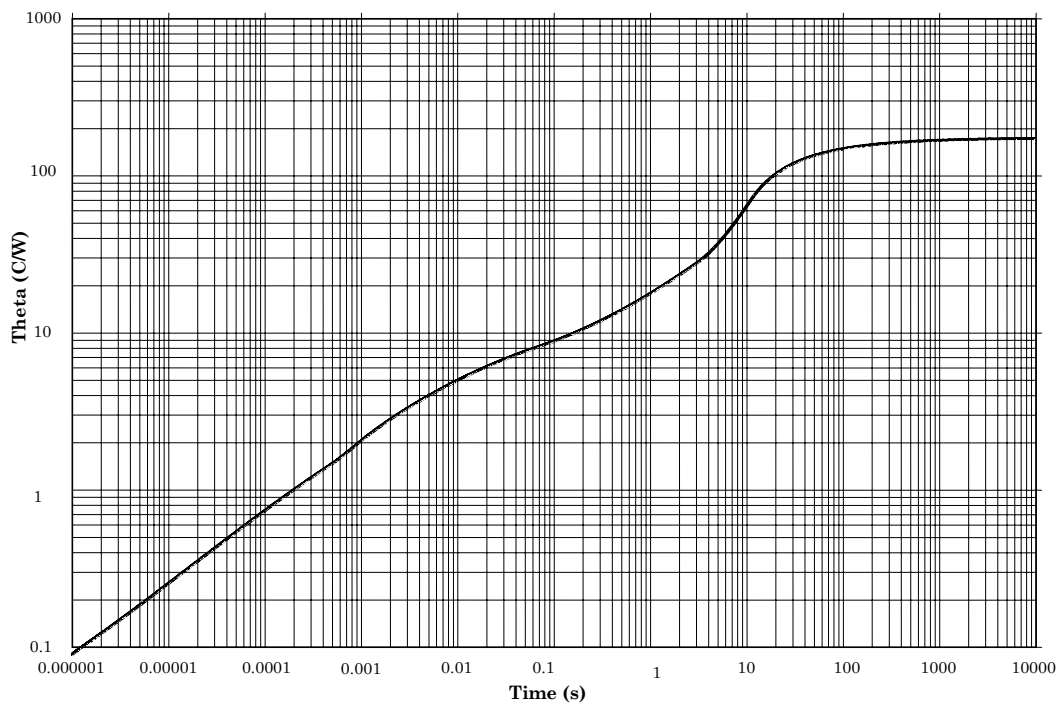
**NOTES:**

1. All devices are capable of operating at  $\leq T_J$  specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum  $T_J$  allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 8. Derating for 2N3867U4, 2N3868U4.

**Maximum Thermal Impedance**

Free Air  $T_a=25^\circ\text{C}$



$R_{\theta JA} = 175^\circ\text{C/W}$

FIGURE 9. Thermal impedance for 2N3867 and 2N3868 (TO-5 and TO-39).

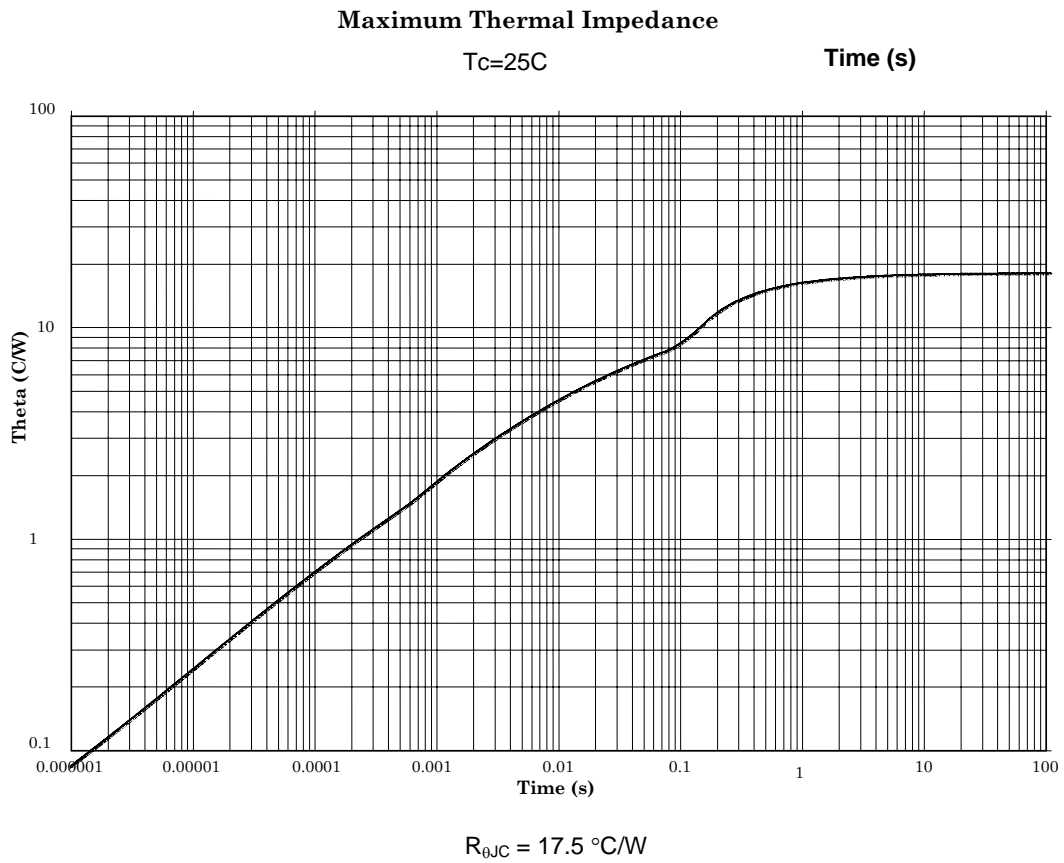
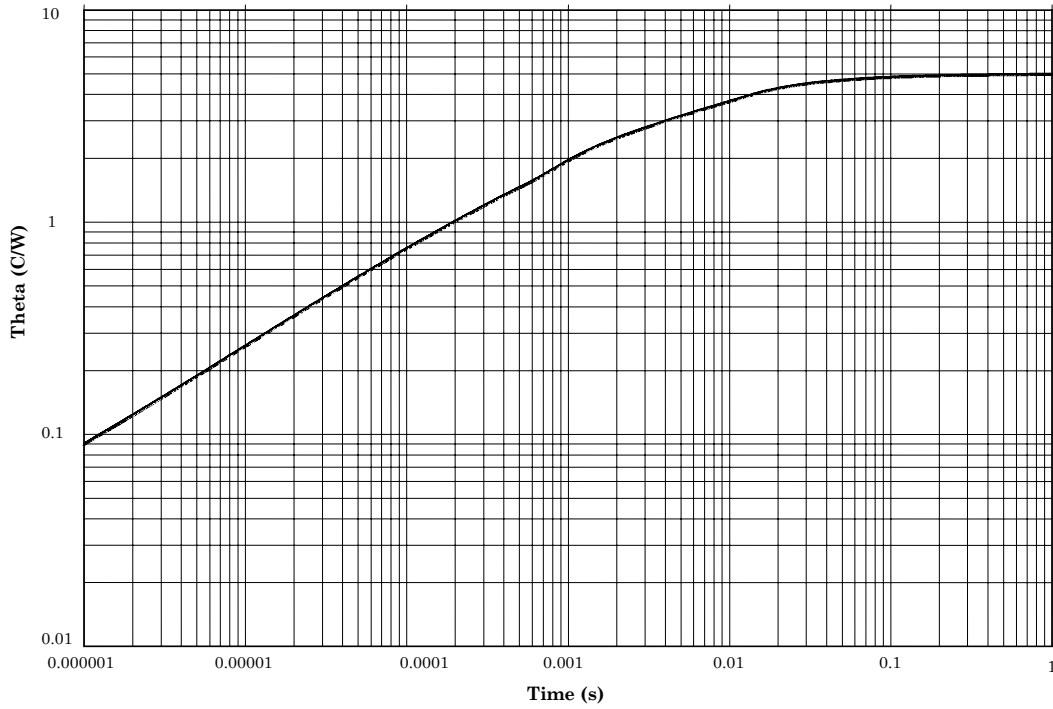


FIGURE 10. Thermal impedance for 2N3867 and 2N3868 (TO-5 and TO-39).

**Maximum Thermal Impedance**

Solder mounted to copper heatsink at  $T_c=25^\circ\text{C}$



$R_{\theta JC} = 5^\circ\text{C/W}$

FIGURE 11. Thermal impedance for 2N3867U4, 2N3868U4.

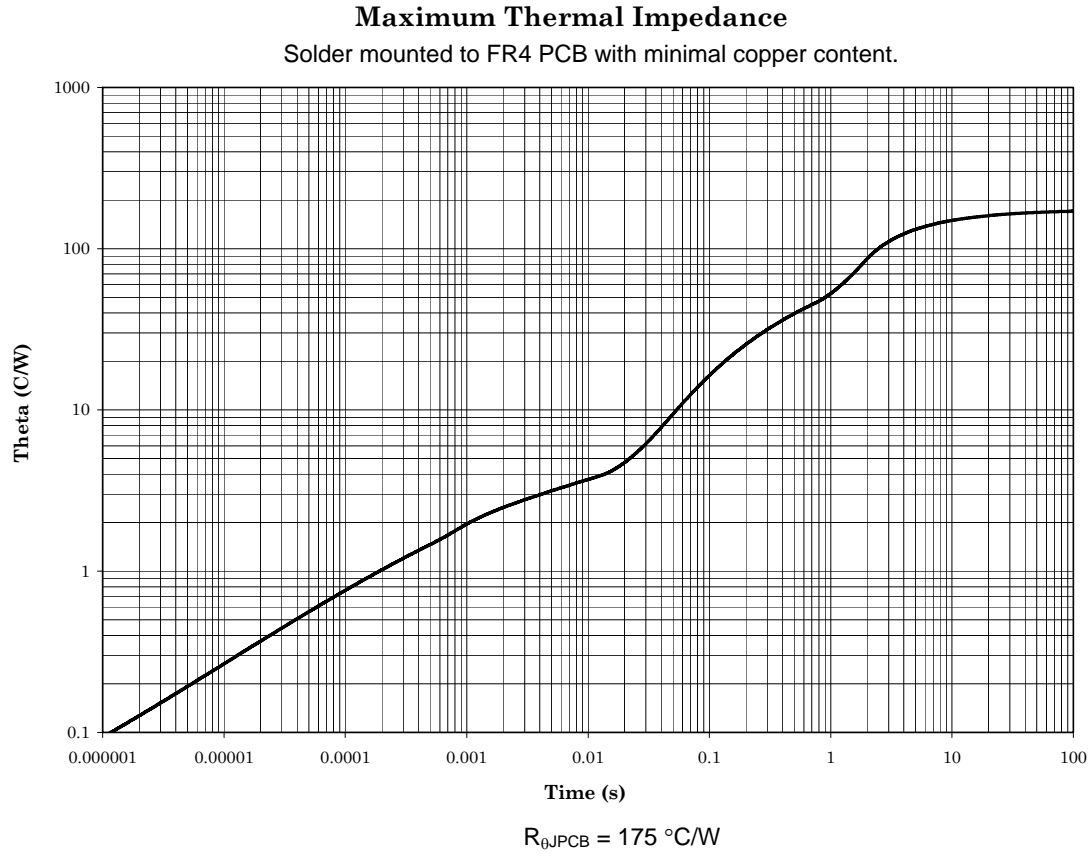


FIGURE 12. Thermal impedance for 2N3867U4, 2N3868U4.



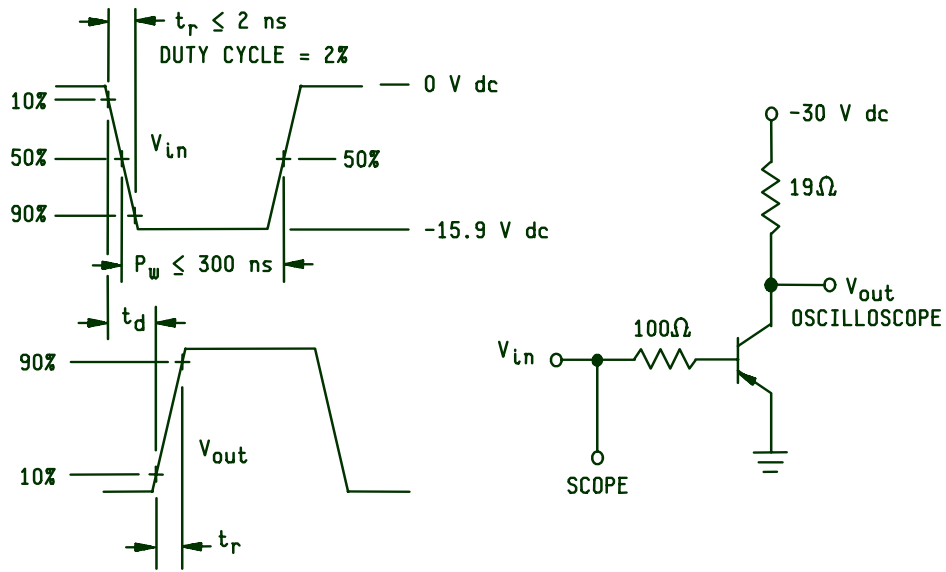


FIGURE 13. Equivalent circuit for measuring delay and rise times.

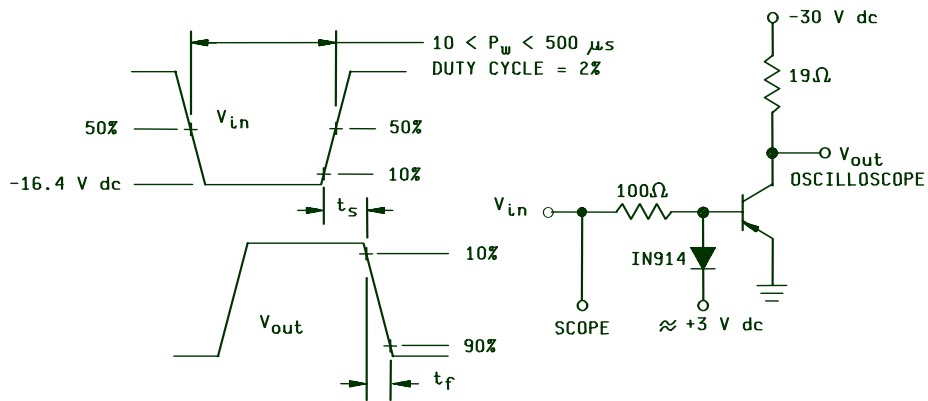


FIGURE 14. Equivalent circuit for measuring storage and fall times.

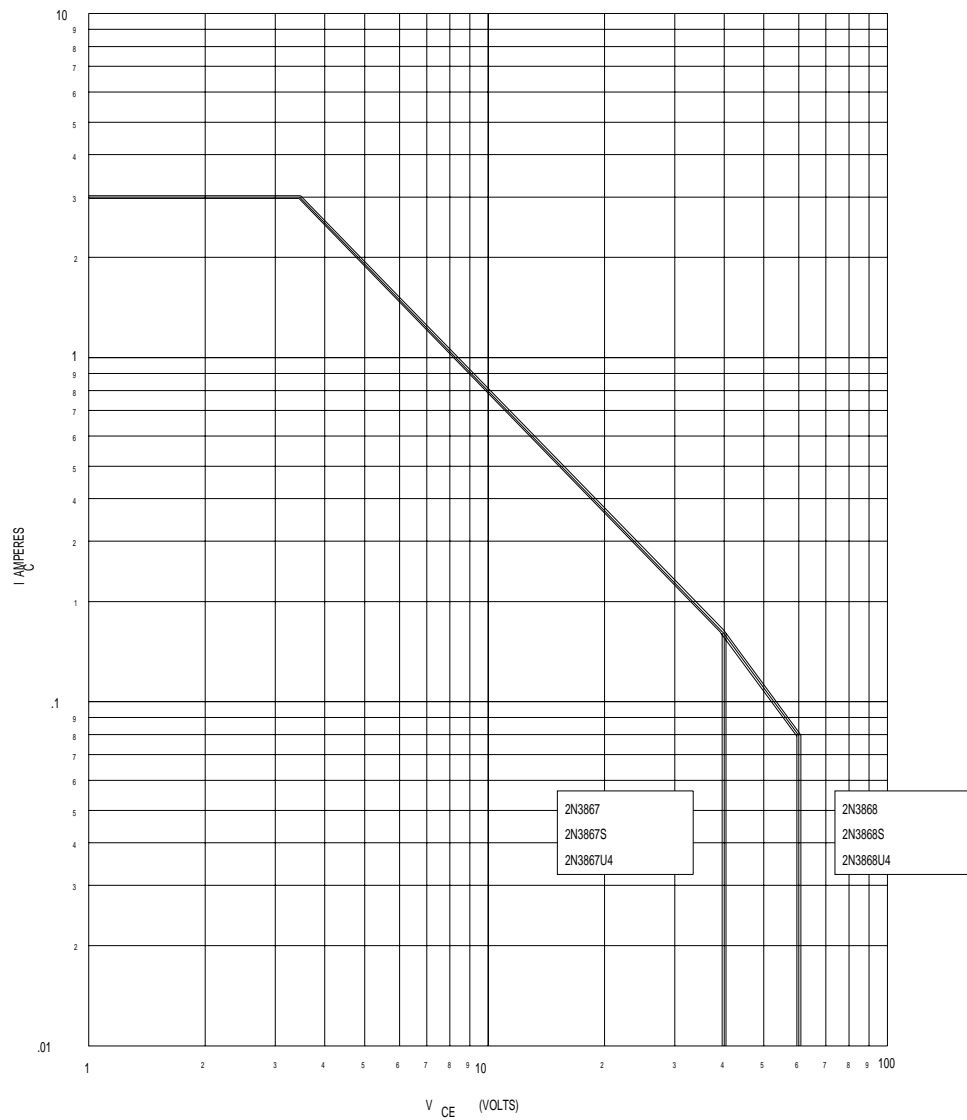


FIGURE 15. Maximum SOA graph (continuous dc).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

\* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

\* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil).

6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example, JANHCA2N3867) will be identified on the QML.

JANHC and JANKC ordering information		
PIN	Manufacturers	
	33178	43611
2N3867	JANHCA2N3867, JANKCA2N3867	JANHCB2N3867, JANKCB2N3867
2N3868	JANHCA2N3868, JANKCA2N3868	JANHCB2N3868, JANKCB2N3868

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR  
Navy - EC  
Air Force - 11  
DLA - CC

Preparing activity:  
DLA - CC

(Project 5961-2007-023)

Review activities:

Army - AR, AV, MI, SM  
Navy - AS, MC  
Air Force - 19, 71, 99

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