FAIRCHILD

SEMICONDUCTOR ™

March 1998

SCAN18245T
Non-Inverting Transceiver with 3-STATE Outputs
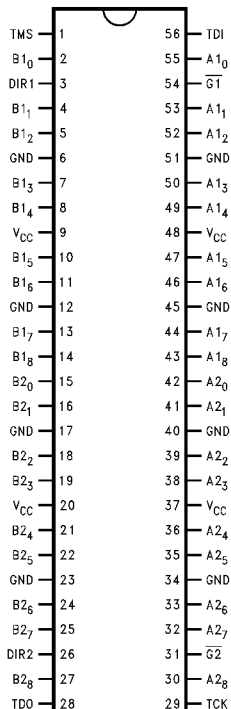
General Description

The SCAN18245T is a high speed, low-power bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Dual output enable control signals
- 3-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 32 mA/sink 64 mA (Comm), source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch SSOP (Shrink Small Outline Package)
- Includes CLAMP and HIGHZ instructions
- Member of Fairchild's SCAN Products
- Available as Known Good Die

Ordering Code:

Connection Diagram

Pin		Pin
TMS — 1		56 — TDI
$B1_0$ — 2		55 — $A1_0$
DIR1 — 3		54 — $\overline{G1}$
$B1_1$ — 4		53 — $A1_1$
$B1_2$ — 5		52 — $A1_2$
GND — 6		51 — GND
$B1_3$ — 7		50 — $A1_3$
$B1_4$ — 8		49 — $A1_4$
V_{CC} — 9		48 — V_{CC}
$B1_5$ — 10		47 — $A1_5$
$B1_6$ — 11		46 — $A1_6$
GND — 12		45 — GND
$B1_7$ — 13		44 — $A1_7$
$B1_8$ — 14		43 — $A1_8$
$B2_0$ — 15		42 — $A2_0$
$B2_1$ — 16		41 — $A2_1$
GND — 17		40 — GND
$B2_2$ — 18		39 — $A2_2$
$B2_3$ — 19		38 — $A2_3$
V_{CC} — 20		37 — V_{CC}
$B2_4$ — 21		36 — $A2_4$
$B2_5$ — 22		35 — $A2_5$
GND — 23		34 — GND
$B2_6$ — 24		33 — $A2_6$
$B2_7$ — 25		32 — $A2_7$
DIR2 — 26		31 — $\overline{G2}$
$B2_8$ — 27		30 — $A2_8$
TDO — 28		29 — TCK

DS010961-1

Pin Names	Description
$A1_{(0-8)}$	Side A1 Inputs or 3-STATE Outputs
$B1_{(0-8)}$	Side B1 Inputs or 3-STATE Outputs
$A2_{(0-8)}$	Side A2 Inputs or 3-STATE Outputs
$B2_{(0-8)}$	Side B2 Inputs or 3-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins
DIR1, DIR2	Direction of Data Flow Pins

Order Number	Description
SCAN18245TSSC	SSOP in Tubes
SCAN18245TSSCX	SSOP in Tape and Reel
SCAN18245TFMQB	Flatpak Military
5962-9311501MXA	Military SMD#

www.fairchildsemi.com

Truth Tables

Inputs		A1		B1
$\overline{G1}$	DIR1	(0–8)		(0–8)
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

Inputs		A2		B2
$\overline{G2}$	DIR2	(0–8)		(0–8)
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance

Functional Description

The SCAN18245 consists of two sets of nine non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B ports to A ports, when HIGH enables data from A ports to B ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B ports by placing them in a high impedance condition.
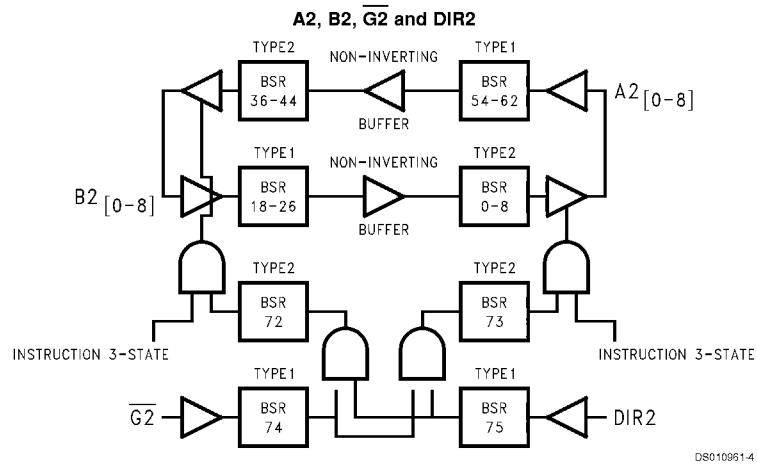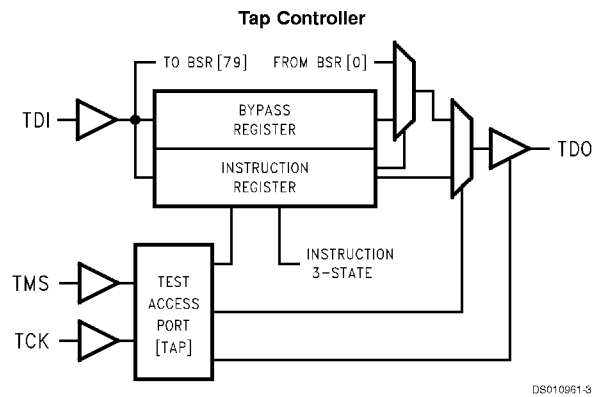
Block Diagrams

A1, B1, $\overline{G1}$ and DIR1
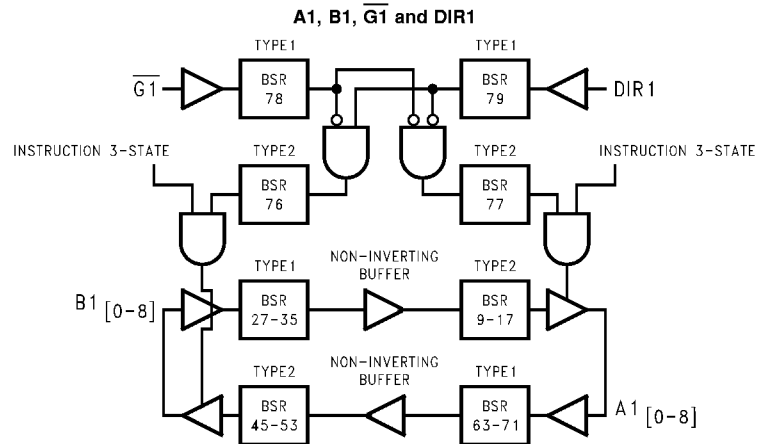
DS010961-2

Note: BSR stands for Boundary Scan Register.

Block Diagrams (Continued)

Tap Controller

DS010961-3

A2, B2, $\overline{G2}$ and DIR2

DS010961-4

Note: BSR stands for Boundary Scan Register.

Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0
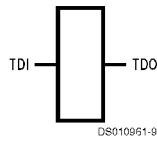
The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18245T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a "pseudo ID" code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

Instruction Register Scan Chain Definition
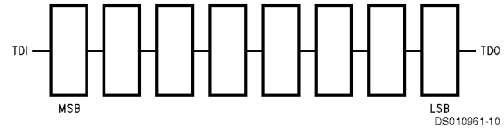
MSB → LSB

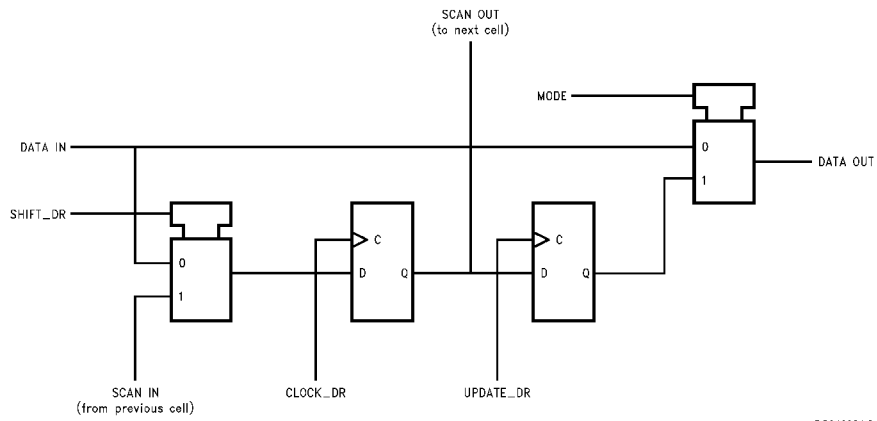| Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

Description of Boundary-Scan Circuitry (Continued)
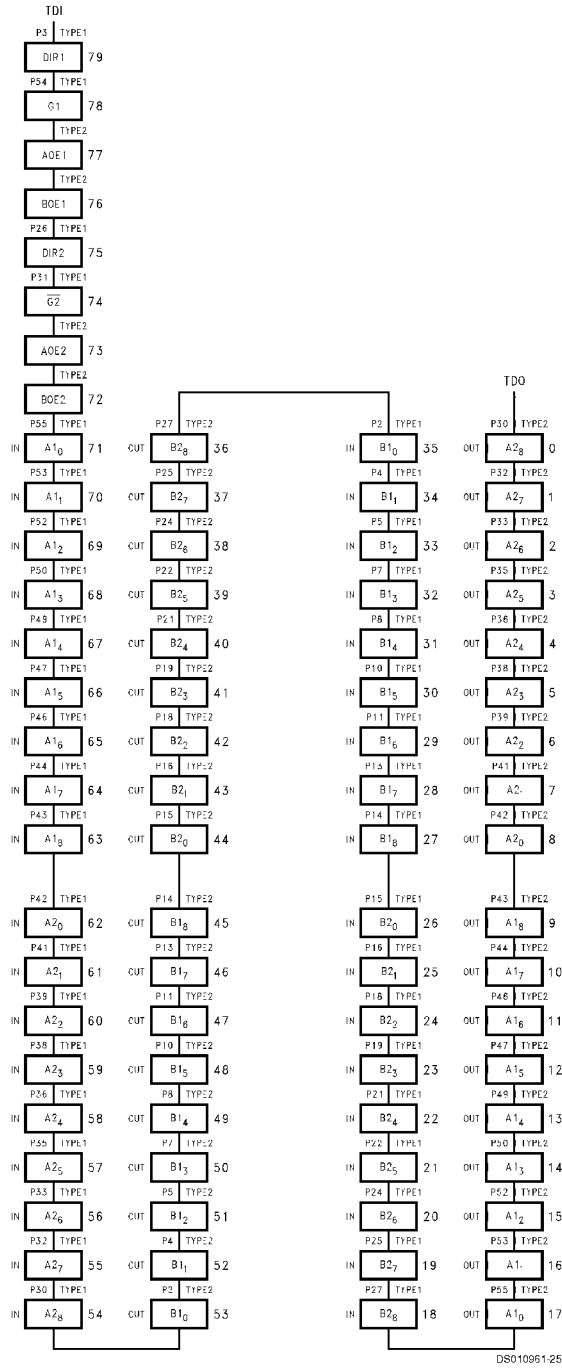
Scan Cell TYPE1
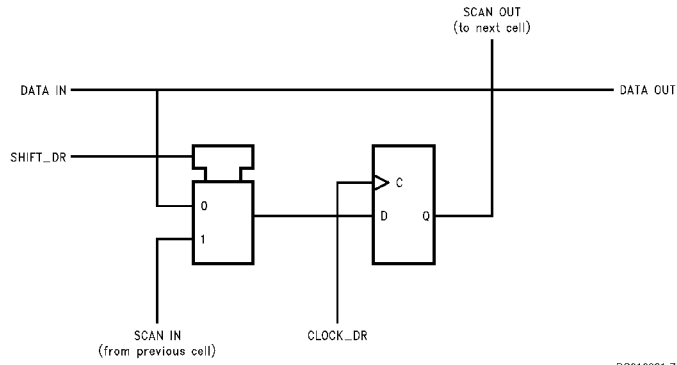
DS010961-7

Scan Cell TYPE2

DS010961-8

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register
Scan Chain Definition (80 Bits in Length)

TDI

P3	TYPE1	
DIR1		79
P54	TYPE1	
G1		78
	TYPE2	
AOE1		77
	TYPE2	
BOE1		76
P26	TYPE1	
DIR2		75
P31	TYPE1	
G2		74
	TYPE2	
AOE2		73
	TYPE2	
BOE2		72

TDO

Col1			Col2			Col3			Col4		
P55	TYPE1		P27	TYPE2		P2	TYPE1		P30	TYPE2	
IN	A1$_0$	71	OUT	B2$_8$	36	IN	B1$_0$	35	OUT	A2$_8$	0
P53	TYPE1		P25	TYPE2		P4	TYPE1		P32	TYPE2	
IN	A1$_1$	70	OUT	B2$_7$	37	IN	B1$_1$	34	OUT	A2$_7$	1
P52	TYPE1		P24	TYPE2		P5	TYPE1		P33	TYPE2	
IN	A1$_2$	69	OUT	B2$_6$	38	IN	B1$_2$	33	OUT	A2$_6$	2
P50	TYPE1		P22	TYPE2		P7	TYPE1		P35	TYPE2	
IN	A1$_3$	68	OUT	B2$_5$	39	IN	B1$_3$	32	OUT	A2$_5$	3
P49	TYPE1		P21	TYPE2		P8	TYPE1		P36	TYPE2	
IN	A1$_4$	67	OUT	B2$_4$	40	IN	B1$_4$	31	OUT	A2$_4$	4
P47	TYPE1		P19	TYPE2		P10	TYPE1		P38	TYPE2	
IN	A1$_5$	66	OUT	B2$_3$	41	IN	B1$_5$	30	OUT	A2$_3$	5
P46	TYPE1		P18	TYPE2		P11	TYPE1		P39	TYPE2	
IN	A1$_6$	65	OUT	B2$_2$	42	IN	B1$_6$	29	OUT	A2$_2$	6
P44	TYPE1		P16	TYPE2		P13	TYPE1		P41	TYPE2	
IN	A1$_7$	64	OUT	B2$_1$	43	IN	B1$_7$	28	OUT	A2$_1$	7
P43	TYPE1		P15	TYPE2		P14	TYPE1		P42	TYPE2	
IN	A1$_8$	63	OUT	B2$_0$	44	IN	B1$_8$	27	OUT	A2$_0$	8
P42	TYPE1		P14	TYPE2		P15	TYPE1		P43	TYPE2	
IN	A2$_0$	62	OUT	B1$_8$	45	IN	B2$_0$	26	OUT	A1$_8$	9
P41	TYPE1		P13	TYPE2		P16	TYPE1		P44	TYPE2	
IN	A2$_1$	61	OUT	B1$_7$	46	IN	B2$_1$	25	OUT	A1$_7$	10
P39	TYPE1		P11	TYPE2		P18	TYPE1		P46	TYPE2	
IN	A2$_2$	60	OUT	B1$_6$	47	IN	B2$_2$	24	OUT	A1$_6$	11
P38	TYPE1		P10	TYPE2		P19	TYPE1		P47	TYPE2	
IN	A2$_3$	59	OUT	B1$_5$	48	IN	B2$_3$	23	OUT	A1$_5$	12
P36	TYPE1		P8	TYPE2		P21	TYPE1		P49	TYPE2	
IN	A2$_4$	58	OUT	B1$_4$	49	IN	B2$_4$	22	OUT	A1$_4$	13
P55	TYPE1		P7	TYPE2		P22	TYPE1		P50	TYPE2	
IN	A2$_5$	57	OUT	B1$_3$	50	IN	B2$_5$	21	OUT	A1$_3$	14
P33	TYPE1		P5	TYPE2		P24	TYPE1		P52	TYPE2	
IN	A2$_6$	56	OUT	B1$_2$	51	IN	B2$_6$	20	OUT	A1$_2$	15
P32	TYPE1		P4	TYPE2		P25	TYPE1		P53	TYPE2	
IN	A2$_7$	55	OUT	B1$_1$	52	IN	B2$_7$	19	OUT	A1$_1$	16
P30	TYPE1		P2	TYPE2		P27	TYPE1		P55	TYPE2	
IN	A2$_8$	54	OUT	B1$_0$	53	IN	B2$_8$	18	OUT	A1$_0$	17

DS010961-25

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE_1		Internal	TYPE2	
76	BOE_1		Internal	TYPE2	Control
75	DIR2	26	Input	TYPE1	Signals
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE_2		Internal	TYPE2	
72	BOE_2		Internal	TYPE2	
71	$A1_0$	55	Input	TYPE1	
70	$A1_1$	53	Input	TYPE1	
69	$A1_2$	52	Input	TYPE1	
68	$A1_3$	50	Input	TYPE1	
67	$A1_4$	49	Input	TYPE1	A1−in
66	$A1_5$	47	Input	TYPE1	
65	$A1_6$	46	Input	TYPE1	
64	$A1_7$	44	Input	TYPE1	
63	$A1_8$	43	Input	TYPE1	
62	$A2_0$	42	Input	TYPE1	
61	$A2_1$	41	Input	TYPE1	
60	$A2_2$	39	Input	TYPE1	
59	$A2_3$	38	Input	TYPE1	
58	$A2_4$	36	Input	TYPE1	A2−in
57	$A2_5$	35	Input	TYPE1	
56	$A2_6$	33	Input	TYPE1	
55	$A2_7$	32	Input	TYPE1	
54	$A2_8$	30	Input	TYPE1	
53	$B1_0$	2	Output	TYPE2	
52	$B1_1$	4	Output	TYPE2	
51	$B1_2$	5	Output	TYPE2	
50	$B1_3$	7	Output	TYPE2	
49	$B1_4$	8	Output	TYPE2	B1−out
48	$B1_5$	10	Output	TYPE2	
47	$B1_6$	11	Output	TYPE2	
46	$B1_7$	13	Output	TYPE2	
45	$B1_8$	14	Output	TYPE2	
44	$B2_0$	15	Output	TYPE2	
43	$B2_1$	16	Output	TYPE2	
42	$B2_2$	18	Output	TYPE2	
41	$B2_3$	19	Output	TYPE2	
40	$B2_4$	21	Output	TYPE2	B2−out
39	$B2_5$	22	Output	TYPE2	
38	$B2_6$	24	Output	TYPE2	
37	$B2_7$	25	Output	TYPE2	
36	$B2_8$	27	Output	TYPE2	

Description of Boundary-Scan Circuitry (Continued)

Boundary-Scan Register Definition Index (Continued)

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
35	$B1_0$	2	Input	TYPE1	
34	$B1_1$	4	Input	TYPE1	
33	$B1_2$	5	Input	TYPE1	
32	$B1_3$	7	Input	TYPE1	
31	$B1_4$	8	Input	TYPE1	B1–in
30	$B1_5$	10	Input	TYPE1	
29	$B1_6$	11	Input	TYPE1	
28	$B1_7$	13	Input	TYPE1	
27	$B1_8$	14	Input	TYPE1	
26	$B2_0$	15	Input	TYPE1	
25	$B2_1$	16	Input	TYPE1	
24	$B2_2$	18	Input	TYPE1	
23	$B2_3$	19	Input	TYPE1	
22	$B2_4$	21	Input	TYPE1	B2–in
21	$B2_5$	22	Input	TYPE1	
20	$B2_6$	24	Input	TYPE1	
19	$B2_7$	25	Input	TYPE1	
18	$B2_8$	27	Input	TYPE1	
17	$A1_0$	55	Output	TYPE2	
16	$A1_1$	53	Output	TYPE2	
15	$A1_2$	52	Output	TYPE2	
14	$A1_3$	50	Output	TYPE2	
13	$A1_4$	49	Output	TYPE2	A1–out
12	$A1_5$	47	Output	TYPE2	
11	$A1_6$	46	Output	TYPE2	
10	$A1_7$	44	Output	TYPE2	
9	$A1_8$	43	Output	TYPE2	
8	$A2_0$	42	Output	TYPE2	
7	$A2_1$	41	Output	TYPE2	
6	$A2_2$	39	Output	TYPE2	
5	$A2_3$	38	Output	TYPE2	
4	$A2_4$	36	Output	TYPE2	A2–out
3	$A2_5$	35	Output	TYPE2	
2	$A2_6$	33	Output	TYPE2	
1	$A2_7$	32	Output	TYPE2	
0	$A2_8$	30	Output	TYPE2	

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})   −0.5V to +7.0V
DC Input Diode Current (I_{IK})
  $V_I = -0.5V$ −20 mA
  $V_I = V_{CC} +0.5V$ +20 mA
DC Output Diode Current (I_{OK})
  $V_O = -0.5V$ −20 mA
  $V_O = V_{CC} +0.5V$ +20 mA
DC Output Voltage (V_O)   −0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)   ±70 mA
DC V_{CC} or Ground Current
  Per Output Pin   ±70 mA
Junction Temperature
  SSOP   +140°C
Storage Temperature   −65°C to +150°C
ESD (Min)   2000V

Recommended Operating Conditions

Supply Voltage (V_{CC})
  SCAN Products   4.5V to 5.5V
Input Voltage (V_I)   0V to V_{CC}
Output Voltage (V_O)   0V to V_{CC}
Operating Temperature (T_A)
  Commercial   −40°C to +85°C
  Military   −55°C to +125°C
Minimum Input Edge Rate dV/dt   125 mV/ns
  V_{IN} from 0.8V to 2.0V
  V_{CC} @ 4.5V, 5.5V

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of SCAN circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Commercial $T_A = +25°C$		Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High	4.5	1.5	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$
	Input Voltage	5.5	1.5	2.0	2.0	2.0		or $V_{CC} -0.1V$
V_{IL}	Maximum Low	4.5	1.5	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$
	Input Voltage	5.5	1.5	0.8	0.8	0.8		or $V_{CC} -0.1V$
V_{OH}	Minimum High	4.5		3.15	3.15	3.15	V	$I_{OUT} = -50 \mu A$
	Output Voltage	5.5		4.15	4.15	4.15		
		4.5		2.4		2.4	V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		2.4		2.4		$I_{OH} = -32$ mA
		4.5		2.4	2.4		V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		2.4	2.4			$I_{OH} = -24$ mA
V_{OL}	Maximum Low	4.5		0.1	0.1	0.1	V	$I_{OUT} = 50 \mu A$
	Output Voltage	5.5		0.1	0.1	0.1		
		4.5		0.55		0.55	V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		0.55		0.55		$I_{OL} = 64$ mA
		4.5		0.55	0.55		V	$V_{IN} = V_{IL}$ or V_{IH}
		5.5		0.55	0.55			$I_{OL} = 48$ mA
I_{IN}	Maximum Input Leakage Current	5.5	±0.1	±1.0	±1.0		μA	$V_I = V_{CC}$, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5	2.8	3.7	3.6		μA	$V_I = V_{CC}$
			−385	−385	−385		μA	$V_I = $ GND
	Minimum Input Leakage	5.5	−160	−160	−160		μA	$V_I = $ GND
I_{OLD}	Minimum Dynamic	5.5	94	63	94		mA	$V_{OLD} = 0.8V$ Max
I_{OHD}	Output Current (Note 3)		−40	−27	−40		mA	$V_{OHD} = 2.0V$ Min
I_{OZT}	Maximum I/O Leakage Current	5.5	±0.6	±11.0	±6.0		μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OS}	Output Short Circuit Current	5.5	−100	−100	−100		mA (min)	$V_O = 0V$

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_CC (V)	Commercial T_A = +25°C		Military T_A = −55°C to +125°C	Commercial T_A = −40°C to +85°C	Units	Conditions
			Typ		Guaranteed Limits			
I_CC	Maximum Quiescent Supply Current	5.5		16.0	168	88	μA	V_O = High TDI, TMS = V_{CC}
		5.5		750	930	820	μA	V_O = High TDI, TMS = GND
I_CCt	Maximum I_CC Per Input	5.5		2.0	2.0	2.0	mA	$V_I = V_{CC}-2.1V$
		5.5		2.15	2.15	2.15	mA	$V_I = V_{CC}-2.1V$ TDI/TMS Pin, test one with the other floating

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Noise Specifications

Symbol	Parameter	V_CC (V)	Commercial T_A = +25°C		Military T_A = −55°C to +125°C	Commercial T_A = −40°C to +85°C	Units
			Typ		Guaranteed Limits		
V_OLP	Maximum High Output Noise (Notes 5, 6)	5.0	1.0	1.5			V
V_OLV	Minimum Low Output Noise (Notes 5, 6)	5.0	−0.6	−1.2			V
V_OHP	Maximum Overshoot (Notes 4, 6)	5.0	$V_{OH}+1.0$	$V_{OH}+1.5$			V
V_OHV	Minimum V_CC Droop (Notes 4, 6)	5.0	$V_{OH}-1.0$	$V_{OH}-1.8$			V
V_IHD	Minimum High Dynamic Input (Notes 4, 7) Voltage Level	5.5	1.6	2.0	2.0	2.0	V
V_ILD	Maximum Low Dynamic Input (Notes 4, 7) Voltage Level	5.5	1.4	0.8	0.8	0.8	V

Note 4: Worst case package.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

Note 6: Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

Note 7: Maximum number of data inputs (n) switching. (n-1) input switching 0V to 3V. Input under test switching 3V to threshold (V_{ILD}).

AC Electrical Characteristics

Normal Operation

Symbol	Parameter	V_CC (V) (Note 9)	Commercial T_A = +25°C C_L = 50 pF			Military T_A=−55°C to +125°C C_L = 50 pF		Commercial T_A=−40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_PLH,	Propagation Delay	5.0	1.6		7.9	1.6	9.0	1.6	8.5	ns
t_PHL	A to B, B to A		1.6		7.9	1.6	9.3	1.6	8.8	

AC Electrical Characteristics (Continued)

Normal Operation

Symbol	Parameter	V_{CC} (V) (Note 9)	Commercial T_A = +25°C C_L = 50 pF			Military T_A=−55°C to +125°C C_L = 50 pF		Commercial T_A=−40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.2 1.2		8.6 8.5	1.2 1.2	10.0 9.5	1.2 1.2	9.5 9.0	ns
t_{PZL}, t_{PZH}	Enable Time	5.0	1.6 1.6		11.0 8.5	1.6 1.6	12.5 10.0	1.6 1.6	12.0 9.5	ns

AC Electrical Characteristics

Scan Test Operation

Symbol	Parameter	V_{CC} (V) (Note 9)	Commercial T_A = +25°C C_L = 50 pF			Military T_A=−55°C to +125°C C_L = 50 pF		Commercial T_A=−40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	2.8 2.8		13.2 13.2	2.8 2.8	15.8 15.8	2.8 2.8	14.5 14.5	ns
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.0 2.0		11.5 11.5	2.0 2.0	12.8 12.8	2.0 2.0	11.9 11.9	ns
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	2.4 2.4		14.5 14.5	2.4 2.4	16.7 16.7	2.4 2.4	15.8 15.8	ns
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		18.0 18.0	4.0 4.0	21.7 21.7	4.0 4.0	19.8 19.8	ns
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	4.0 4.0		18.6 18.6	4.0 4.0	21.2 21.2	4.0 4.0	20.2 20.2	ns
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	4.4 4.4		19.9 19.9	4.4 4.4	23.0 23.0	4.4 4.4	21.5 21.5	ns
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	3.2 3.2		16.4 16.4	3.2 3.2	19.6 19.6	3.2 3.2	18.2 18.2	ns
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	2.8 2.8		18.0 18.0	2.8 2.8	20.9 20.9	2.8 2.8	19.3 19.3	ns
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	2.8 2.8		18.4 18.4	2.8 2.8	21.8 21.8	2.8 2.8	20.0 20.0	ns
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0		18.9 18.9	4.0 4.0	22.6 22.6	4.0 4.0	20.9 20.9	ns

AC Electrical Characteristics (Continued)

Scan Test Operation

Symbol	Parameter	V_CC (V) (Note 9)	Commercial T_A = +25°C C_L = 50 pF			Military T_A=−55°C to +125°C C_L = 50 pF		Commercial T_A=−40°C to +85°C C_L = 50 pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	3.2 3.2		19.9 19.9	3.2 3.2	23.7 23.7	3.2 3.2	21.7 21.7	ns
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	3.6 3.6		21.3 21.3	3.6 3.6	24.9 24.9	3.6 3.6	23.3 23.3	ns

Note 8: All Propagation Delays involving TCK are measured from the falling edge of TCK.

AC Operating Requirements

Scan Test Operation

Symbol	Parameter	V_CC (V) (Note 9)	Commercial T_A = +25°C C_L = 50 pF	Military T_A = −55°C to +125°C C_L = 50 pF	Commercial T_A = −40°C to +85°C C_L = 50 pF	Units
			Guaranteed Minimum			
t_S	Setup Time, H or L Data to TCK (Note 10)	5.0	0.0	0.0	0.0	ns
t_H	Hold Time, H or L TCK to Data (Note 10)	5.0	6.5	7.5	6.5	ns
t_S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK (Note 11)	5.0	0.0	0.0	0.0	ns
t_H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$ (Note 11)	5.0	4.0	4.0	4.0	ns
t_S	Setup Time, H or L DIR1, DIR2 to TCK (Note 13)	5.0	0.0	0.0	0.0	ns
t_H	Hold Time, H or L TCK to DIR1, DIR2 (Note 13)	5.0	4.0	4.0	4.0	ns
t_S	Setup Time, H or L Internal AOE_n, BOE_n to TCK (Note 12)	5.0	1.0	1.0	1.0	ns
t_H	Hold Time, H or L TCK to Internal AOE_n, BOE_n (Note 12)	5.0	4.0	5.0	4.0	ns
t_S	Setup Time, H or L TMS to TCK	5.0	7.0	7.0	7.0	ns
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	2.0	2.0	ns
t_S	Setup Time, H or L TDI to TCK	5.0	1.0	1.0	1.0	ns
t_H	Hold Time, H or L TCK to TDI	5.0	3.5	4.5	3.5	ns

AC Operating Requirements (Continued)

Scan Test Operation

Symbol	Parameter		V_{CC} (V) (Note 9)	Commercial $T_A = +25°C$	Military $T_A = -55°C$ to $+125°C$	Commercial $T_A = -40°C$ to $+85°C$	Units
				C_L = 50 pF	C_L = 50 pF	C_L = 50 pF	
				Guaranteed Minimum			
t_W	Pulse Width		5.0				
		H		15.0	15.0	15.0	ns
		L		5.0	5.0	5.0	
f_{max}	Maximum TCK Clock Frequency		5.0	25	25	25	MHz
T_{PU}	Wait Time, Power Up to TCK		5.0	100	100	100	ns
T_{DN}	Power Down Delay		0.0	100	100	100	ms

Note 9: Voltage Range 5.0 is 5.0V ±0.5V.

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 10: Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0–8, 9–17, 18–26, 27–35, 36–44, 45–53, 54–62, 63–71).

Note 11: Timing pertains to BSR 74 and 78 only.

Note 12: Timing pertains to BSR 72, 73, 76 and 77 only.

Note 13: Timing pertains to BSR 75 and 79 only.

Extended AC Electrical Characteristics

Symbol	Parameter	T_A = Comm V_{CC} = Comm C_L = 50 pF 18 Outputs Switching (Note 15)			T_A = Mil V_{CC} = Mil C_L = 50 pF 18 Outputs Switching (Note 15)		T_A = Comm V_{CC} = Comm C_L = 250 pF (Note 16)		T_A = Mil V_{CC} = Mil C_L = 250 pF (Note 16)		Units
		Min	Typ	Max	Min	Max	Min	Max	Min	Max	
t_{PLH},	Propagation Delay	2.5		10.5	2.5	11.0	3.5	12.0	3.5	13.0	ns
t_{PHL}	Data to Output	2.5		10.5	2.5	11.0	3.5	13.5	3.5	14.5	
t_{PZH},	Output Enable Time	2.5		10.5	2.5	11.0	(Note 17)		(Note 17)		ns
t_{PZL}		2.5		13.5	2.5	14.0					
t_{PHZ},	Output Disable Time	2.0		9.5	2.0	10.0	(Note 18)		(Note 18)		ns
t_{PLZ}		2.0		10.0	2.0	10.5					
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output		0.5	1.0				1.0			ns
t_{OSLH} (Note 14)	Pin to Pin Skew LH data to Output		0.5	1.0				1.0			ns

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW.

Note 15: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 16: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 17: 3-STATE delays are load dominated and have been excluded from the datasheet.

Note 18: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	20	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	41	pF	$V_{CC} = 5.0V$

Pad Diagram

DS010961-24
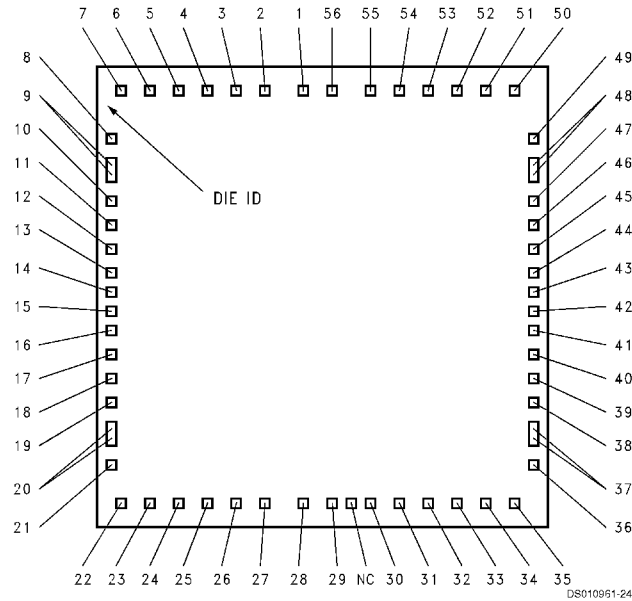
SCAN18245T Die Information

Die Revision	Z
Die ID	Y8J245
Die Size (X)	4310 µm
Die Size (Y)	4310 µm
Die Thickness	14 mil
Substrate Bias	V_{CC} (optional)
Backside Coating	None

Pad Locations

Signal Number	Signal Name	Pad Location (Note 19)
1	TMS	−8.58, 77.81
2	$B1_0$	−19.94, 77.81
3	DIR1	−30.50, 77.81
4	$B1_1$	−40.98, 77.81
5	$B1_2$	−53.59, 77.81
6	GND	−63.73, 77.81
7	$B1_3$	−74.47, 77.81
8	$B1_4$	−79.73, 62.30
9	V_{CC}	−79.73, 51.55
		−79.73, 46.28
10	$B1_5$	−79.73, 36.05
11	$B1_6$	−79.73, 27.48
12	GND	−79.72, 19.46
13	$B1_7$	−79.73, 10.09
14	$B1_8$	−79.73, 3.46
15	$B2_0$	−79.73, −3.43
16	$B2_1$	−79.73, −10.06
17	GND	−79.72, −19.43
18	$B2_2$	−79.73, −27.45
19	$B2_3$	−79.73, −36.02
20	V_{CC}	−79.73, −46.24
		−79.73, −51.52
21	$B2_4$	−79.73, −62.27
22	$B2_5$	−74.47, −77.81
23	GND	−63.73, −77.81
24	$B2_6$	−53.59, −77.81
25	$B2_7$	−40.98, −77.81
26	DIR2	−30.50, −77.81
27	$B2_8$	−19.94, −77.81
28	TDO	−8.58, −77.81
29	TCK	5.54, −77.81
30	$A2_8$	19.94, −77.81
31	$\overline{G2}$	30.50, −77.81
32	$A2_7$	40.98, −77.81
33	$A2_6$	53.59, −77.81
34	GND	63.73, −77.81
35	$A2_5$	74.47, −77.81
36	$A2_4$	79.73, −62.27

Pad Locations (Continued)

Signal Number	Signal Name	Pad Location (Note 19)
37	V_{CC}	79.73, −51.50
		79.73, −46.23
38	$A2_3$	79.73, −36.02
39	$A2_2$	79.73, −27.40
40	GND	79.73, −19.43
41	$A2_1$	79.73, −10.06
42	$A2_0$	79.73, −3.43
43	$A1_8$	79.73, 3.46
44	$A1_7$	79.73, 10.09
45	GND	79.72, 19.46
46	$A1_6$	79.73, 27.43
47	$A1_5$	79.73, 36.05
48	V_{CC}	79.73, 46.26
		79.73, 51.54
49	$A1_4$	79.73, 62.30
50	$A1_3$	74.47, 77.81
51	GND	63.73, 77.81
52	$A1_2$	53.59, 77.81
53	$A1_1$	40.98, 77.81
54	$\overline{G1}$	30.50, 77.81
55	$A1_0$	19.94, 77.81
56	TDI	5.54, 77.81

Note 19: X, Y coordinates measured in mils from center of die.
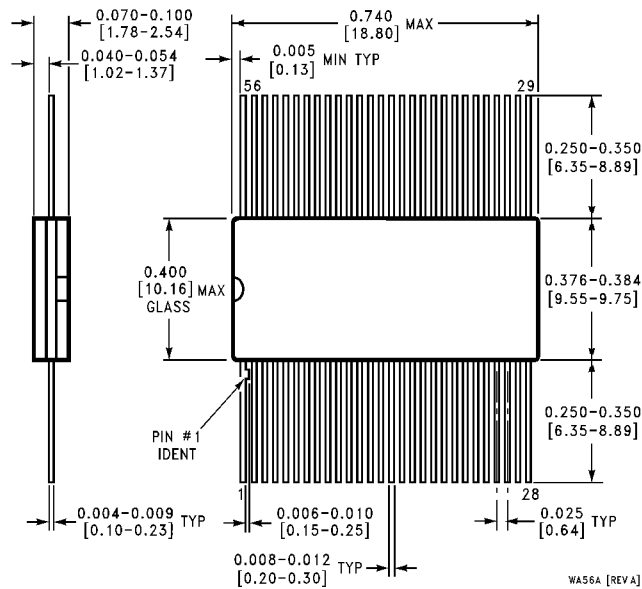
Ordering Information Scan Series

SCAN 18 245 T SS C X

Serially Controlled Access Network

18-Bit Logic

Function Type

Technology Designator
   T = TTL Input TTL Output CMOS Device
   C = CMOS Input/Output CMOS Device
   B = Bipolar TTL Device
   E = ECL Device
   A = BiCMOS Device
   F = TTL Input/CMOS Output CMOS Device

Special Variations
   X = Tape and Reel
   QB = Military grade device with environmental and burn-in processing.

Temperature Range
   C = Commercial (−40°C to +85°C)
   M = Military (−55°C to +125°C)

Package Code
   SS = 25 mil Pitch (JEDEC) SSOP
   F = 25 mil Pitch Ceramic Flatpak

DS010961-26

Physical Dimensions inches (millimeters) unless otherwise noted

0.720 – 0.730
[18.30 – 18.54]
- A -

56   29

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

⊕ 0.010 [0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]

- B -

1   28

0.020 ±0.003
[0.51 ±0.08] TYP

0.025
[0.635] TYP

0.008 – 0.012
[0.21 – 0.30] TYP

⊕ 0.0031 [0.08] Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE
0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

- D -
- C -

0.025
[0.635] TYP

0.010
[0.25] MIN TYP

0° – 8° TYP

△ 0.004 [0.10]

MS56A (REV E)
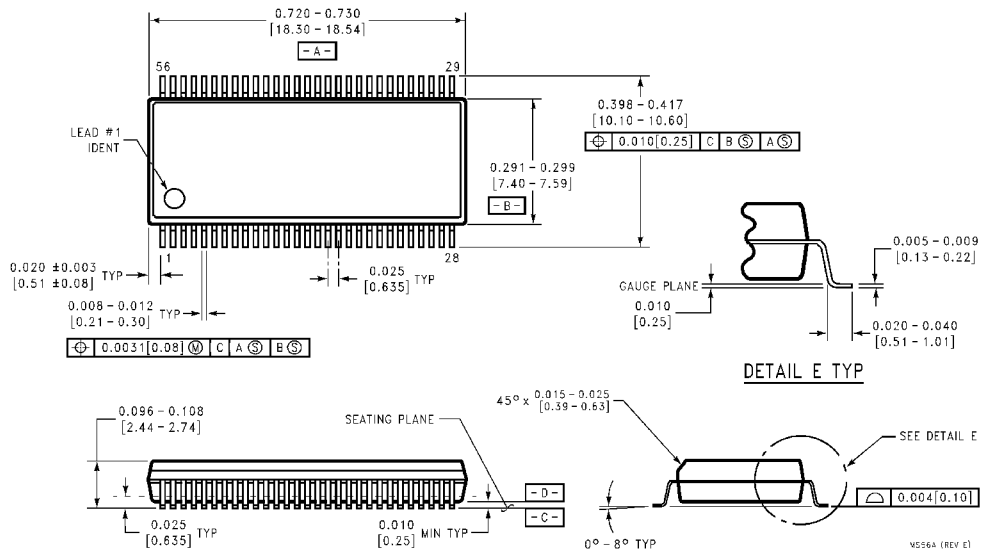
56-Lead SSOP (0.300" Wide) (SS)
Package Number MS56A

0.070 – 0.100
[1.78 – 2.54]

0.740
[18.80] MAX

0.040 – 0.054
[1.02 – 1.37]

0.005
[0.13] MIN TYP

56   29

0.250 – 0.350
[6.35 – 8.89]

0.400
[10.16] MAX
GLASS

0.376 – 0.384
[9.55 – 9.75]

0.250 – 0.350
[6.35 – 8.89]

PIN #1
IDENT

1   28

0.004 – 0.009
[0.10 – 0.23] TYP

0.006 – 0.010
[0.15 – 0.25]

0.025
[0.64] TYP

0.008 – 0.012
[0.20 – 0.30] TYP

WA56A [REV A]

56-Lead Ceramic Flatpak (F)
Package Number WA56A

SCAN18245T Non-Inverting Transceiver with 3-STATE Outputs

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DE-
VICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMI-
CONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or sys-
tems which, (a) are intended for surgical implant into
the body, or (b) support or sustain life, and (c) whose
failure to perform when properly used in accordance
with instructions for use provided in the labeling, can
be reasonably expected to result in a significant injury
to the user.

2. A critical component in any component of a life support
device or system whose failure to perform can be rea-
sonably expected to cause the failure of the life support
device or system, or to affect its safety or effectiveness.