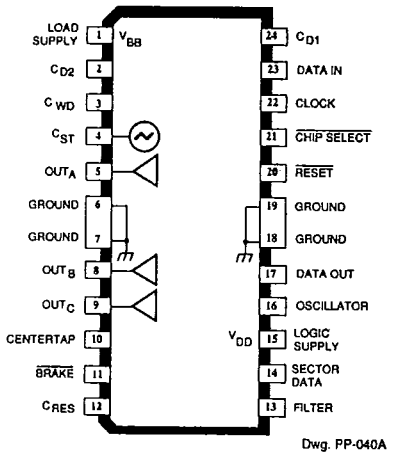
8902 AND 8903

T-52-13-25

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING



Dwg. PP-040A

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB}
- A8902SLB ..... V_{DD} + 1.0 V
- A8903SLB ..... 14 V

Output Current, I_{OUT} (peak) ..... ±1.5 A
- (continuous) ..... ±1.1 A

Logic Input Voltage Range, V_{IN} ..... -0.3 V to V_{DD} + 0.3 V

Logic Supply Voltage, V_{DD} ..... 6.0 V

Package Power Dissipation, P_D ..... See Graph

Operating Temperature Range, T_A ..... -20°C to +85°C

Junction Temperature, T_J ..... +150°C†

Storage Temperature Range, T_S ..... -55°C to +150°C

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The A8902SLB and A8903SLB are three-phase DMOS back-EMF sensing spindle motor drivers for use in 5 V and 12 V Winchester disc drives, respectively. The power output stages are capable of ±1 A output currents and have 1 Ω (total resistance, typical) DMOS power outputs for low power dissipation. Intrinsic ground clamp and flyback diodes are provided for driving inductive loads. Thermal shutdown circuitry is provided to protect the devices from excessive junction temperature.

Internal logic and analog detection circuitry provide complete sequencing of the outputs during start-up and run modes without the need for external Hall-effect position-sensing devices. Internal linear control of the output current is used to provide frequency-locked loop speed control. A serial port allows the user flexibility in programming the reference frequency count number which determines motor speed. Additionally, the serial port provides user programmability of maximum start-up current levels, a sleep mode, and system diagnostics.

Both devices are provided in 24-lead wide-body, small-outline plastic power packages (SOICs) for surface-mount applications. The copper batwing provides for maximum package power dissipation in the smallest possible construction.

FEATURES

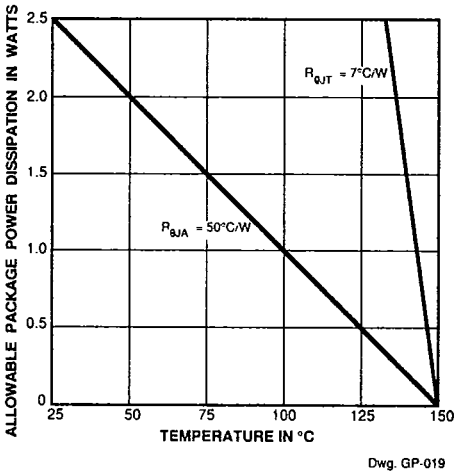
- DMOS Outputs
- Low $r_{DS(on)}$ - 1 Ω Typical Total
- Back-EMF Commutation Circuitry
- Frequency-Locked Loop Speed Control
- Sector Data Tachometer Signal Input
- Programmable Start-Up Current
- Diagnostics Mode
- Sleep Mode
- Linear Current Control
- Dynamic Braking With Delay
- System Diagnostics Data Out
- Internal Thermal Shutdown Circuitry
- Power Surface-Mount Package

Always order by complete part number:

A8902SLB	5 Volt Drive
A8903SLB	12 Volt Drive

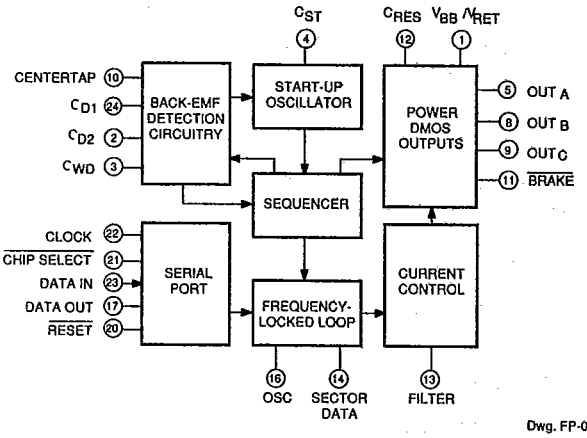
8902 AND 8903
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING

T-52-13-25



Dwg. GP-019

FUNCTIONAL BLOCK DIAGRAM



Dwg. FP-022A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V, V_{BB} = 5.0 V (A8902SLB) or 12 V (A8903SLB)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Supply Current	I_{DD}	Operating	—	7.5	10	mA
		Sleep Mode	—	—	500	µA
Load Supply Voltage	V_{BB}	A8902SLB, Operating	—	5.0	6.0	V
		A8903SLB, Operating	—	12	14	V
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	A8902SLB, V_{OUT} = 6.0 V	—	100	300	µA
		A8903SLB, V_{OUT} = 14 V	—	100	300	µA
		V_{OUT} = 0 V	—	-100	-300	µA
Total Output ON Resistance (Source + Sink + R_S)	$r_{DS(on)}$	I_{OUT} = 900 MA, Pulse Test	—	1.1	1.4	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	A8902SLB, I_{OUT} = 900 mA, L = 3 mH	7.0	—	—	V
		A8903SLB, I_{OUT} = 900 mA, L = 3 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.25	1.5	V

Continued next page...

8902 AND 8903
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING

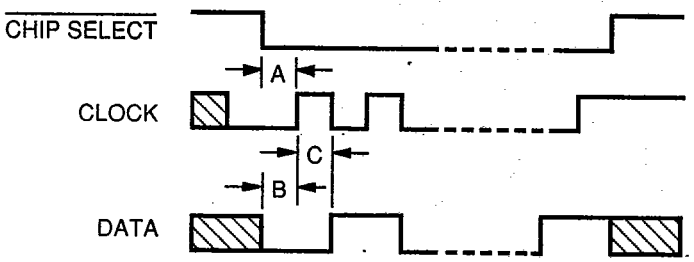
T-52-13-25

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	DATA, RESET, CLK, CHIP SELECT	-0.3	—	1.5	V
	$V_{IN(1)}$	DATA, RESET, CLK, CHIP SELECT	3.5	—	5.3	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	1.0	µA
DATA Output Voltage	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -500 µA	3.5	—	—	V
C_{ST} Current	I_{CST}	Charging	16	20	24	µA
		Discharging	-16	-20	-24	µA
Filter Current	I_{FILTER}	Charging	8.0	10	12	µA
		Discharging	-8.0	-10	-12	µA
C_D Current (CD_1 or C_{D2})	I_{CD}	Charging	16	20	24	µA
		Discharging	-35	-44	-53	µA
C_D Current Matching	—	$I_{CD(DISCHRG)}/I_{CD(CHRG)}$	2.1	2.2	2.3	—
C_{WD} Current	I_{CWD}	Charging	16	20	24	µA
C_{WD} Trip Voltage	V_{TL}		0.45	0.50	0.55	V
	V_{TH}		2.25	2.50	2.75	V
Clock Frequency	f_{CLK}		3.3	—	—	MHz
FLL Oscillator Frequency	f_{OSC}		—	>10	—	MHz
I_{OUT}(MAX) Accuracy	—		—	±10	—	%
Transconductance Gain	g_m		0.45	0.50	0.55	A/V
Centertap Resistors	R_{CT}		8.0	10	12	kΩ

8902 AND 8903 3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING

T-52-13-25



Dwg. WP-014-1

SERIAL PORT TIMING CONDITIONS

A. Minimum CHIP SELECT setup time before CLOCK rising edge ..... **150 ns**
B. Minimum DATA setup time before CLOCK rising edge ..... **150 ns**
C. Minimum DATA hold time before CLOCK falling edge ..... **150 ns** .

FUNCTIONAL DESCRIPTION

Power Outputs. The power outputs of the A8902/03SLB are DMOS transistors with a total source plus sink $r_{DS(on)}$ of typically 1.1 Ω. Intrinsic ground clamp and flyback diodes clamp transient voltage spikes when switching inductive loads. Internal charge-pump circuitry is used to drive the gates of the N-channel source drivers to their required gate voltages. The truth table for the output drivers sequencing is:

SEQUENCER STATE	OUT_A	OUT_B	OUT_C
1	High	Low	Z
2	Z	Low	High
3	Low	Z	High
4	Low	High	Z
5	Z	High	Low
6	High	Z	Low

Braking. Dynamic braking of the motor, where all source drivers are turned OFF and all sink drivers are turned ON, is achieved by activating the BRAKE input or through the serial port - DATA IN. During power-down conditions, the external charge-pump storage capacitor is used to provide power to turn ON the three sink drivers which, due to their inherent capacitive input, will remain activated until the device is reset.

8902 AND 8903 3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING

T-52-13-25

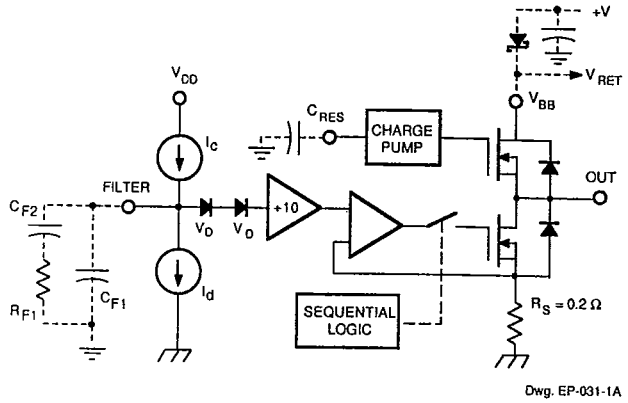


FIGURE 1

An external resistor/capacitor can be utilized in conjunction with the BRAKE input to provide a delay on braking (100 ms max.) during power down to ensure retraction of the voice coil head before spindle-motor braking is activated.

Current Control. The A8902SLB and A8903SLB provide linear current control of the sink drivers during start-up and running modes. In the start-up mode, the maximum load current can be programmed via the serial port (see Serial Port). During the running mode, the output current is linearly controlled for low noise in frequency-locked speed-control systems. Current control is achieved by monitoring the load current with an internal sense resistor (R_S). The voltage across the sense resistor is compared to one-tenth the voltage at the FILTER terminal less two diode drops, generating an error voltage to drive the gate of the appropriate output sink transistor. This creates a load current that is proportional to the voltage at the FILTER terminal less two diode drops. This transconductance function is $I_{OUT} = (V_{FILTER} - 2V_D)/10R_S$, where R_S is approximately 0.2 Ω and V_D is approximately 0.7 V.

Speed Control. The A8902/03SLB include a frequency-locked loop speed control system. This system operates by generating motor speed (TACH) and desired speed reference (REF) signals which are compared to provide a speed error signal, which is then used to turn ON current sources I_c and I_d, to charge or discharge a lead/lag loop filter compensation network at the FILTER terminal.

The circuitry implementing the speed control loop is shown in Figure 2. The operation of this circuit is as follows: the FCOM signal is a logic signal that changes state every time the A8902/03SLB detects a back-EMF zero crossing. By dividing the FCOM signal by three times the number of poles in the motor, a TACH signal is developed that changes state every mechanical revolution. This is done to develop a low-jitter tachometer signal.

The derived TACH signal is compared to the desired time (REF) for one revolution. This is done by using the positive-going edge of the TACH signal to trigger a latch that enables a programmable counter. The counter, driven by an accurate external oscillator signal, counts the desired number of oscillator cycles in a single revolution. The desired number of oscillator cycles is programmed via the serial port DATA IN.

$$\text{desired total count} = \frac{120 \times f_{osc}}{\text{desired motor speed.(rpm)}}$$

When the counter reaches its desired number, the latch is reset and the REF signal goes low (see Figure 2). The TACH and REF signals are fed to the switchable current sources to charge and discharge the loop compensation network at the FILTER terminal. If the TACH signal goes low before REF an Error-Fast signal turns ON I_d lowering the current in the motor and thereby reducing its speed. If the REF signal goes low before TACH an Error-Slow signal turns ON I_c which

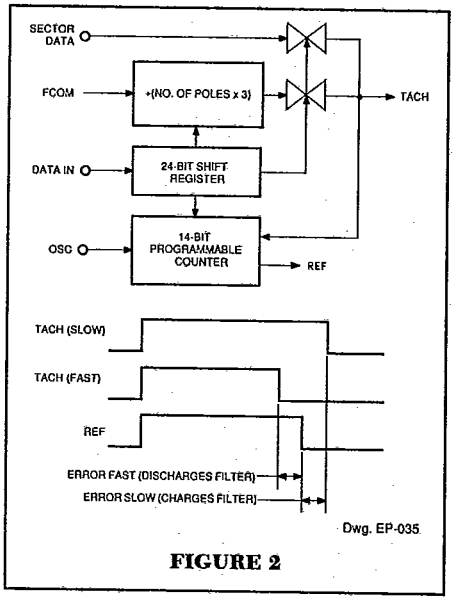


FIGURE 2

8902 AND 8903 3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING

T-52-13-25

increases the load current and thereby the speed of the motor. The loop filter components are used to dampen the response of the loop and achieve optimal settling time.

Response time to disturbances in speed can be improved by synchronizing to sector data once information is being read from the disc. This change can be made by changing the count number in the programmable counter (see Serial Port) and switching TACH to a sector tachometer signal. This should be done when TACH and REF are in the low state so as not to generate an erroneous error signal. This can be achieved by programming the serial port to provide the SYNC signal (high) on the DATA OUT terminal which will indicate exact timing for the switch to sector data.

Start-Up and Back-EMF Commutation Circuitry. The A8902/03SLB provide sensorless operation of three-phase bipolar brushless dc motors. This is done by randomly energizing one of the six output commutation states to start the motor moving. The motor's back-EMF is then quickly examined to determine if the motor is moving in the correct direction and if the drivers are in their correct output states. If they are not, the output drivers are advanced to the next state in the output sequence and the process repeats itself. If the motor is synchronized to the correct output commutation state, and moving in the right direction, the back-EMF circuitry disables the start-up circuitry and continues to commutate the motor off the back-EMF signals in the windings.

Serial Port - DATA IN. The serial port functions to write various operational and diagnostic modes to the A8902/03SLB. The serial port DATA IN is enabled/disabled by the CHIP SELECT input. When CHIP SELECT is high the serial port is disabled and the chip is not affected by changes in data at the DATA IN or CLOCK inputs.

To write data to the serial port, the CLOCK input should be low prior to the CHIP SELECT input going low. Once CHIP SELECT goes low, information on the DATA IN terminal is read into the shift register on the positive-going transition of the CLOCK. There are 23 bits in the serial input port. Their functions are:

D0 - Sleep/Run Mode; LOW = Sleep, HIGH = Run
This bit allows the device to be powered down when not in use.

D1 - Step Mode; LOW = Normal Operation, HIGH = Step Only
When in the step-only mode the back-EMF detection circuitry is disabled and the power outputs are stepped through their normal commutation sequence by the start-up oscillator. This mode is intended to facilitate device and system testing.

D2 - Brake; LOW = Run, HIGH = Brake.

D3 and D4 - These two bits set the maximum output current:

D4	D5	I_{OUT}(MAX)
0	0	1 A
0	1	800 mA
1	0	600 mA
1	1	400 mA

D5 thru D18 - This 14-bit word programs the REF time to set desired motor speed. The user provides the OSC input for the master clock to the 18-bit counter.

Bit Number	Count Number
D5	16
D6	32
D7	64
D8	128
D9	256
D10	512
D11	1 024
D12	2 048
D13	4 096
D14	8 192
D15	16 384
D16	32 768
D17	65 536
D18	131 072

D19 - This bit sets the frequency-locked loop synchronization;

LOW = Internal once-around speed signal, HIGH = External sector data.

8902 AND 8903 3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVERS WITH BACK-EMF SENSING

T-52-13-25

D20 and D21 - These bits program the number of motor poles for the once-around FCOM counter:

D20	D21	Motor Poles
0	0	8
0	1	—
1	0	16
1	1	12

D22 and D23 - Controls the multiplexor for DATA OUT:

D22	D23	DATA OUT
0	0	Tach. (once around or sector)
0	1	Thermal Shutdown
1	0	Sync. (tach.-sector switch)
1	1	FCOM

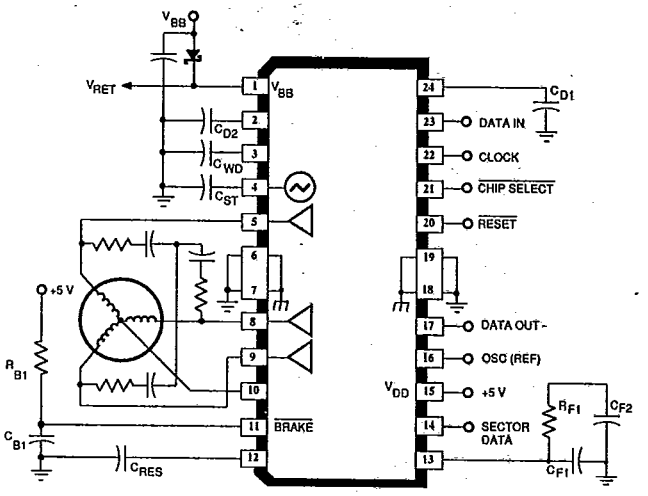
Data written into the serial port is latched and becomes active upon the low-to-high transition of the CHIP SELECT input at the end of the write cycle. D0 will be the last bit written to the serial port.

Reset. The RESET terminal when pulled low clears all serial port bits, including the DO latch which puts the A8902/03SLB in the sleep mode. When in the sleep mode, the FILTER terminal is pulled high to allow the output drivers to fully saturate at startup.

Centertap. The A8902/03SLB internally simulate the centertap voltage of the motor. To obtain reliable start-up performance from motor to motor, the motor centertap should be connected to this terminal.

External Component Selection. Applications information regarding the selection of external component values is available.

TYPICAL APPLICATION



Dwg. EP-036A