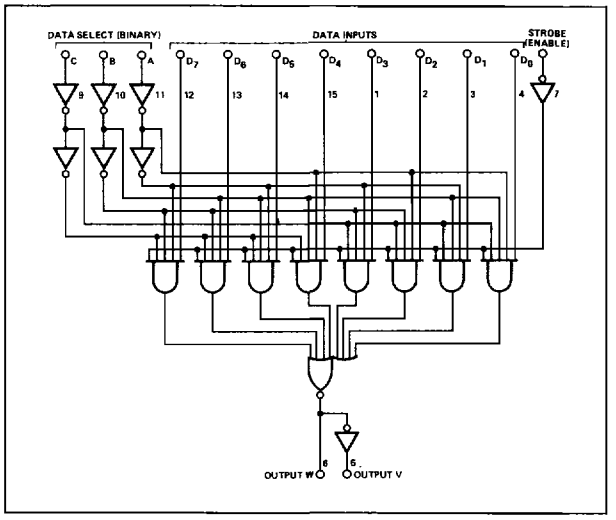
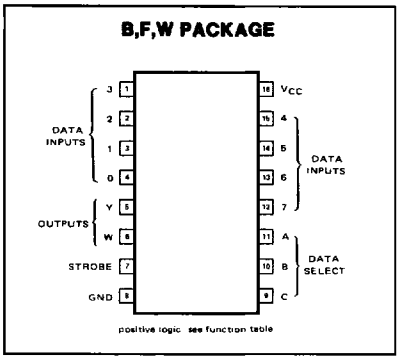
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant

D0, D1 . . . D7 = the level of the D respective input

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time													
t_{PLH}	Low-to-high	A,B,C (4 levels)	Y		35	52		27	43		12	18	ns
t_{PHL}	High-to-low				20	30		31	50		12	18	
t_{PLH}	Low-to-high	A,B,C,D (3 levels)	W		23	35							
t_{PHL}	High-to-low				22	33							
t_{PLH}	Low-to-high	A,B,C (3 levels)	W					24	39		10	15	
t_{PHL}	High-to-low							20	32		9	13.5	
t_{PLH}	Low-to-high	Strobe	Y		35	52		23	37		11	16.5	
t_{PHL}	High-to-low				19	30		25	42		12	18	
t_{PLH}	Low-to-high	Strobe	W		15.5	24		19	31		9	13	
t_{PHL}	High-to-low				21	30		16	26		8.5	12	
t_{PLH}	Low-to-high	D_0—D_7	Y		19	29							
t_{PHL}	High-to-low				16	24							
t_{PLH}	Low-to-high	E_0—E_{15}	W		13	20							
t_{PHL}	High-to-low				8.5	14							
t_{PLH}	Low-to-high	Any D	Y					16	26		8	12	
t_{PHL}	High-to-low							20	32		8	12	
t_{PLH}	Low-to-high	Any D	W					13	21		4.5	7	
t_{PHL}	High-to-low							9	15		4.5	7	

Load circuit and typical waveforms are shown at the front of section.

LOGIC

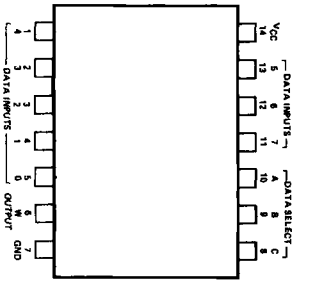
8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER 54/74152

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

PIN CONFIGURATION

W PACKAGE

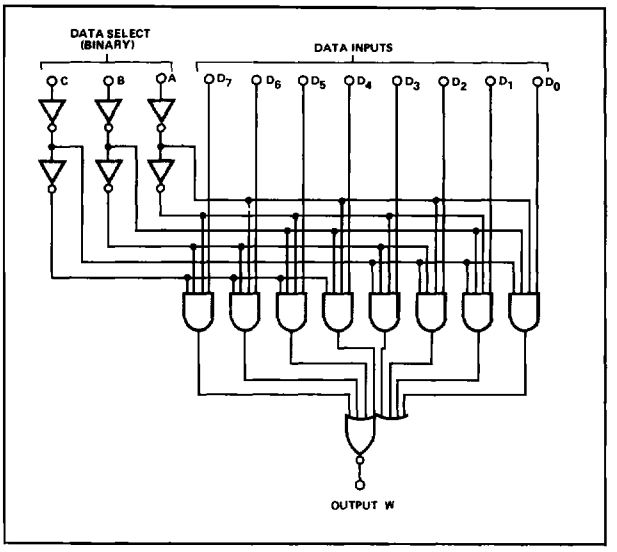


TRUTH TABLE

INPUTS											OUTPUTS
C	B	A	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	W
X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	X	X	X	X	X	X	X	1
0	0	0	1	X	X	X	X	X	X	X	0
0	0	1	X	0	X	X	X	X	X	X	1
0	0	1	X	1	X	X	X	X	X	X	0
0	1	0	X	X	0	X	X	X	X	X	1
0	1	0	X	X	1	X	X	X	X	X	0
0	1	1	X	X	X	0	X	X	X	X	1
0	1	1	X	X	X	1	X	X	X	X	0
1	0	0	X	X	X	X	0	X	X	X	1
1	0	0	X	X	X	X	1	X	X	X	0
1	0	1	X	X	X	X	X	0	X	X	1
1	0	1	X	X	X	X	X	1	X	X	0
1	1	0	X	X	X	X	X	X	0	X	1
1	1	0	X	X	X	X	X	X	1	X	0
1	1	1	X	X	X	X	X	X	X	0	1
1	1	1	X	X	X	X	X	X	X	1	0

When used to indicate an input, X = Irrelevant.

LOGIC DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54 C_L = 15pF R_L = 400 Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time							
t_{PLH}	Low-to-high	A,B,C,D (3 levels)	W		23	35	ns
t_{PHL}	High-to-low				22	33	ns
t_{PLH}	Low-to-high	D_0-D_7	W		13	20	ns
T_{PHL}	High-to-low				8.5	14	ns

Load circuit and typical waveforms are shown at the front of section.