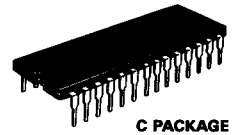
MCM6164
MCM61L64

8K x 8 Bit Fast Static Random Access Memory



C PACKAGE
CERAMIC
CASE 733

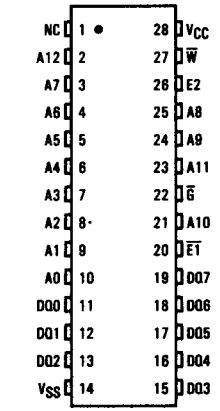
The MCM6164/MCM61L64 is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6164/MCM61L64 is available in a 600 mil, 28 pin ceramic dual-in-line package, with JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 45, 55 ns (Maximum)
- Low Power Dissipation — 495, 440 mW (Maximum, Active)
- Low Power/Data Retention Version (MCM61L64)
- Fully TTL Compatible
- Three State Data Outputs
- Also Available in Industrial Temperature Range (−40 to 85°C) as MCM6164C

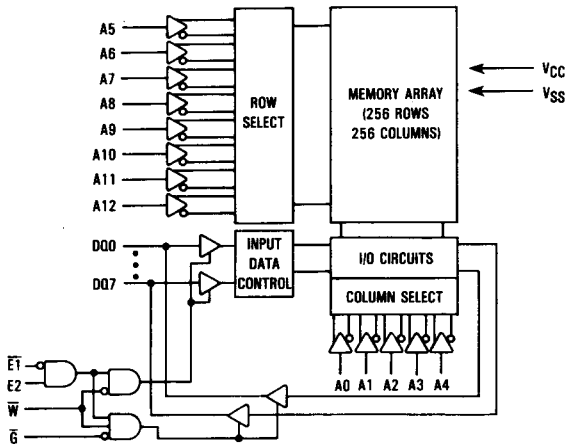
PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc, V_{IL} (min) = −3.0 V (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	<0.01	±1.0	μA
Power Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0)	t_{AVAV} = 45 ns	I_{CC}	–	50	90	mA
	t_{AVAV} = 55 ns		–	40	80	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	–	1.3	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V)	MCM6164	I_{SB2}	–	–	1.0	mA
	MCM61L64		–	5	50	μA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.15	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	3.0	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
Input/Output Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

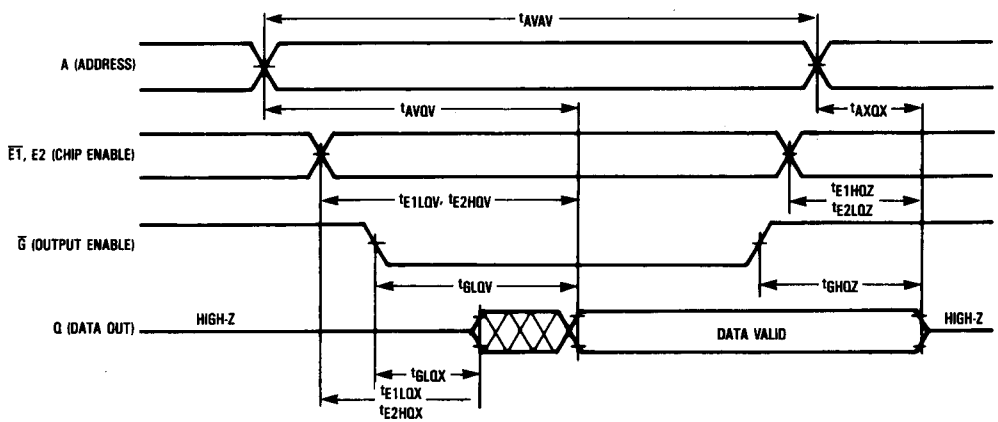
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . 0.8 V and 2.0 V
Output Load . . . . . Figure 1

READ CYCLE (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	—	55	—	ns	—
Address Cycle Time	t_{AVQV}	t_{AA}	—	45	—	55	ns	—
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	—	45	—	55	ns	—
E2 Access Time	t_{E2HQV}	t_{AC2}	—	45	—	55	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	20	—	25	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	—
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	—	5	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. Periodically sampled rather than 100% tested.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

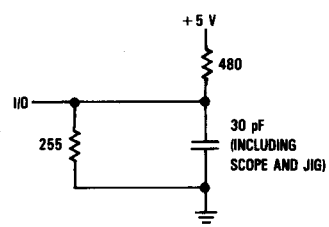
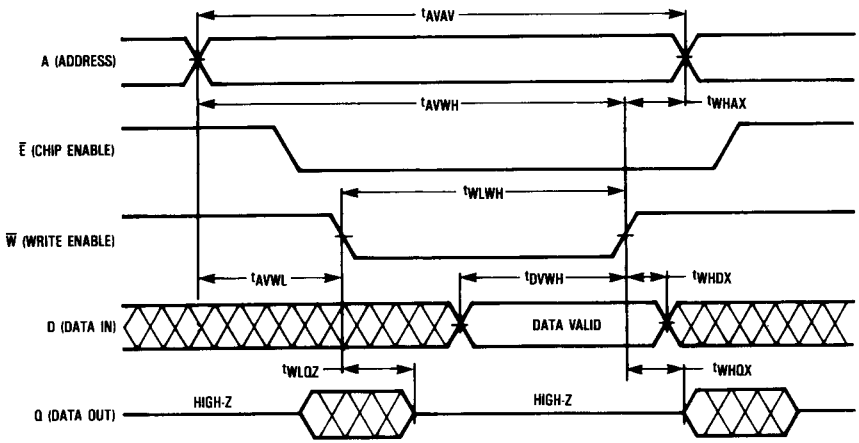


Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	–	55	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	40	–	50	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	25	–	30	–	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	20	–	25	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{OW}	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. Periodically sampled rather than 100% tested.



TYPICAL CHARACTERISTICS

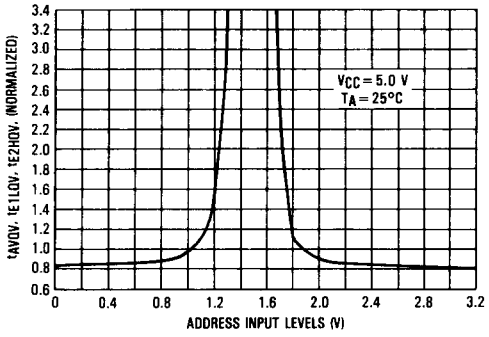
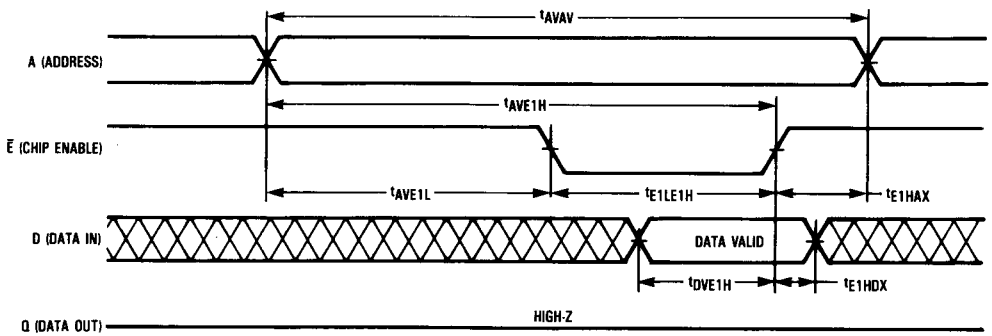


Figure 2. Access Time Versus Address Input Levels

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	–	55	–	ns	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVE1H}	t_{AW}	40	–	50	–	ns	–
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	40	–	50	–	ns	3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	20	–	25	–	ns	–
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	0	–	ns	4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	0	–	ns	–

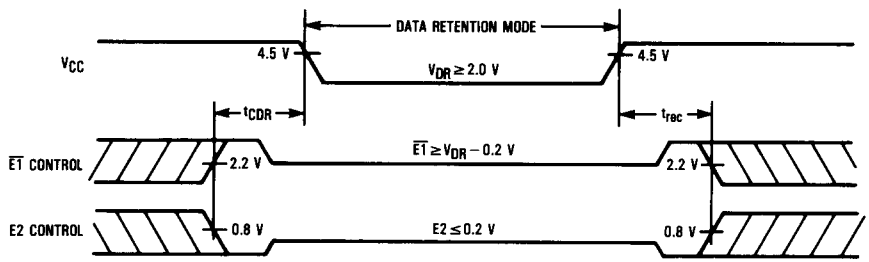
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.



LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C) (MCM61L64 Only)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ 0.2 V, $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V)	V_{DR}	2.0	1.0	7.0	V
Data Retention Current (V_{CC} = 3.0 V, $\overline{E1} \geq 2.8$ V or E2 ≤ 0.2 V, $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V)	I_{CCDR}	–	10	30	µA
Chip Disable to Data Retention Time (see waveform below)	t_{CDR}	0	–	–	ns
Operation Recovery Time (see waveform below)	t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time



TYPICAL CHARACTERISTICS
(Continued)

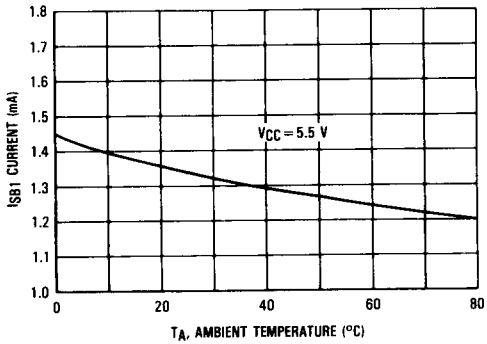


Figure 3. Standby Current Versus Temperature

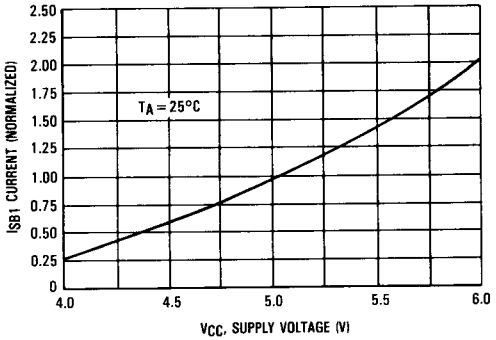


Figure 4. Standby Current Versus Supply Voltage

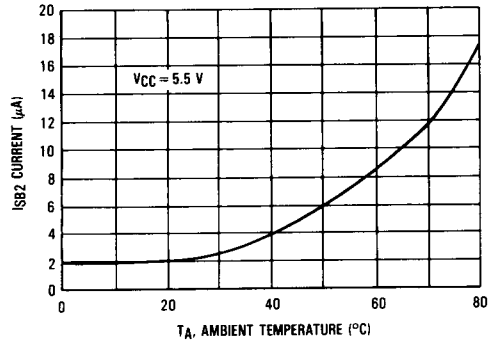


Figure 5. Standby Current Versus Temperature

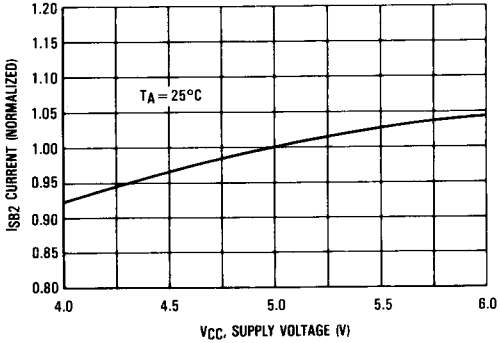


Figure 6. Standby Current Versus Supply Voltage

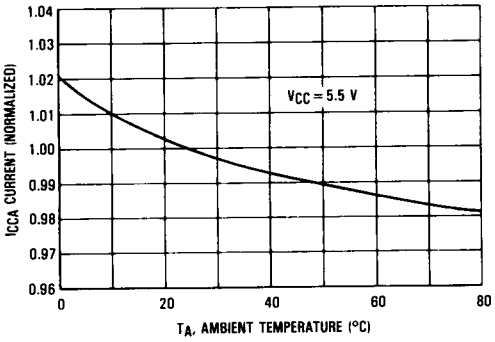


Figure 7. Supply Current Versus Temperature

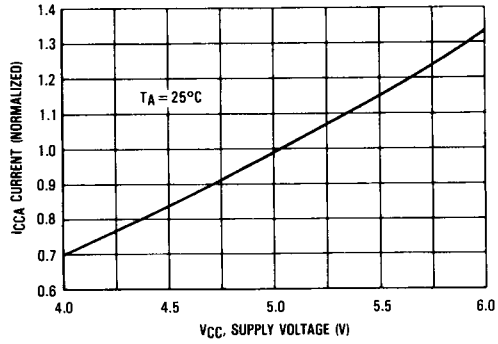


Figure 8. Supply Current Versus Supply Voltage

TYPICAL CHARACTERISTICS
(Continued)

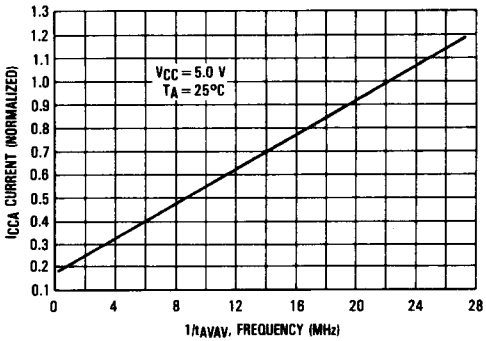


Figure 9. Supply Current Versus Frequency

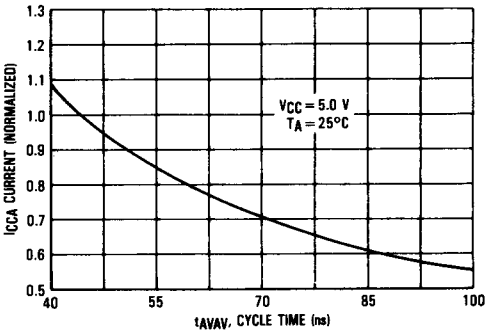


Figure 10. Supply Current Versus Cycle Time

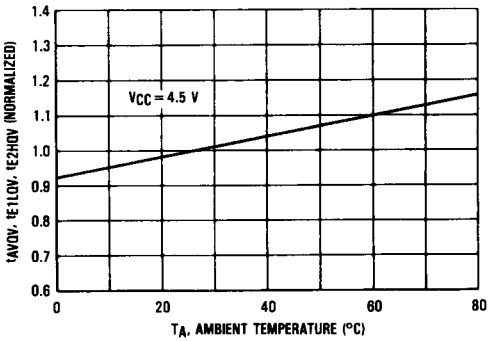


Figure 11. Access Time Versus Temperature

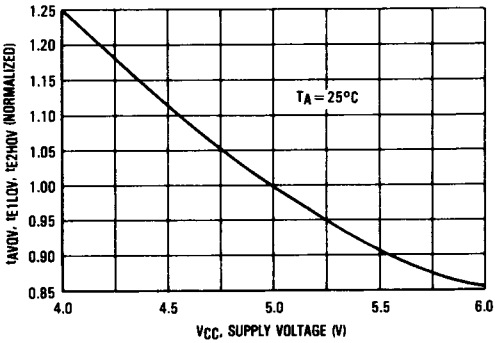


Figure 12. Access Time Versus Supply Voltage

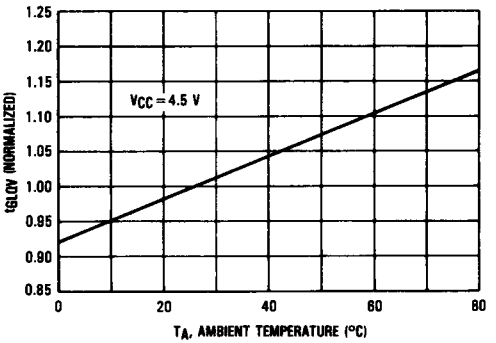


Figure 13. Access Time Versus Temperature

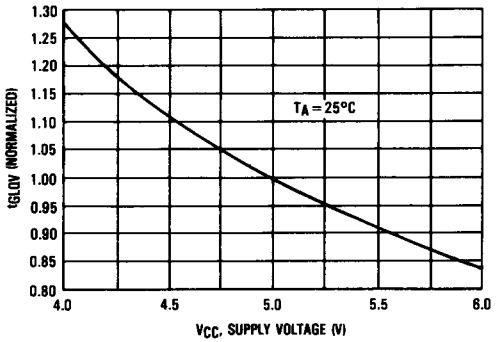
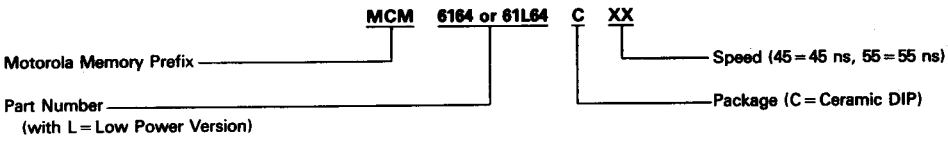


Figure 14. Access Time Versus Supply Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6164C45 MCM6164C55 MCM61L64C45 MCM61L64C55

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