FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-50102-2E

MCP (Multi-Chip Package) FLASH MEMORY

CMOS

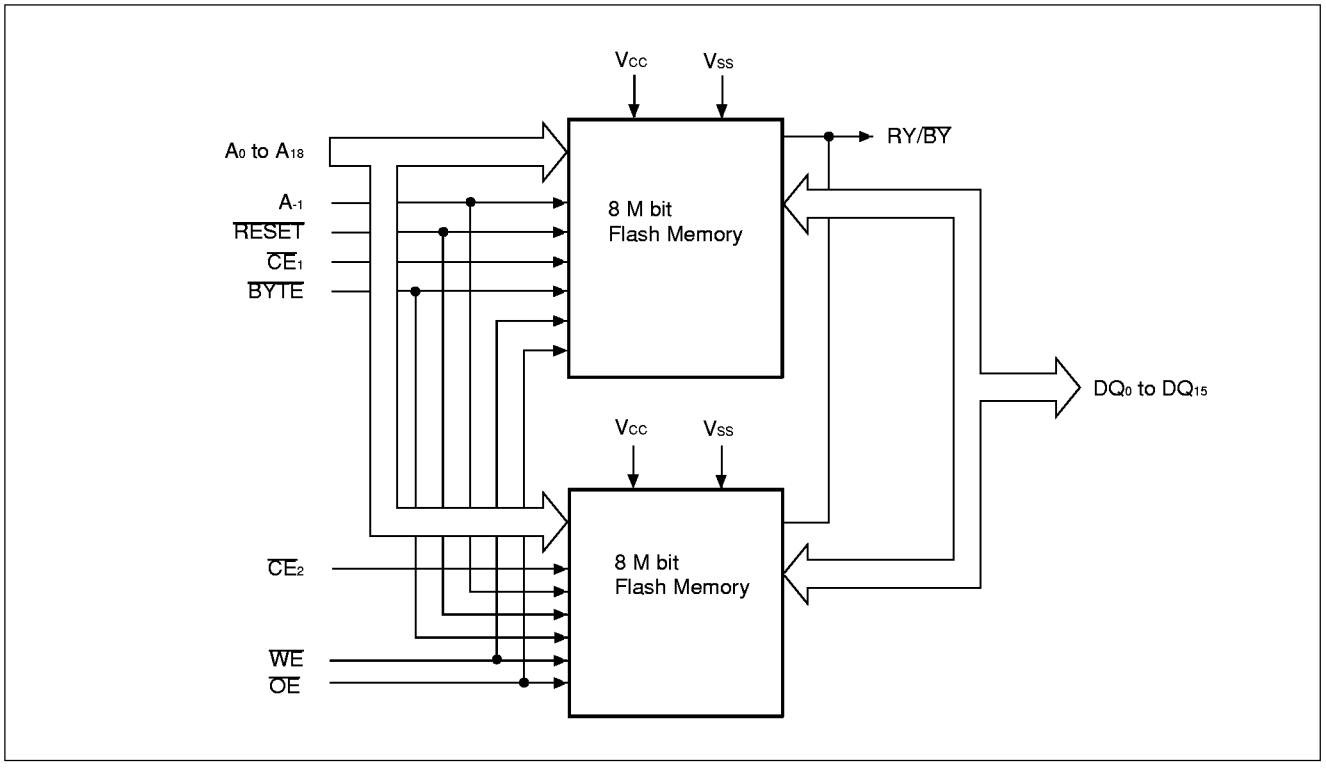
8M (× 8/× 16) FLASH MEMORY & 8M (× 8/× 16) FLASH MEMORY

MB84VB2000-10/MB84VB2001-10

■ FEATURES

- **Contain 2 chips of MBM29LV800A, and each chip have separate $\overline{CE}$.**
- **Power supply voltage of 2.7 to 3.6 V**
- **High performance**
  100 ns maximum access time
- **Operating Temperature**
  –40 to +85°C
- **Minimum 100,000 write/erase cycles**
- **Sector erase architecture**
  One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes × 2 chips
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  MB84VB2000: Top sector
  MB84VB2001: Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{Data}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{BY}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data in another sector within the same device
- **Please refer to "MBM29LV800TA/BA" data sheet in detailed function**

■ BLOCK DIAGRAM



■ CONNECTION DIAGRAM

(Top View)

	A	B	C	D	E	F	G	H
6	N.C.	V_{SS}	DQ_1	A_1	A_2	A_4	N.C.	A_9
5	A_{10}	DQ_5	DQ_2	A_0	A_3	A_7	RY/$\overline{BY}$	A_{14}
4	$\overline{OE}$	DQ_7	DQ_4	DQ_0	A_6	A_{18}	$\overline{RESET}$	A_{15}
3	A_{11}	A_8	A_5	DQ_8	DQ_3	DQ_{12}	A_{12}	$\overline{BYTE}$
2	A_{13}	A_{17}	$\overline{CE}_2$	$\overline{CE}_1$	DQ_{10}	V_{CC}	DQ_6	DQ_{15}/A_{-1}
1	$\overline{WE}$	N.C.	A_{16}	V_{SS}	DQ_9	DQ_{11}	DQ_{13}	DQ_{14}

Table 1 MB84VB2000/MB84VB2001 Pin Configuration

Pin	Function	Input/ Output
A_{-1}, A_0 to A_{18}	Address Inputs (Common)	I
DQ_0 to DQ_{15}	Data Inputs/Outputs (Common)	I/O
$\overline{CE}_1$	Chip Enable 1	I
$\overline{CE}_2$	Chip Enable 2	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RY/$\overline{BY}$	Ready/Busy Outputs (Common)	O
$\overline{RESET}$	Hardware Reset Pin/Sector Protection Unlock (Common)	I
$\overline{BYTE}$	Selects 8-bit or 16-bit mode (Common)	I
N.C.	No Internal Connection	—
V_{SS}	Device Ground (Common)	Power
V_{CC}	Device Power Supply (Common)	Power

■ PRODUCT LINE UP

Part No.		MB84VB2000/MB84VB2001
Ordering Part No.	V_{CC} = 3.0 V $^{+0.6\ V}_{-0.3\ V}$	-10
Max. Address Access Time (ns)		100
Max. $\overline{CE}$ Access Time (ns)		100
Max. $\overline{OE}$ Access Time (ns)		40

■ LOGIC SYMBOL

Table 2 MB84VB2000/MB84VB2001 User Bus Operations ($\overline{BYTE}$ = V_{IH})

Operation (5)	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_0 to DQ_{15}	$\overline{RESET}$
Auto-Select Manufacture's Code (1)	H	L	L	H	L	L	L	V_{ID}	Code	H
	L	H								
Auto-Select Device Code (1)	H	L	L	H	H	L	L	V_{ID}	Code	H
	L	H								
Read (3)	H	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
	L	H								
Full Standby	H	H	X	X	X	X	X	X	HIGH-Z	H
Output Disable	X	X	H	H	X	X	X	X	HIGH-Z	H
Write (Program/Erase)	H	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H
	L	H								
Enable Sector Protection (2), (4)	H	L	V_{ID}	⌐⌐	L	H	L	V_{ID}	X	H
	L	H								
Verify Sector Protection (2), (4)	H	L	L	H	L	H	L	V_{ID}	Code	H
	L	H								
Temporary Sector Unprotection	X	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)/Standby	X	X	X	X	X	X	X	X	HIGH-Z	L

Table 3 MB84VB2000/MB84VB2001 User Bus Operations ($\overline{BYTE}$ = V_{IL})

Operation (5)	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/A_{-1}	A_0	A_1	A_6	A_9	DQ_0 to DQ_7	$\overline{RESET}$
Auto-Select Manufacture's Code (1)	H	L	L	H	L	L	L	L	V_{ID}	Code	H
	L	H									
Auto-Select Device Code (1)	H	L	L	H	L	H	L	L	V_{ID}	Code	H
	L	H									
Read (3)	H	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H
	L	H									
Full Standby	H	H	X	X	X	X	X	X	X	HIGH-Z	H
Output Disable	X	X	H	H	X	X	X	X	X	HIGH-Z	H
Write (Program/Erase)	H	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H
	L	H									
Enable Sector Protection (2), (4)	H	L	V_{ID}	⌐⌐	L	L	H	L	V_{ID}	X	H
	L	H									
Verify Sector Protection (2), (4)	H	L	L	H	L	L	H	L	V_{ID}	Code	H
	L	H									
Temporary Sector Unprotection	X	X	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)/Standby	X	X	X	X	X	X	X	X	X	HIGH-Z	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⌐⌐ = Pulse input. See DC Characteristics for voltage levels.

Notes: 1.Manufacturer and device codes may also be accessed via a command register write sequence. See Table 7.

2.Refer to the section on Sector Protection.

3.$\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

4.V_{CC} = 3.3 V ±10%

5.Do not apply $\overline{CE}_1$ = $\overline{CE}_2$ = V_{IL} at a time.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16 K byte, two 8 K bytes, one 32 K byte, and fifteen 64 K bytes × 2.
- Individual-sector, multiple-sector, or bulk-erase capability.

	(×8)	(×16)
	FFFFFH	7FFFFH
16K byte/8K word	FC000H	7E000H
8K byte/4K word	FA000H	7D000H
8K byte/4K word	F8000H	7C000H
32K byte/16K word	F0000H	78000H
64K byte/32K word	E0000H	70000H
64K byte/32K word	D0000H	68000H
64K byte/32K word	C0000H	60000H
64K byte/32K word	B0000H	58000H
64K byte/32K word	A0000H	50000H
64K byte/32K word	90000H	48000H
64K byte/32K word	80000H	40000H
64K byte/32K word	70000H	38000H
64K byte/32K word	60000H	30000H
64K byte/32K word	50000H	28000H
64K byte/32K word	40000H	20000H
64K byte/32K word	30000H	18000H
64K byte/32K word	20000H	10000H
64K byte/32K word	10000H	08000H
64K byte/32K word	00000H	00000H

MB84VB2000 Sector Architecture

	(×8)	(×16)
	FFFFFH	7FFFFH
64K byte/32K word	F0000H	78000H
64K byte/32K word	E0000H	70000H
64K byte/32K word	D0000H	68000H
64K byte/32K word	C0000H	60000H
64K byte/32K word	B0000H	58000H
64K byte/32K word	A0000H	50000H
64K byte/32K word	90000H	48000H
64K byte/32K word	80000H	40000H
64K byte/32K word	70000H	38000H
64K byte/32K word	60000H	30000H
64K byte/32K word	50000H	28000H
64K byte/32K word	40000H	20000H
64K byte/32K word	30000H	18000H
64K byte/32K word	20000H	10000H
64K byte/32K word	10000H	08000H
32K byte/16K word	08000H	04000H
8K byte/4K word	06000H	03000H
8K byte/4K word	04000H	02000H
16K byte/8K word	00000H	00000H

MB84VB2001 Sector Architecture

■ FUNCTIONAL DESCRIPTION

Table 4 Sector Address Tables (MB84VB2000)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range (×8)	Address Range (×16)
SA0	0	0	0	0	X	X	X	00000H to 0FFFFH	00000H to 07FFFH
SA1	0	0	0	1	X	X	X	10000H to 1FFFFH	08000H to 0FFFFH
SA2	0	0	1	0	X	X	X	20000H to 2FFFFH	10000H to 17FFFH
SA3	0	0	1	1	X	X	X	30000H to 3FFFFH	18000H to 1FFFFH
SA4	0	1	0	0	X	X	X	40000H to 4FFFFH	20000H to 27FFFH
SA5	0	1	0	1	X	X	X	50000H to 5FFFFH	28000H to 2FFFFH
SA6	0	1	1	0	X	X	X	60000H to 6FFFFH	30000H to 37FFFH
SA7	0	1	1	1	X	X	X	70000H to 7FFFFH	38000H to 3FFFFH
SA8	1	0	0	0	X	X	X	80000H to 8FFFFH	40000H to 47FFFH
SA9	1	0	0	1	X	X	X	90000H to 9FFFFH	48000H to 4FFFFH
SA10	1	0	1	0	X	X	X	A0000H to AFFFFH	50000H to 57FFFH
SA11	1	0	1	1	X	X	X	B0000H to BFFFFH	58000H to 5FFFFH
SA12	1	1	0	0	X	X	X	C0000H to CFFFFH	60000H to 67FFFH
SA13	1	1	0	1	X	X	X	D0000H to DFFFFH	68000H to 6FFFFH
SA14	1	1	1	0	X	X	X	E0000H to EFFFFH	70000H to 77FFFH
SA15	1	1	1	1	0	X	X	F0000H to F7FFFH	78000H to 7BFFFH
SA16	1	1	1	1	1	0	0	F8000H to F9FFFH	7C000H to 7CFFFH
SA17	1	1	1	1	1	0	1	FA000H to FBFFFH	7D000H to 7DFFFH
SA18	1	1	1	1	1	1	X	FC000H to FFFFFH	7E000H to 7FFFFH

Table 5 Sector Address Tables (MB84VB2001)

Sector Address	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Address Range (×8)	Address Range (×16)
SA0	0	0	0	0	0	0	X	00000H to 03FFFH	00000H to 01FFFH
SA1	0	0	0	0	0	1	0	04000H to 05FFFH	02000H to 02FFFH
SA2	0	0	0	0	0	1	1	06000H to 07FFFH	03000H to 03FFFH
SA3	0	0	0	0	1	X	X	08000H to 0FFFFH	04000H to 07FFFH
SA4	0	0	0	1	X	X	X	10000H to 1FFFFH	08000H to 0FFFFH
SA5	0	0	1	0	X	X	X	20000H to 2FFFFH	10000H to 17FFFH
SA6	0	0	1	1	X	X	X	30000H to 3FFFFH	18000H to 1FFFFH
SA7	0	1	0	0	X	X	X	40000H to 4FFFFH	20000H to 27FFFH
SA8	0	1	0	1	X	X	X	50000H to 5FFFFH	28000H to 2FFFFH
SA9	0	1	1	0	X	X	X	60000H to 6FFFFH	30000H to 37FFFH
SA10	0	1	1	1	X	X	X	70000H to 7FFFFH	38000H to 3FFFFH
SA11	1	0	0	0	X	X	X	80000H to 8FFFFH	40000H to 47FFFH
SA12	1	0	0	1	X	X	X	90000H to 9FFFFH	48000H to 4FFFFH
SA13	1	0	1	0	X	X	X	A0000H to AFFFFH	50000H to 57FFFH
SA14	1	0	1	1	X	X	X	B0000H to BFFFFH	58000H to 5FFFFH
SA15	1	1	0	0	X	X	X	C0000H to CFFFFH	60000H to 67FFFH
SA16	1	1	0	1	X	X	X	D0000H to DFFFFH	68000H to 6FFFFH
SA17	1	1	1	0	X	X	X	E0000H to EFFFFH	70000H to 77FFFH
SA18	1	1	1	1	X	X	X	F0000H to FFFFFH	78000H to 7FFFFH

Table 6.1 Flash Memory Autoselect Codes

Type			A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			V_{IL}	V_{IL}	V_{IL}	V_{IL}	04H
Device Code	MB84VB2000	Byte	V_{IL}	V_{IL}	V_{IH}	V_{IL}	DAH
		Word				X	22DAH
	MB84VB2001	Byte	V_{IL}	V_{IL}	V_{IH}	V_{IL}	5BH
		Word				X	225BH

*1: A_{-1} is for Byte mode.

Table 6.2 Expanded Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacture's Code			04H	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MB84VB2000	(B)	DAH	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	1	0	1	1	0	1	0
		(W)	22DAH	0	0	1	0	0	0	1	0	1	1	0	1	1	0	1	0
	MB84VB2001	(B)	5BH	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	0	1	1	0	1	1
		(W)	225BH	0	0	1	0	0	0	1	0	0	1	0	1	1	0	1	1

(B): Byte mode
(W): Word mode

Table 7 Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
		AAAH		555H		AAAH							
Autoselect	3	555H	AAH	2AAH	55H	555H	90H	—	—	—	—	—	—
		AAAH		555H		AAAH							
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
		AAAH		555H		AAAH							
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
		AAAH		555H		AAAH		AAAH		555H			
Sector Erase Suspend		Erase can be suspended during sector erase with Addr. ("H" or "L"). Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr. ("H" or "L"). Data (30H)											
Set to Fast Mode	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
		AAAH		555H		AAAH							
Fast Program (Note)	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
		XXXH											
Reset from Fast Mode (Note)	2	XXXH	90H	XXXH	F0H	—	—	—	—	—	—	—	—
		XXXH		XXXH									
Extended Sector Protect	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—

Address bits A_{11} to A_{17} = X = "H" or "L" for all address commands except or Program Address (PA) and Sector Address (SA).

Bus operations are defined in Tables 2 and 3.

The system should generate the following address patterns:
Word Mode: 555H or 2AAH to addresses A_0 to A_{10}
Byte Mode: AAAH or 555H to addresses A_{-1} and A_0 to A_{10}

Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

RA =Address of the memory location to be read
PA =Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
SA =Address of the sector to be erased. The combination of A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
RD =Data read from location RA during read operation.
PD =Data to be programmed at location PA. Data is latched on the falling edge of write pulse.
SPA:Sector address to be protected. Set sector address (SA) and (A_6, A_1, A_0) = (0, 1, 0).
SD:Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –55°C to +125°C
Ambient Temperature with Power Applied ..... –25°C to +85°C
Voltage with Respect to Ground All pins (Note) ..... –0.3 V to V_{CC} + 0.5 V
V_{CCf}/V_{CCs} Supply (Note) ..... –0.3 V to +4.6 V

Note: Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{CCf} + 0.5 V or V_{CCs} + 0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Commercial Devices
Ambient Temperature (T_A) ..... –40°C to +85°C
V_{CC} Supply Voltages ..... +2.7 V to +3.6 V
Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max. A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	70	µA
I_{CC1}	V_{CC} Active Current (Note 1, 5)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 10 MHz	Byte	—	22	mA
			Word		25	
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz	Byte	—	12	mA
			Word		15	
I_{CC2}	V_{CC} Active Current (Note 2, 5)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	35	mA
I_{CC3}	V_{CC} Current (Standby) (Note 5)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ± 0.3 V, $\overline{RESET}$ = V_{CC} ± 0.3 V		—	5	µA
I_{CC4}	V_{CC} Current (Standby, Reset) (Note 5)	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{SS} ± 0.3 V		—	5	µA
I_{CC5}	V_{CC} Current (Automatic Sleep Mode) (Note 3, 5)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{SS} ± 0.3 V, $\overline{RESET}$ = V_{CC} ± 0.3 V V_{IN} = V_{CC} ± 0.3 V or V_{SS} ± 0.3 V		—	5	µA
V_{IL}	Input Low Level	—		–0.5	0.6	V
V_{IH}	Input High Level	—		2.0	V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) (Note 4)	—		11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min.		—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min.		2.4	—	V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.		V_{CC} – 0.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—		2.3	2.5	V

Notes: 1.The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 10 MHz).

2.I_{CC} active while Embedded Algorithm (program or erase) is in progress.

3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

4. (V_{ID} – V_{CC}) do not exceed 9 V.

5. Total power consumption is (condition of Flash 1) + (condition of Flash 2).

■ AC CHARACTERISTICS

- **$\overline{CE}$ Timing**

Parameter Symbols		Description	Test Setup		-10	Unit
JEDEC	Standard					
—	t_{CCR}	$\overline{CE}$ Recover Time	—	Min.	0	ns

- **Read Only Operations Characteristics**

Parameter Symbols		Description	Test Setup	-10 (Note)		Unit
JEDEC	Standard			Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	—	100	—	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	—	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	—	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	—	30	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	0	—	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	—	20	µs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	—	5	ns

Note: Test Conditions–Output Load: 1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

• **Erase/Program Operations**

Parameter Symbols		Description		-10			Unit
JEDEC	Standard			Min.	Typ.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time		100	—	—	ns
t_{AVWL}	t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)		0	—	—	ns
t_{AVEL}	t_{AS}	Address Setup Time ($\overline{CE}$ to Addr.)		0	—	—	ns
t_{WLAX}	t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)		50	—	—	ns
t_{ELAX}	t_{AH}	Address Hold Time ($\overline{CE}$ to Addr.)		50	—	—	ns
t_{DVWH}	t_{DS}	Data Setup Time		50	—	—	ns
t_{WHDX}	t_{DH}	Data Hold Time		0	—	—	ns
—	t_{OES}	Output Enable Setup Time		0	—	—	ns
—	t_{OEH}	Output Enable Hold Time	Read	0	—	—	ns
			Toggle and $\overline{Data}$ Polling	10	—	—	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$)		0	—	—	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)		0	—	—	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time ($\overline{CE}$ to $\overline{WE}$)		0	—	—	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time ($\overline{WE}$ to $\overline{CE}$)		0	—	—	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time ($\overline{CE}$ to $\overline{WE}$)		0	—	—	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time ($\overline{WE}$ to $\overline{CE}$)		0	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width		50	—	—	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		50	—	—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		30	—	—	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		30	—	—	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		—	8	—	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		—	1	15	sec
—	t_{VCS}	V_{CC} Setup Time		50	—	—	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)		500	—	—	ns
—	t_{VLHT}	Voltage Transition Time (Note 2)		4	—	—	µs
—	t_{WPP}	Write Pulse Width (Note 2)		100	—	—	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		4	—	—	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)		4	—	—	µs
—	t_{RB}	Recover Time from RY/$\overline{BY}$		0	—	—	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		500	—	—	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		200	—	—	ns
—	t_{EOE}	Delay Time from Embedded Output Enable		—	—	100	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		—	—	90	ns
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z		—	—	30	ns
—	t_{FLQV}	$\overline{BYTE}$ Switching High to Output Active		30	—	—	ns

Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Protection operation.

■ SWITCHING WAVEFORMS

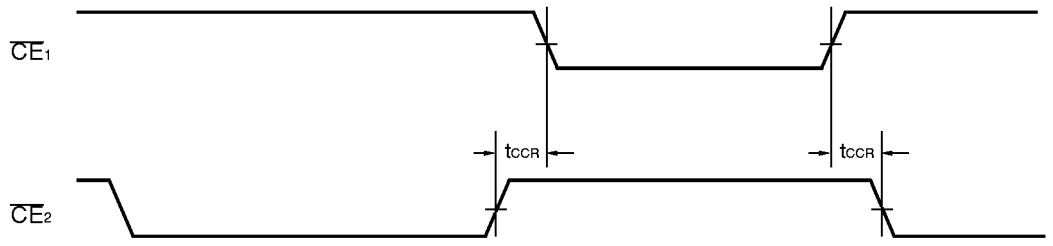


Figure 1 Timing Diagram for Alternating Flash to Flash

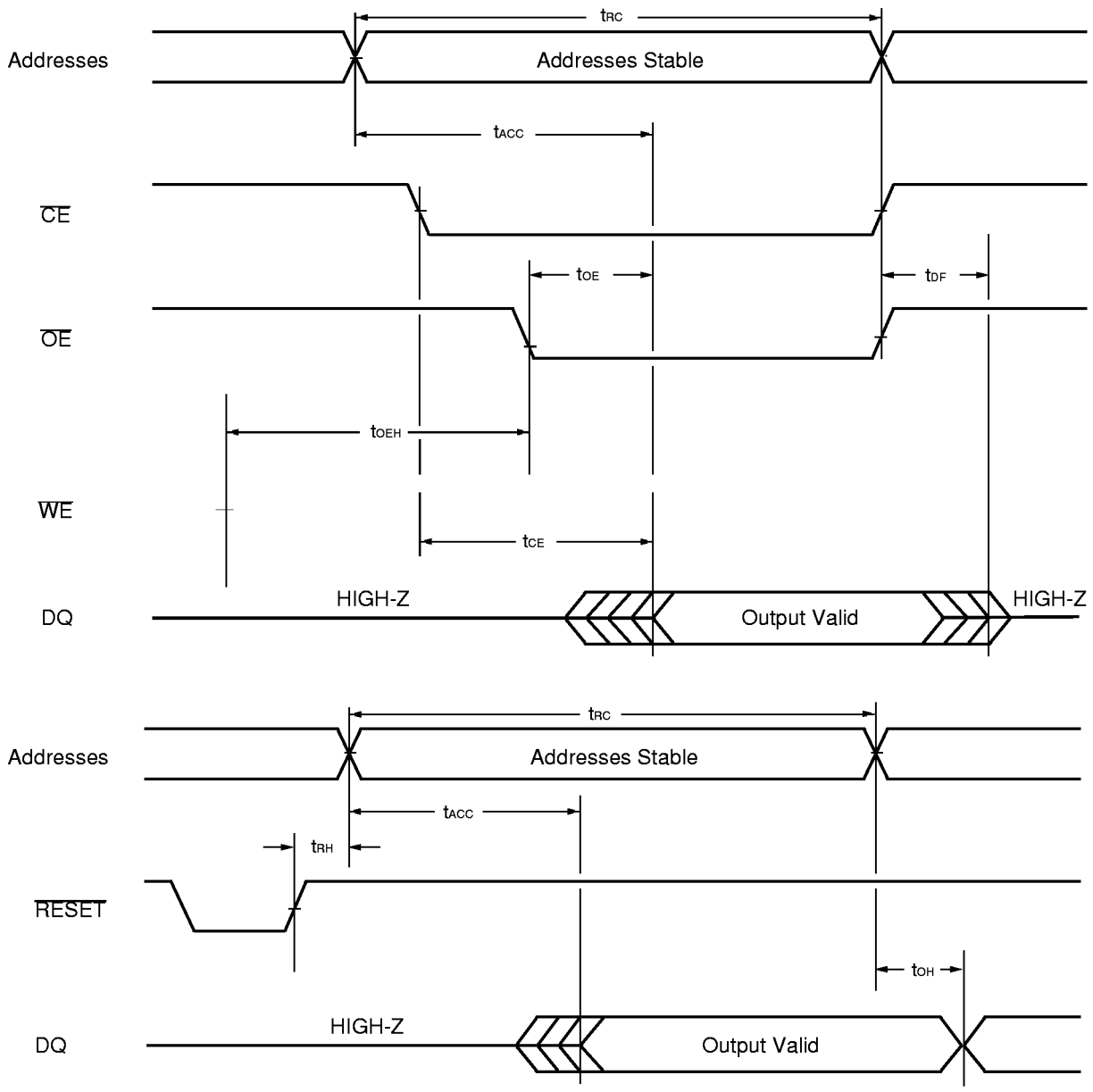
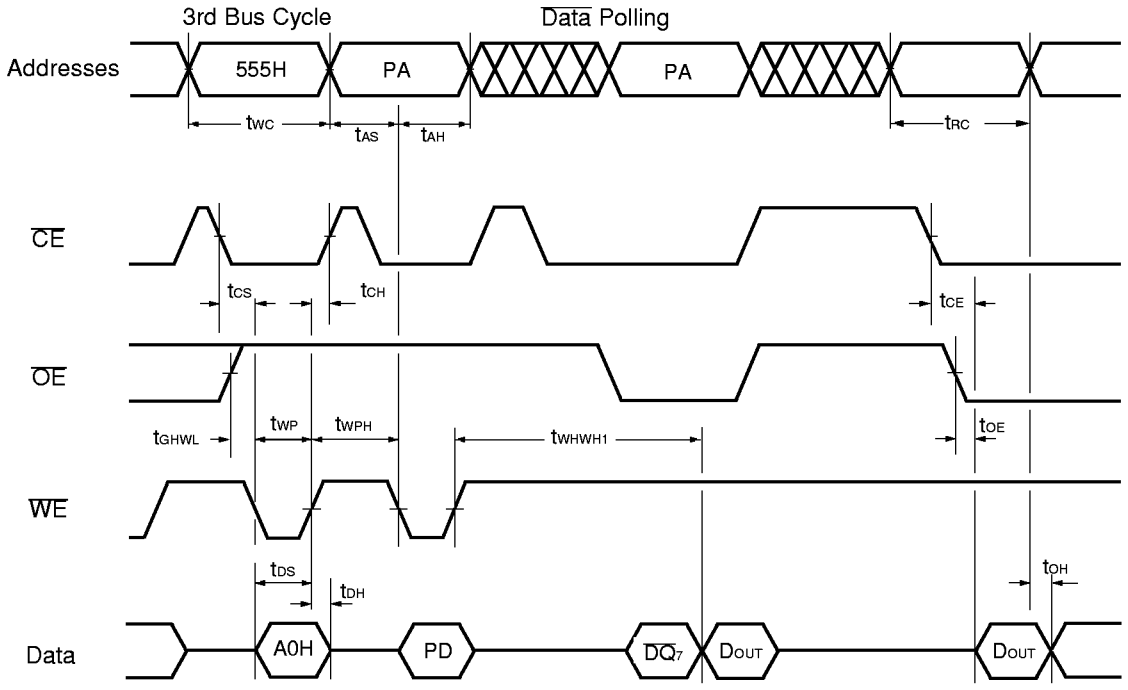
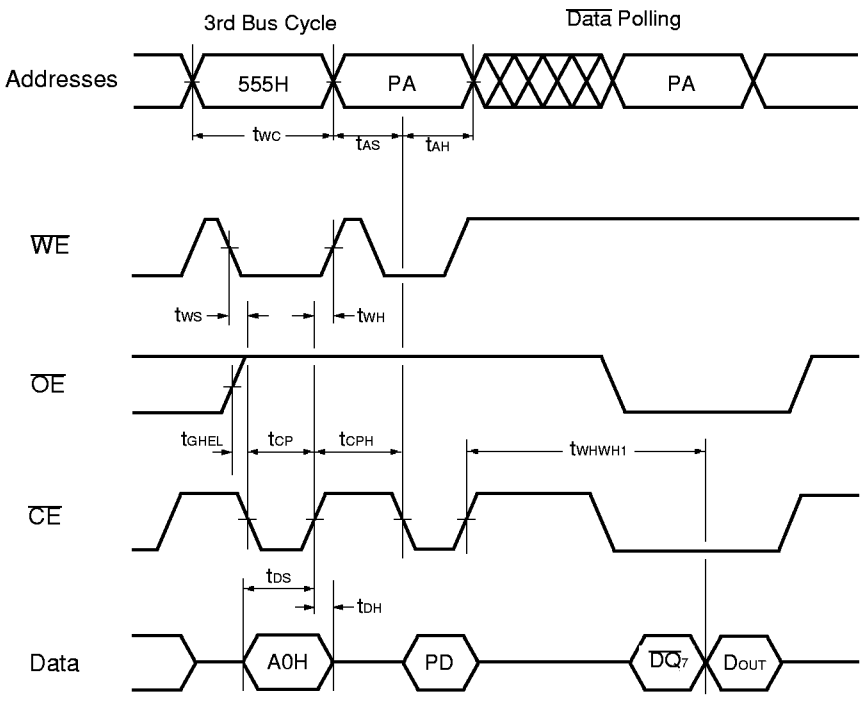


Figure 2 AC Waveforms for Read Operations



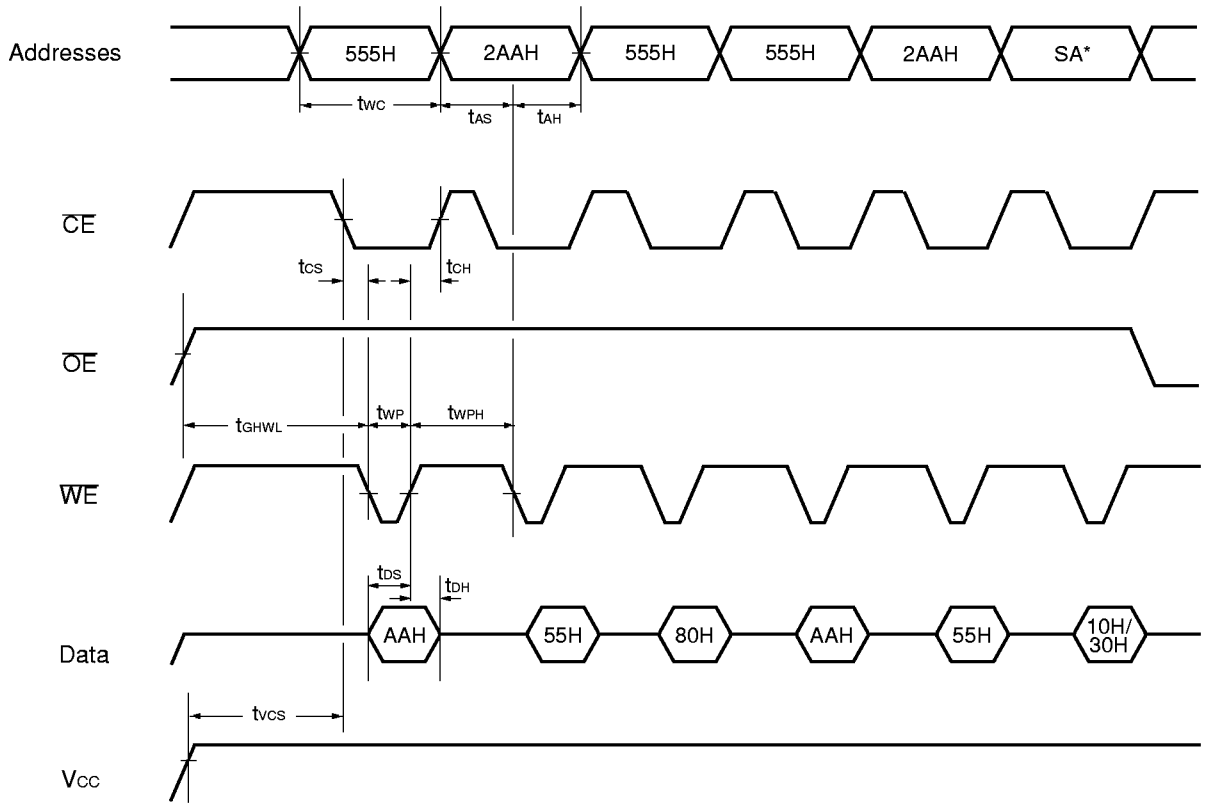
Notes: 1.PA is address of the memory location to be programmed.
2.PD is data to be programmed at byte address.
3.$\overline{DQ_7}$ is the output of the complement of the data written to the device.
4.D_{OUT} is the output of the data written to the device.
5.Figure indicates last two bus cycles out of four bus cycle sequence.
6.These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

Figure 3 Alternate $\overline{WE}$ Controlled Program Operation Timings



Notes: 1.PA is address of the memory location to be programmed.
2.PD is data to be programmed at byte address.
3.$\overline{DQ_7}$ is the output of the complement of the data written to the device.
4.D_{OUT} is the output of the data written to the device.
5.Figure indicates last two bus cycles out of four bus cycle sequence.
6.These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

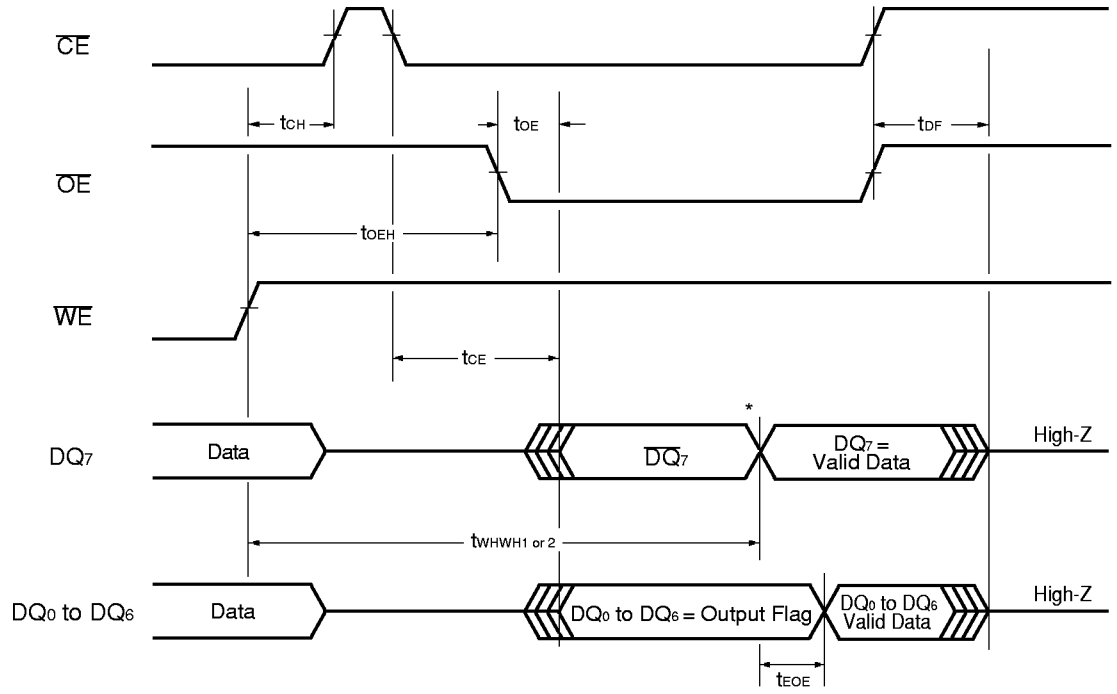
Figure 4 Alternate $\overline{CE}$ Controlled Program Operation Timings



* : SA is the sector address for Sector Erase. Addresses = 555H (Word), AAAH (Byte) for Chip Erase.

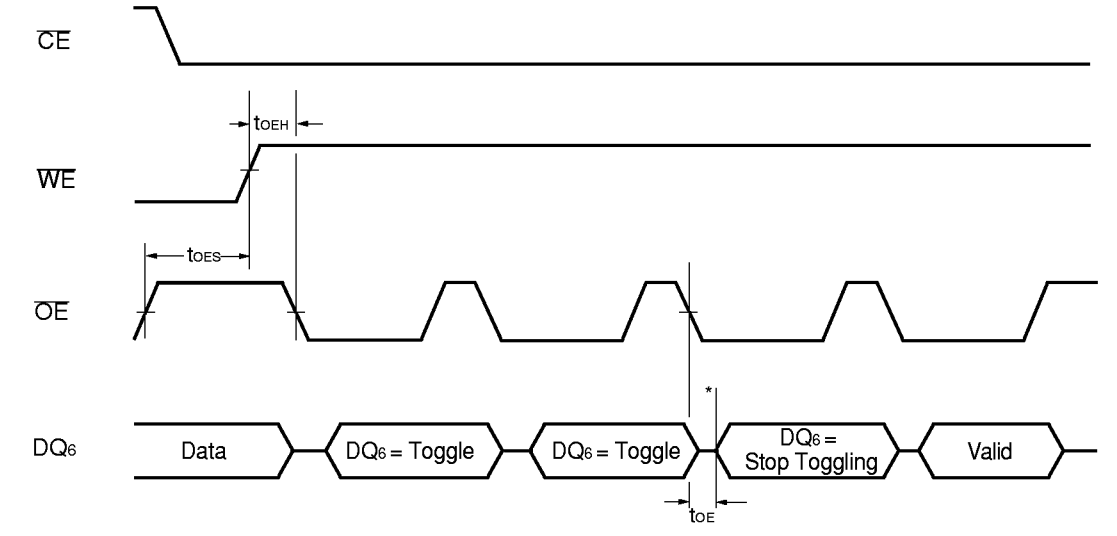
Note: These waveforms are for the × 16 mode. (The addresses differ from × 8 mode.)

Figure 5 AC Waveforms Chip/Sector Erase Operations



* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

Figure 6 AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations



* : DQ_6 stops toggling.(The device has completed the Embedded operation.)

Figure 7 AC Waveforms for Toggle Bit during Embedded Algorithm Operations

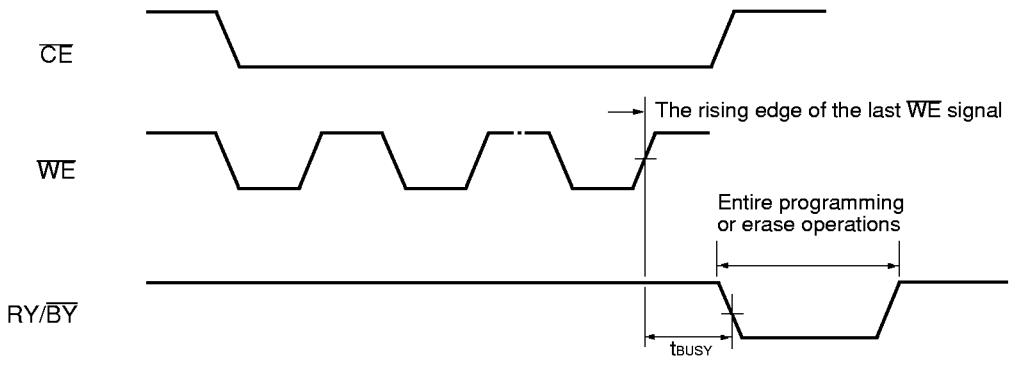


Figure 8 RY/BY Timing Diagram during Write/Erase Operations

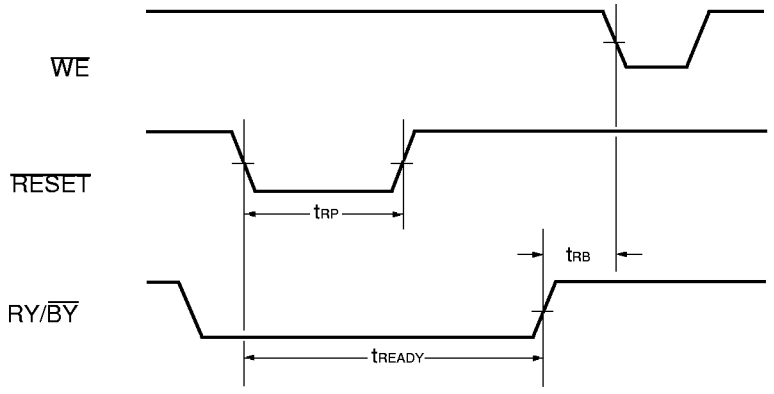


Figure 9 RESET, RY/BY Timing Diagram

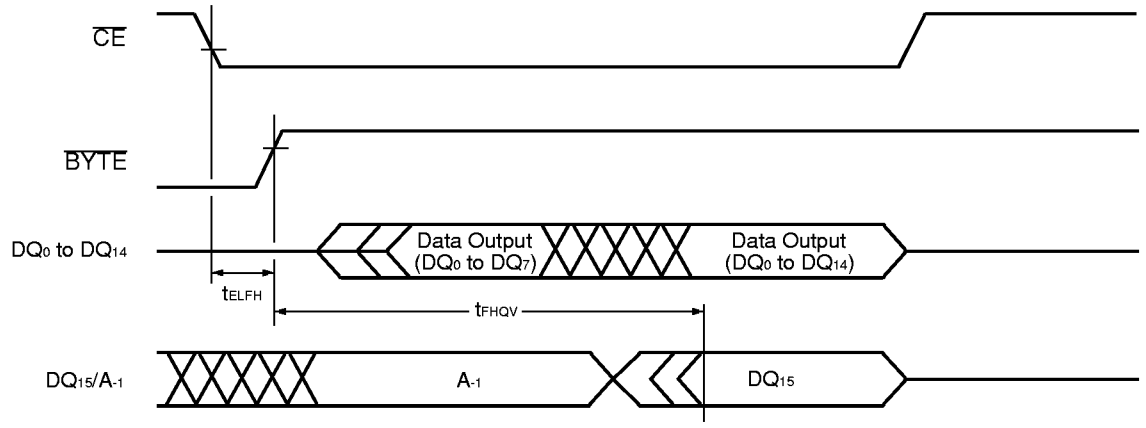


Figure 10 Timing Diagram for Word Mode Configuration

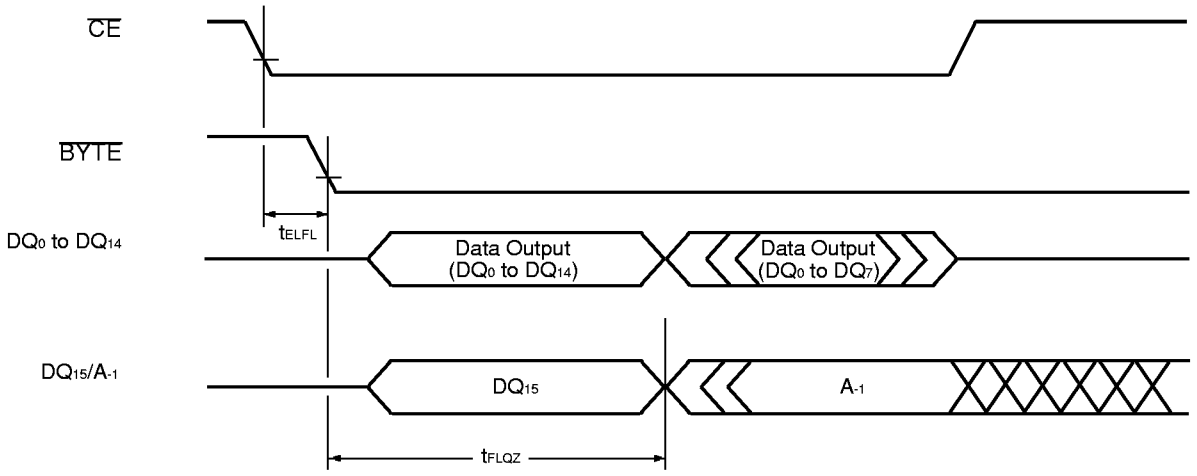


Figure 11 Timing Diagram for Byte Mode Configuration

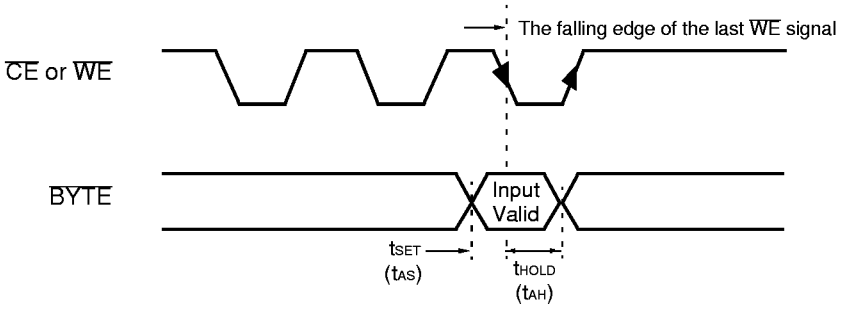
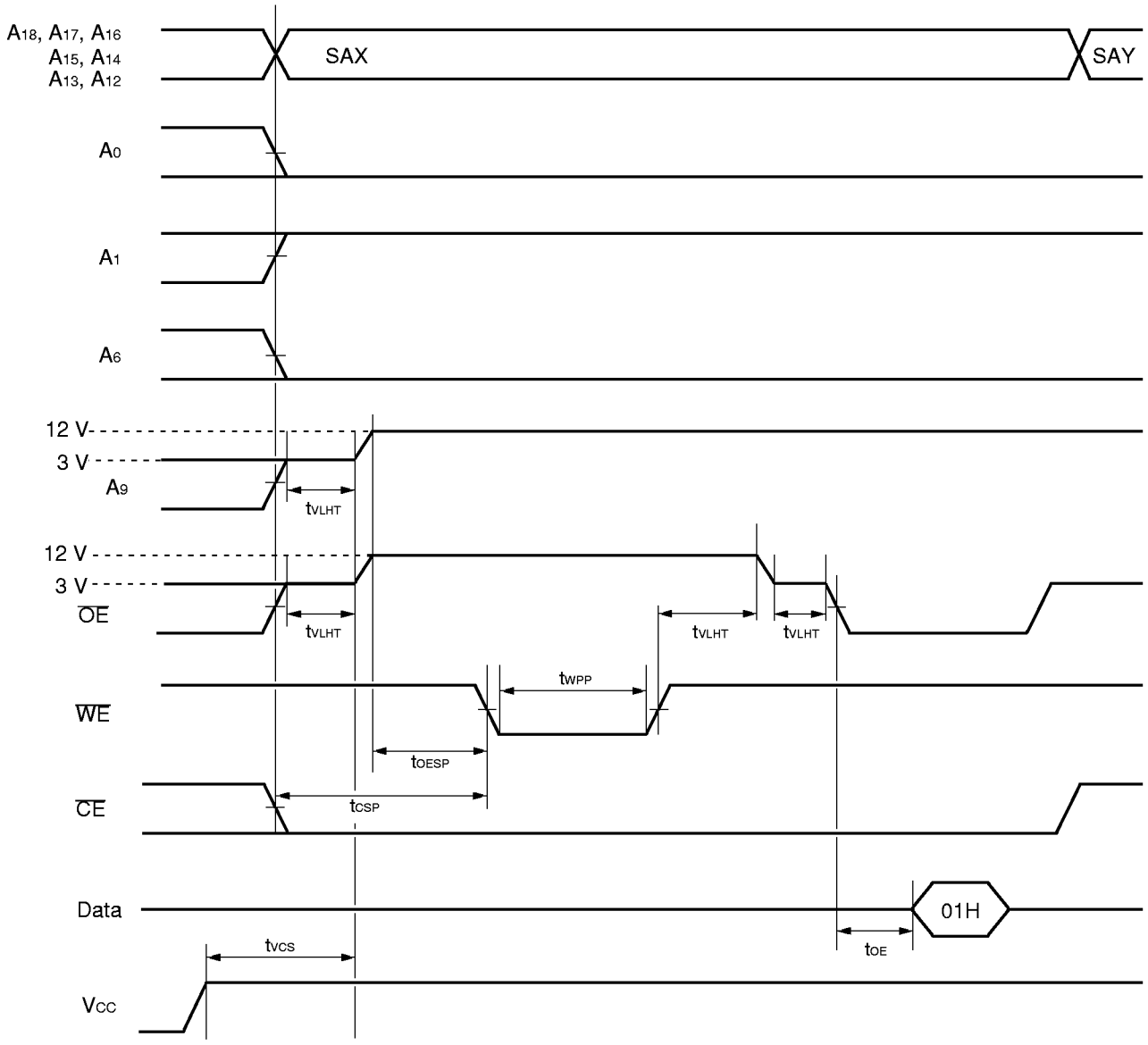


Figure 12 BYTE Timing Diagram for Write Operations



SAX : Sector Address for initial sector
SAY : Sector Address for next sector
Note: A_{-1} is V_{IL} on byte mode.

Figure 13 AC Waveforms for Sector Protection Timing Diagram

FAST MODE ALGORITHM

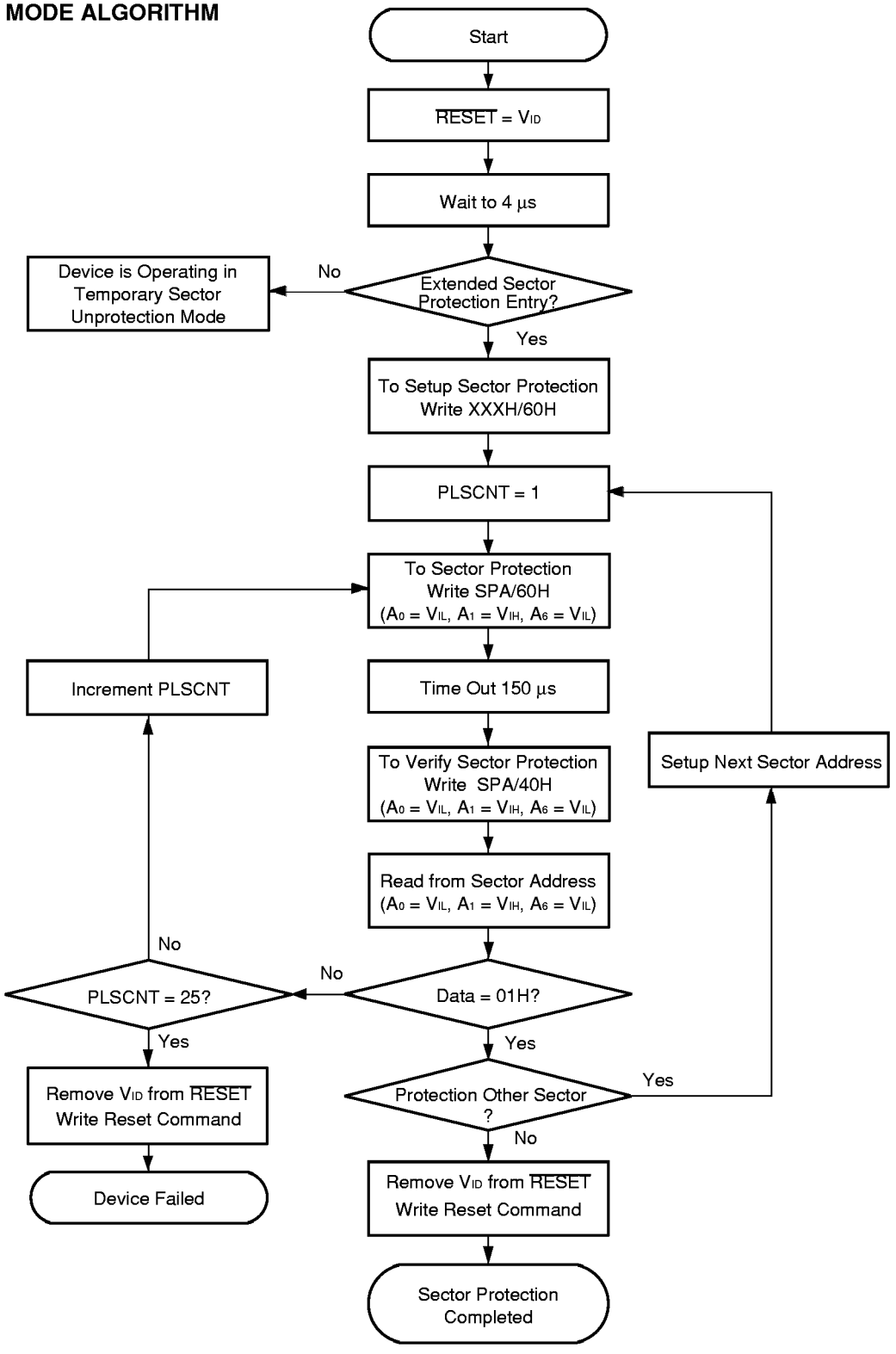


Figure 14 Extended Sector Protection Algorithm

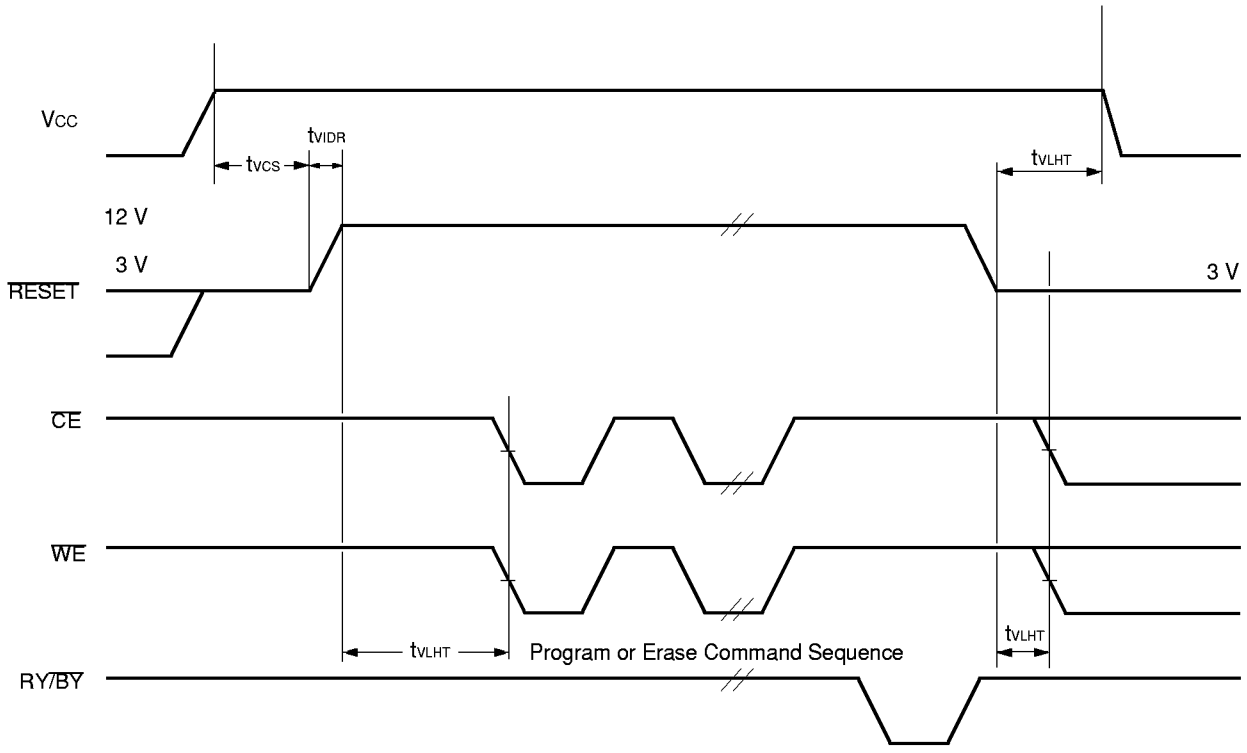
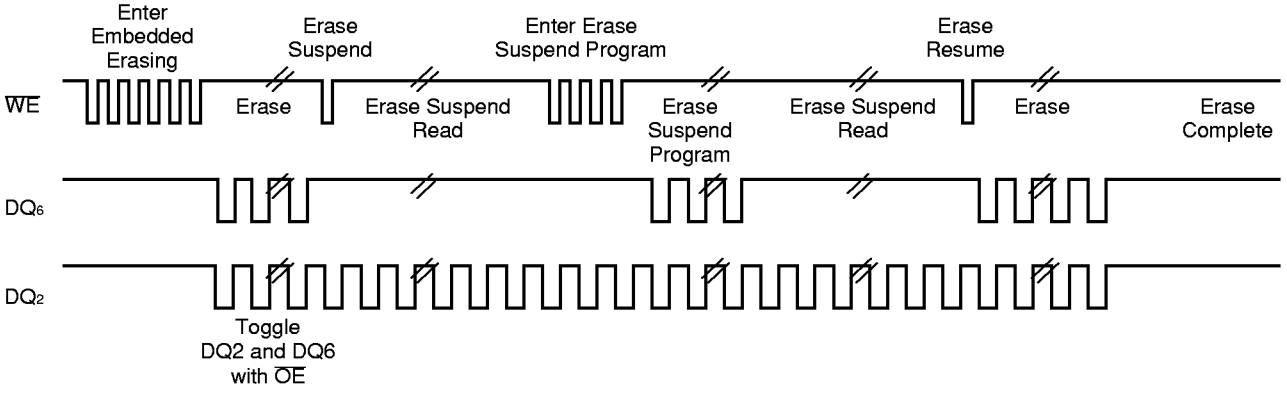


Figure 15 Temporary Sector Unprotection Timing Diagram



Note: DQ_2 is read from the erase-suspended sector.

Figure 16 DQ_2 vs DQ_6

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes programming time prior to erasure
Word Programming Time	—	16	5,200	µs	Excludes system-level overhead
Byte Programming Time	—	8	3,600	µs	
Chip Programming Time (1M Byte)	—	8.4	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TBD	TBD	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TBD	TBD	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TBD	TBD	pF

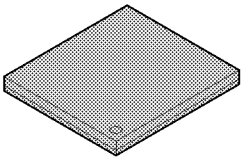
Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ HANDLING OF PACKAGE

Please hadle this package carefully since the sides of package are right angle.

■ PACKAGE

48-pin plastic FBGA

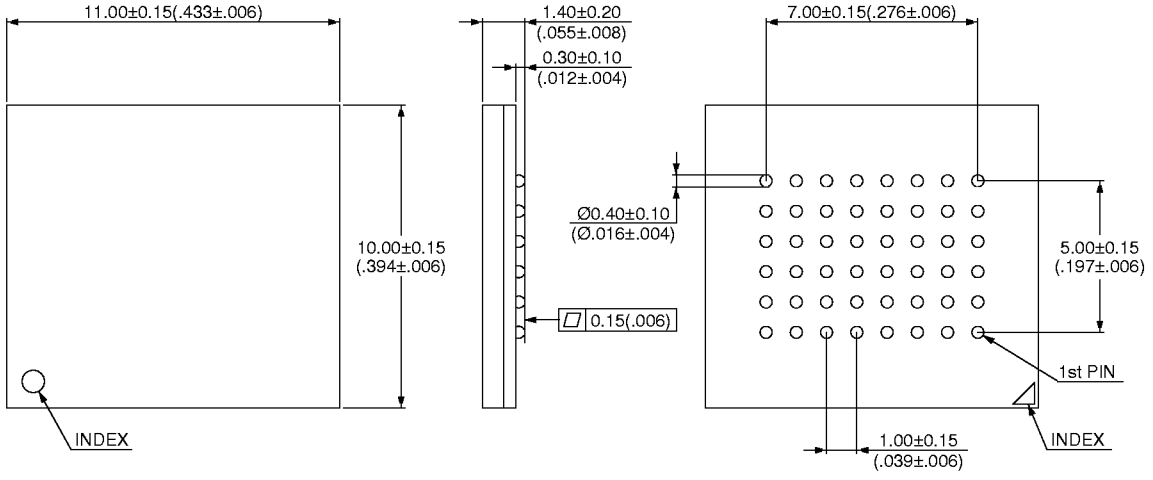


(BGA-48P-M06)

■ PACKAGE DIMENSIONS

48-pin plastic BGA
(BGA-48P-M06)

Note: The actual shape of corners may differ from the dimension.



Dimension in mm (inches).

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