256K x 4 Static RAM

Key Parameters S256K4 and S256K4L	Device Types			Unit
	25C	35M 35I 35C	45M 45I 45C	
Access Time	25	35	45	nS
Cycle Time	25	35	45	nS
Output Enable Access	10	15	20	nS

Features

- **300 mil wide 28 pin DIP**
- **Advanced 4-T CMOS technology**
- **SOJ, LCC, and Flatpack Available**
- **Military, industrial, and commercial temperature range**
- **Military grades compliant to MIL-STD-883C**

General Description

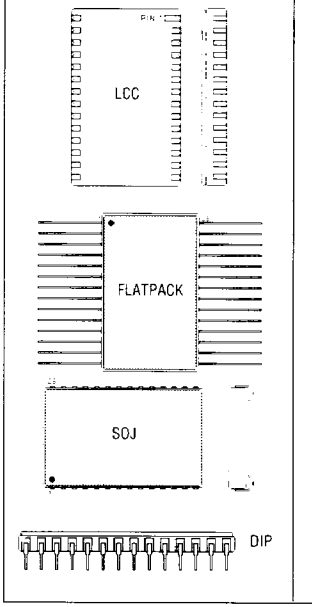
The Inova S256K4 is a high performance one megabit Static Random Access Memory (SRAM) organized as 256K by four bits.

The S256K4 is manufactured using a highly reliable, four transistor cell CMOS process. This provides a component which combines low active and standby power characteristics with high performance.

All inputs are fully TTL-compatible. Operation is fully static, without need for extra control logic to generate clock signals.

Every military grade device is fully compliant to MIL-STD-883C, paragraph 1.2.1. Industrial and commercial grade devices are fabricated in the same production line which ensures that they are also of the highest quality.

Package Options



Pinout

1	A10	28	VCC
2	A9	27	A11
3	A8	26	A12
4	A7	25	A13
5	A6	24	A14
6	A5	23	A15
7	A4	22	A16
8	A3	21	A17
9	A2	20	NC
10	A1	19	I/O3
11	A0	18	I/O2
12	$\overline{CS}$	17	I/O1
13	$\overline{OE}$	16	I/O0
14	VSS	15	$\overline{WE}$

A0-A17 Address Inputs
I/O0-I/O3 Data Input/ Output
$\overline{WE}$ Write Enable
$\overline{OE}$ Output Enable
$\overline{CS}$ Chip Select
VCC +5V Power
VSS Ground

Recommended Operating Conditions

Parameter	*Symbol*	*Min.*	*Max.*	*Unit*
Supply Voltage(1)	V_{CC}	4.5	5.5	V
Input HIGH Voltage	V_{IH}	2.2	V_{CC}+0.5	V
Input LOW Voltage	V_{IL}	-0.5	0.8	V
Operating Temp. Mil.	T_C	-55	125	°C
Operating Temp. Ind.	T_C	-40	85	°C
Operating Temp. Comm.	T_C	0	70	°C

Absolute Maximum Ratings (2)

Temperature Under Bias	-55 °C to 125 °C
Storage Temperature	-65 °C to 150 °C
Supply Voltage(1)	-0.5V to 7.0 V
Signal Voltage On Any Pin	-0.5 V to V_{CC} + 0.5V
Power Dissipation	1 Watt
D.C. Continuous Output Current Per Output	20 mA
Lead Temperature (Soldering 10 sec)	260 °C

Notes:

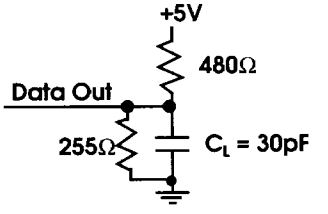
1. All voltages referenced to V_{SS} (GND).

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*I/O Operation*	*Supply Current*
Standby	H	X	X	High Z	I_{SB}/I_{FSB}
Read	L	L	H	Output	I_{CC2}
Write	L	X	L	Input	I_{CC2}
Output Disable	L	H	H	High Z	I_{CC2}

Load Test Circuits



C_L = 5pF for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{WLZ}.

Memory Scale

Access Time	25	35	45	**Unit**
S256K4	40	29	22	kbits/ns

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

DC and Operating Characteristics

M=Military; C=Commercial; I=Industrial

Parameters	Symbol	Test Conditions		S256K4 Min	S256K4 Max	S256K4L Min	S256K4L Max	UNITS
Input Leakage	$\|I_{LI}\|$	V_{CC} = max, V_{IN} = GND to V_{CC}			2		2	µA
Output Leakage	$\|I_{LO}\|$	V_{OUT} = GND to V_{CC}, $\overline{CS} > V_{IH}$			2		2	µA
Static Supply Current	I_{CC1}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$ No Address Transitions	C I M		90 95 100		80 85 90	mA
Dynamic Supply Current	I_{CC2}	$\overline{CS} \leq V_{IL}$, $\overline{OE} = V_{IH}$ Address change every t_{RC}			140		125	mA
Standby Supply Current With Address Changes	I_{SB}	$\overline{CS} > V_{IH}$ Address change every t_{RC}	C I M		30 35 40		3 4 10	mA
Standby Supply Current With CMOS Levels	I_{FSB}	$\overline{CS} = V_{CC} \pm 0.2V$ No Address Transistions	C I M				0.75 1.25 5.0	mA
Data Retention Current At V = 2.0V_{DR}	I_{CCDR}	$\overline{CS} = V_{DR}$ min $V_{CC} = V_{DR}$ min	C I M				0.10 0.15 2.0	mA
Data Retention Voltage	V_{DR}	V_{CC} input voltage		3.0		2.0		V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA		2.4		2.4		V

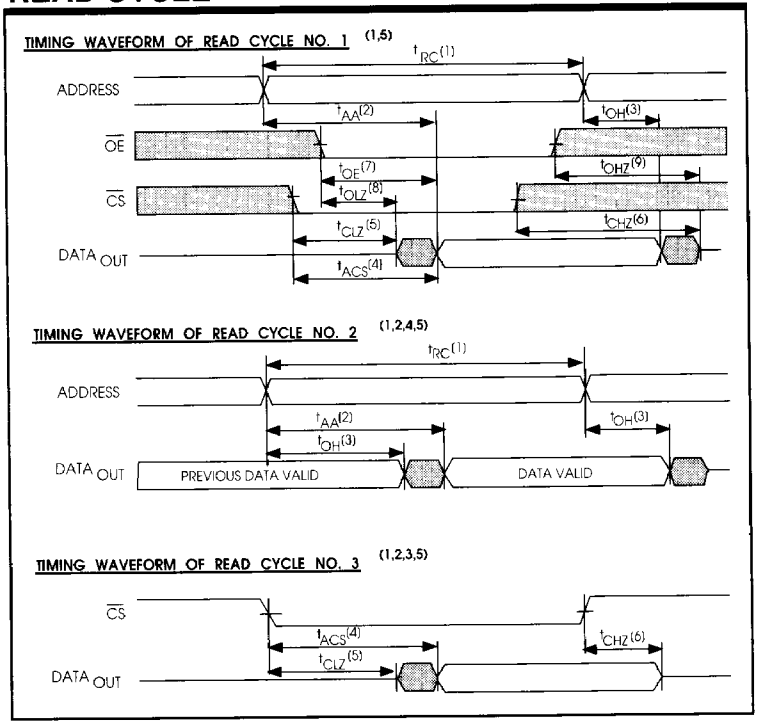
Pin Capacitance (Typical)	Test Conditions	Addresses	Data I/O	$\overline{CS}$, $\overline{WE}$, $\overline{OE}$	Units
	Pin Voltage = 0V, f=1.0 Mhz	8	10	12	pF

AC Characteristics (1)

No.	S256K4 and S256K4L Parameter	Symbol	25C Min	25C Max	35C,I,M Min	35C,I,M Max	45C,I,M Min	45C,I,M Max
1	Read Cycle Time	t_{RC}	25		35		45	
2	Address Access Time	t_{AA}		25		35		45
3	Output Hold from Address Change	t_{OH}	3		5		5	
4	$\overline{CS}$ Access Time	t_{ACS}		25		35		45
5	$\overline{CS}$ on to Output in Low Z	t_{CLZ} (2,3)	5		5		5	
6	$\overline{CS}$ off to Output in High Z	t_{CHZ} (2,3)	0	10	0	15	0	20
7	$\overline{OE}$ on to Output Valid	t_{OE}		10		15		20
8	$\overline{OE}$ on to Output in Low Z	t_{OLZ} (2,3)	0		0		0	
9	$\overline{OE}$ off to Output in High Z	t_{OHZ} (2,3)	0	10	0	15	0	20
10	Write Cycle Time	t_{WC}	25		35		45	
11	Chip Selection to End of Write	t_{CW}	20		25		30	
12	Address Valid to End of Write	t_{AW}	20		25		30	
13	Address Set-up Time	t_{AS}	0		0		0	
14	Write Pulse Width	t_{WP}	20		25		30	
15	Write Recovery Time	t_{WR}	0		0		0	
16	Data Valid Set-Up to End of Write	t_{DW}	15		20		25	
17	Data Hold from End of Write	t_{DH}	0		0		0	
18	Write Pulse on to Output in High Z	$t_{WHZ(2,3)}$	0	10	0	15	0	20
19	Write Pulse off to Output in Low Z	$t_{WLZ(2,3)}$	5		5		5	
20	Chip Deselect to Data Retention	$t_{CDR(2)}$	0		0		0	
21	Operation Recovery Time	t_{R} (2)		25		35		45

Notes: (1) At Recommended Operating Conditions. All Values in Nanoseconds. (2) This Parameter is characterized initially and after any design or process change which could affect it. It is guaranteed to, but not tested to, the limits specified. (3) All I/O Transitions are measured ± 500mV from steady state with loading as specified in "Load Test Circuits."

READ CYCLE



Reading the S256K4 device is accomplished by taking chip select ($\overline{CS}$) and output enable($\overline{OE}$) LOW , while write enable ($\overline{WE}$) remains inactive or high. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/ output pins.

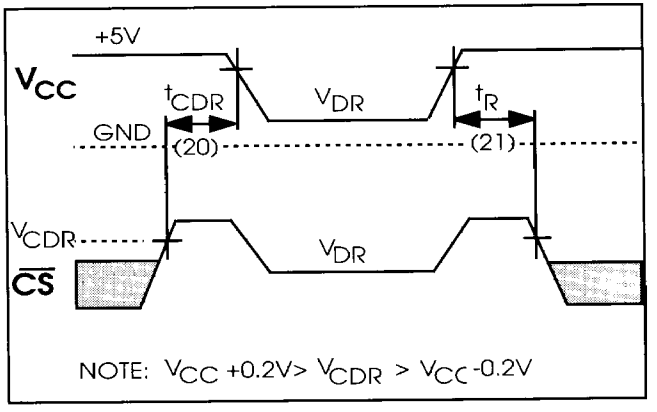
Notes:

1. $\overline{WE}$ is high for READ CYCLES.
2. Device is continuously selected, $\overline{CS}$= V_{IL} for all outputs active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ =V_{IL}
5. Data Output transitions measured ±500mV from steady state. This parameter is sampled and not 100% tested

Data Retention

S256K4 devices exhibit very low current drain when operated in Data Retention Mode. This Mode is entered by first driving Chip Select to V_{CC} and subsequently driving both V_{CC} and Chip Select to V_{DR}. Chip Select must be set up before the V_{CC} drops below its minimum level. When exiting from Data Retention Mode, the user must wait one full Read Cycle Time prior to asserting Chip Select.

DATA RETENTION TIMING



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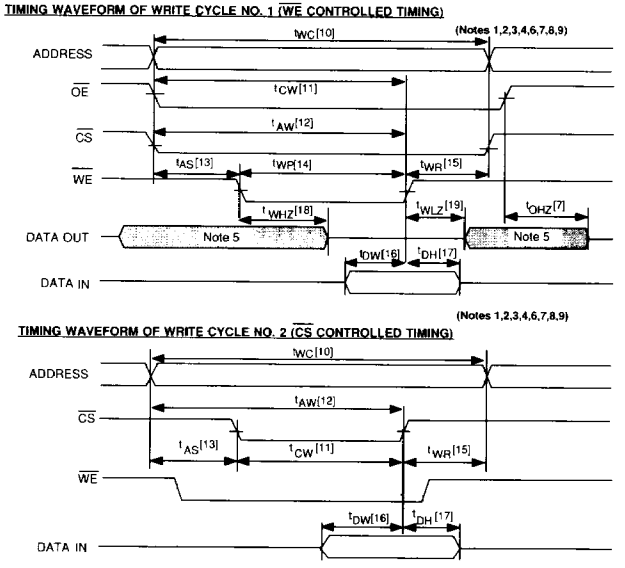
WRITE CYCLE



Writing to the S256K4 is achieved when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are LOW. Data on the input/output pins is written into the memory location specified on the address pins (A0-A17).

The input/output pins remain in a high impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

NOTES

1. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition of $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition of $\overline{CS}$ going high and $\overline{WE}$ going high. During a $\overline{WE}$ controlled write cycle, write pulse low is ≥ TDW + TWHZ to allow the I/O drivers to turn off and data to be placed on the bus for the required TDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle this requirement does not apply and the write pulse can be as short as the specified TWP.

2. TCW is measured from $\overline{CS}$ going low to the end of write.

3. TAS is measured from the address valid to the beginning of write.

4. TWR is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write.

5. During this period, I/O pins are in the output state, therefore input signals of opposite phase must not be applied.

6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ goes low, the outputs remain in a high impedance state.

7. DATA OUT is the same data written during the present cycle.

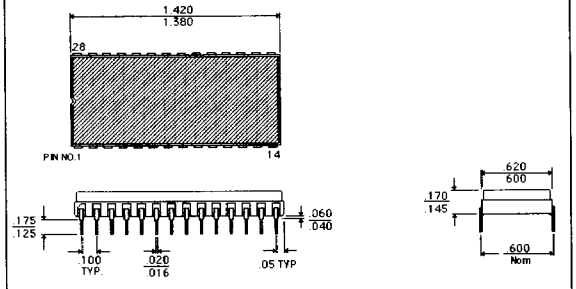
8. The real data of the next address is present at DATA OUT TAA after the address transition.

9. The tri-state parameters of data input and output are measured ±500mV from steady state. These parameters are sampled and characterized but not 100% tested.

Package Dimension and Ordering Information

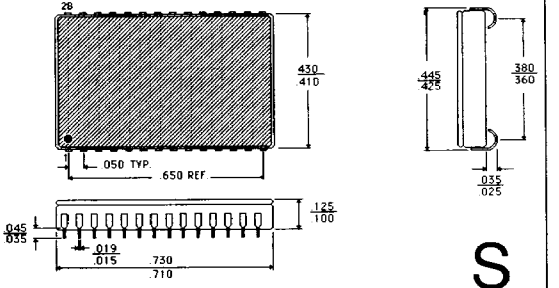
C

28 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
600 MILWIDE



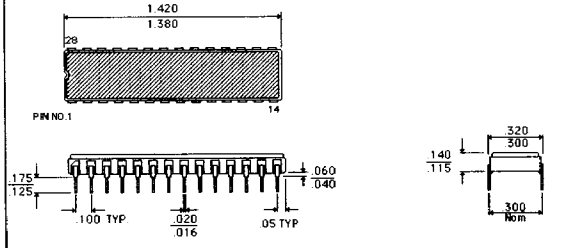
S

28 PIN CERAMIC "J" LEADED 400 MIL WIDE PACKAGE



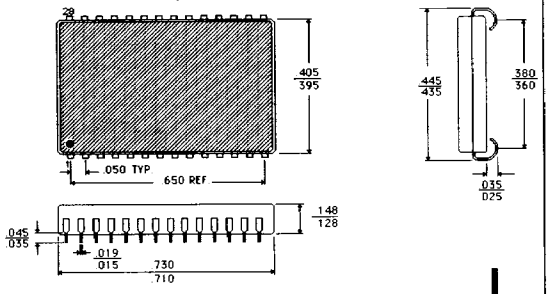
T

28 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
300 MIL WIDE



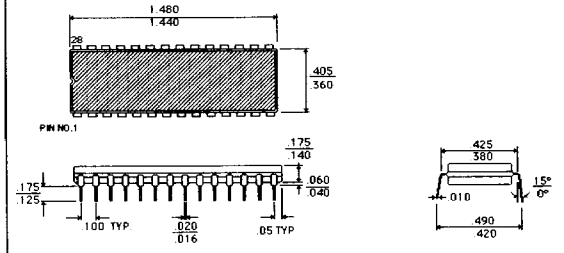
J

28 PIN PLASTIC SOJ PACKAGE, 400 MIL WIDE BODY



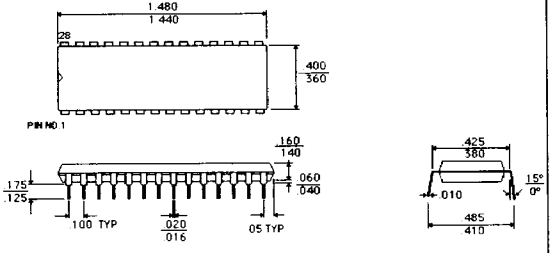
D

28 LEAD (400 MIL) CERDIP PACKAGE



P

28 LEAD (400 MIL) MOLDED DIP PACKAGE



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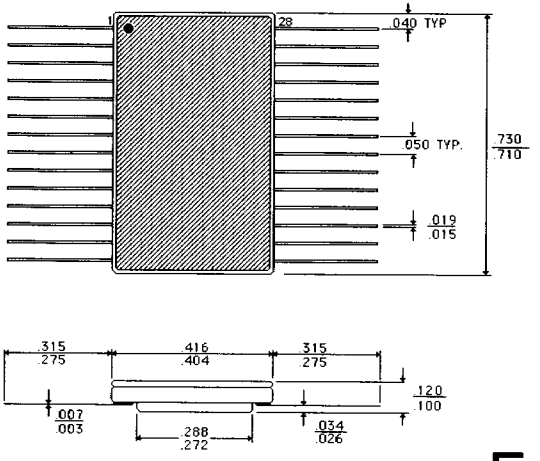
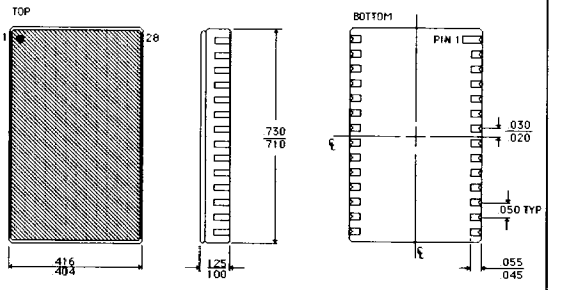
Package Dimension and Ordering Information

28 PIN CERAMIC FLATPACK, 400 MIL WIDE PACKAGE



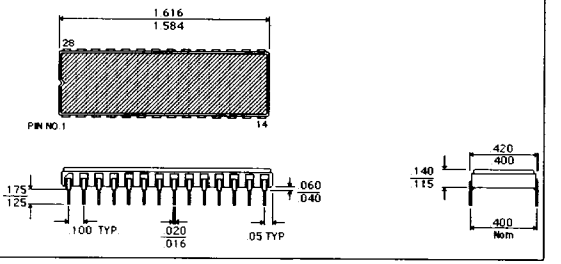
F

28 PIN LEADLESS CHIP CARRIER PACKAGE



L

28 PIN CERAMIC SIDEBRAZED
DUAL-IN-LINE PACKAGE
400 MIL WIDE



E

S256K4X-25XX

- C = Commercial Temperature Range (0°C to 70°C)
- I = Industrial Temperature Range (-40°C to 85°C)
- M = Military Temperature Range (-55°C to 125°C)

- C = 600 mil Ceramic Sidebrazed DIP
- D = 400 mil CERDIP
- E = 400 mil Ceramic Sidebrazed DIP
- T = 300 mil Ceramic Sidebrazed DIP
- P = 400 mil Plastic DIP
- F = Flatpack
- S = Ceramic SOJ
- J = Plastic SOJ
- L = Leadless Chip Carrier

- L suffix on base part number = Low Power Device