

10-bit D-type flip-flop; positive-edge trigger (3-State)

74ABT821

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jeduc JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT821 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT821 is a buffered 10-bit wide version of the 'ABT374/'ABT534 functions.

The 'ABT821 is a 10-bit, edge triggered register coupled to ten 3-State output

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	5.4	ns
C_{IN}	Input capacitance	$V_I = 0\text{V or } V_{CC}$	4	pF
C_{OUT}	Output capacitance	$V_I = 0\text{V or } V_{CC}$	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; $V_{CC} = 5.5\text{V}$	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT821N
24-pin plastic SOL	-40°C to +85°C	74ABT821D

buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable (\overline{OE}) control gates.

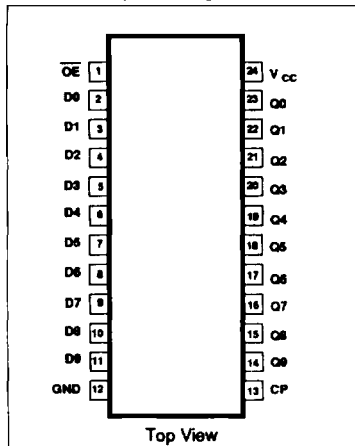
The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses,

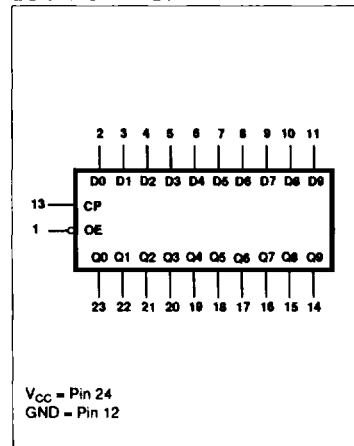
MOS memories, or MOS microprocessors.

The active Low Output Enable (\overline{OE}) controls all ten 3-State buffers independent of the register operation. When \overline{OE} is Low, the data in the register appears at the outputs. When \overline{OE} is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

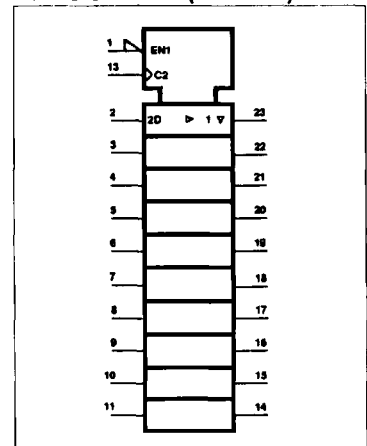
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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PIN DESCRIPTION

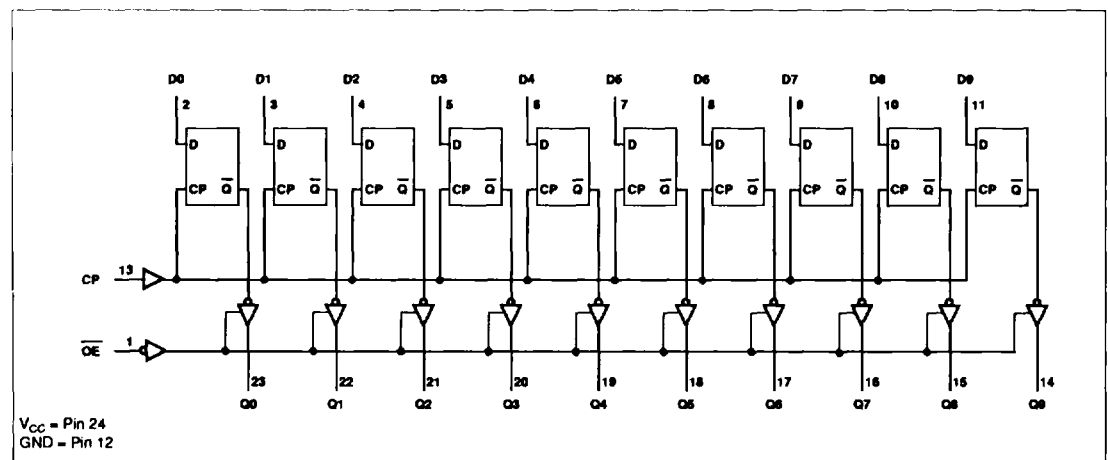
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	\overline{OE}	Output Enable input (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10, 11	D0 - D9	Data inputs
14, 15, 16, 17, 18, 19, 20, 21, 22, 23	Q0 - Q9	Data outputs
13	CP	Clock Pulse Input (active rising edge)
12	GND	Ground (0V)
24	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
\overline{OE}	CP	D _n		Q0 - Q9	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	≠	X	NC	NC	Hold
H	≠	X	NC	Z	Disable outputs
H	↑	D _n	D _n	Z	

- H = High voltage level
 h = High voltage level one set-up time prior to the Low-to-High clock transition
 L = Low voltage level
 l = Low voltage level one set-up time prior to the Low-to-High clock transition
 NC = No change
 X = Don't care
 Z = High impedance "off" state
 ↑ = Low-to-High clock transition
 ≠ = Not a Low-to-High clock transition

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	μA
I _O	Short-circuit output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-100	-180	-50	-180	mA
I _{OCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High; V _I = GND or V _{CC}		0.5	50		50	μA
I _{OCL}		V _{CC} = 5.5V; Outputs Low; V _I = GND or V _{CC}		30	38		38	mA
I _{Ocz}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	50		50	μA
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 5.5V; One input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.