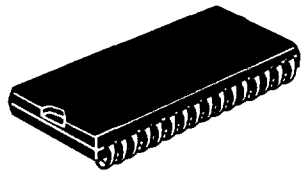
■ Features

- CMOS SRAM organized as 131,072 X 8bits
- Single+3.3V(± 0.3V) Power Supply
- High Speed Access time : 15/20/25ns
- Low power operation : 120mA (max.)

- Packages
  -32pin Plastic SOJ(400mil)



32pin Plastic SOJ(400mil)

■ Description

The N341026L is a high performance CMOS static RAM organized as 131,072 X 8bits.

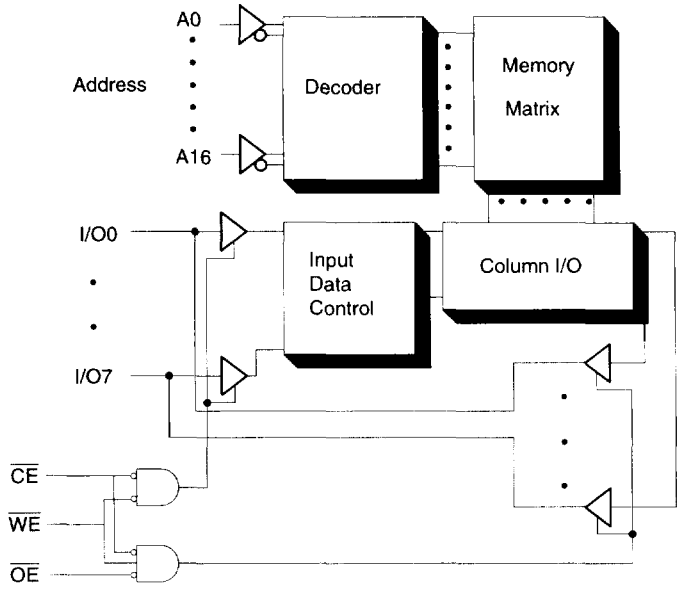
Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip select ($\overline{CE}$) inputs are both Low.

Reading is accomplished when $\overline{WE}$ is High and $\overline{CE}$ and the output enable ($\overline{OE}$) are both Low.

The N341026L operates from a single +3.3V power supply.

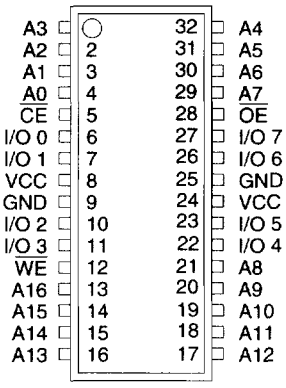
5

■ Functional Block Diagram



■ Pin Configuration

32 pin Plastic SOJ



■ Pin Description

SYMBOL	PIN NAME
A0-A16	Address input
I/O0-I/O7	Data input/output
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input
VCC	PowerSupply Pin(+3.3V)
GND	Ground Pin

■ Mode Selection Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	High	High impedance	Standby
Low	High	Low	Data out	Read
X	Low	Low	Data in	Write
High	High	Low	High impedance	Output disable

■ Absolute Maximum Ratings

Symbol	Rating	Min.	Max.	Unit
VCC	Supply Voltage	GND-0.5	4.6	V
VTERM	Terminal Voltage with Respect to GND	GND-0.5	VCC+0.5 (Max. 4.6)	V
TA	Operating Temperature	0	70	°C
TBIAS	Temperature Under Bias	-55	125	°C
TSTG	Storage Temperature	-55	125	°C

NOTICE
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ Recommended Operating Conditions

Recommended Operating Temperature and Supply Voltage

Ambient Temperature	GND	VCC
0°C to 70°C	0V	3.3V ± 0.3V

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	-	VCC + 0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

Note : VIL(min) = -2.0V for pulse width less than 20ns.

■ Capacitance

(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

5

■ DC Electrical Characteristics

(Vcc = 3.3V ± 0.3V, TA=0 to +70°C)

Symbol	.Parameter	N341026L -15	N341026L -20	N341026L -25	Unit
ICC	Dynamic Operating Current $\overline{CE}$ ≤ VIL, VCC = max, f = fmax, IOUT = 0mA, VIN ≥ VIH or ≤ VIL	120	110	100	mA
ISB	Standby Power Supply Current (TTL level) $\overline{CE}$ ≥ VIH, VCC = max, f = fmax, VIN ≥ VIH or ≤ VIL	30	30	30	mA
ISB1	Full Standby Power Supply Current (CMOS level) $\overline{CE}$ ≥ VCC-0.2V, f = 0, VIN ≤ 0.2V or ≥ VCC-0.2V	2	2	2	mA

DC Electrical Characteristics(1)

(Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I ILI I	Input Leakage Current	VCC = max, VIN = GND to VCC	-	2	µA
I ILO I	Output Leakage Current	VCC = max, $\overline{CE}$ ≥ VIH, VOUT = GND to VCC	-	2	µA
VOL	Output Low Voltage	IOL = 4mA, VCC = min	-	0.4	V
VOH	Output High Voltage	IOH = -4mA, VCC = min	2.4		V

■ AC Test Conditions

Input pulse levels	GND to 3V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See figure 1 and 2

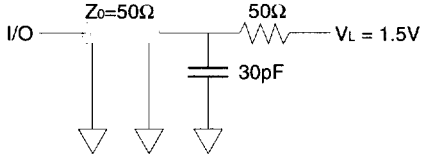


Figure 1. Output Load Equivalent

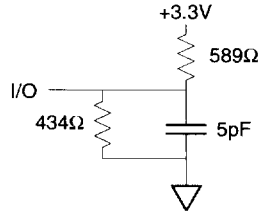


Figure 2. Output Load Equivalent
(for tLZCE, tHZCE, tLZWE, tHZWE, tLZOE, tHZOE)

■ AC Electrical Characteristics

(Vcc = 3.3V ± 0.3V, TA=0°C to 70°C)

Description	Symbol	N341026L-15		N341026L-20		N341026L-25		Unit
Read Cycle		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle time	t_{RC}	15		20		25		ns
Address access time	t_{AA}		15		20		25	ns
Chip enable access time	t_{ACE}		15		20		25	ns
Output hold from address change	t_{OH}	3		3		3		ns
Chip enable to output in low-Z	t_{LZCE}	5		5		5		ns
Chip disable to output in high-Z	t_{HZCE}		7		8		10	ns
Chip enable to power up time	t_{PU}	0		0		0		ns
Chip disable to power down time	t_{PD}		15		20		25	ns
Output enable access time	t_{AOE}		6		6		8	ns
Output enable to output in low-Z	t_{LZOE}	0		0		0		ns
Output disable to output in high-Z	t_{HZOE}		6		6		8	ns

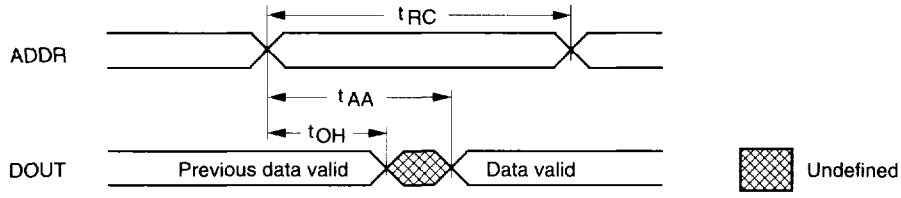
(Vcc = 3.3V ± 0.3V, TA=0°C to 70°C)

Description	Symbol	N341026L-15		N341026L-20		N341026L-25		Unit
Write Cycle		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle time	tWC	15		20		25		ns
Chip enable to end of write	tCW	11		13		15		ns
Address valid to end of write	tAW	11		13		15		ns
Address set-up time	tAS	0		0		0		ns
Address hold from end of write	tAH	0		0		0		ns
Write pulse width ($\overline{OE} \geq$ VIH)	tWP1	11		13		15		ns
Write pulse width ($\overline{OE} \leq$ VIL)	tWP2	12		14		15		ns
Data set-up time	tDS	7		8		10		ns
Data hold time	tDH	0		0		0		ns
Write disable to output in low-Z	tLZWE	0		0		0		ns
Write enable to output in high-Z	tHZWE		7		8		10	ns

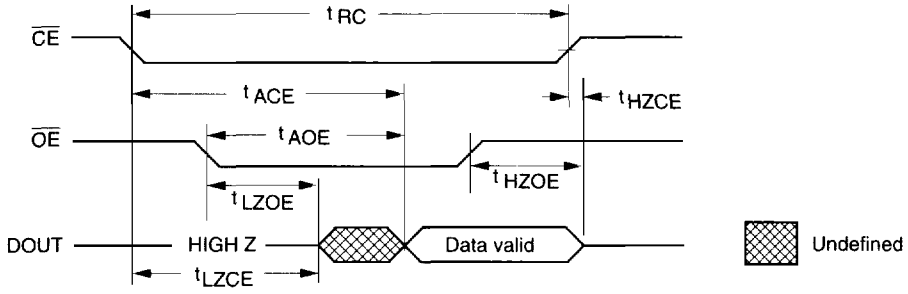
5

■ AC Timing Waveform

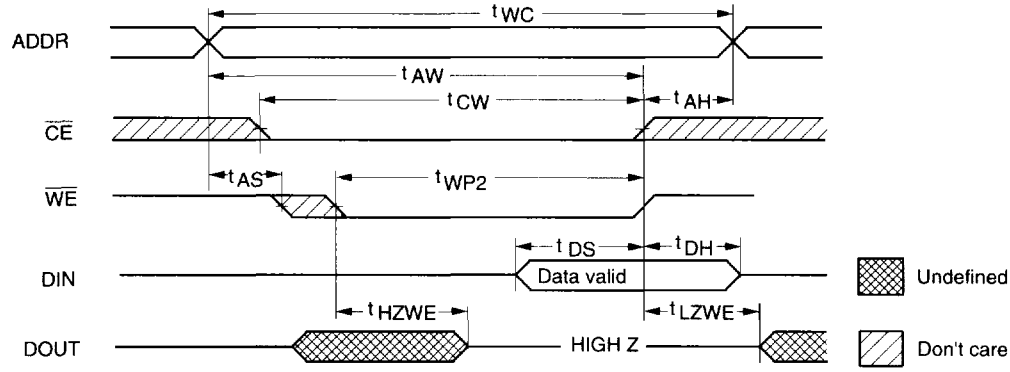
Read Cycle No.1



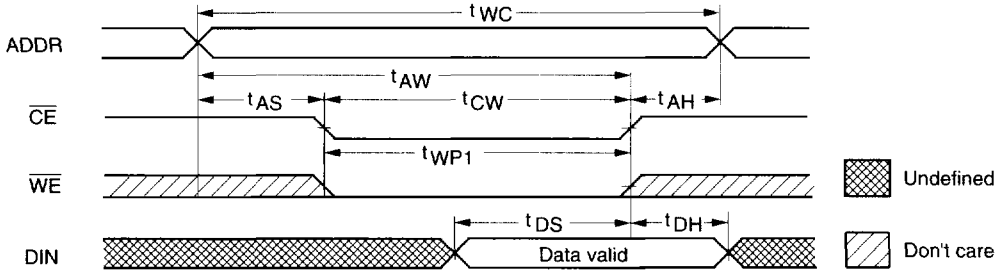
Read Cycle No.2



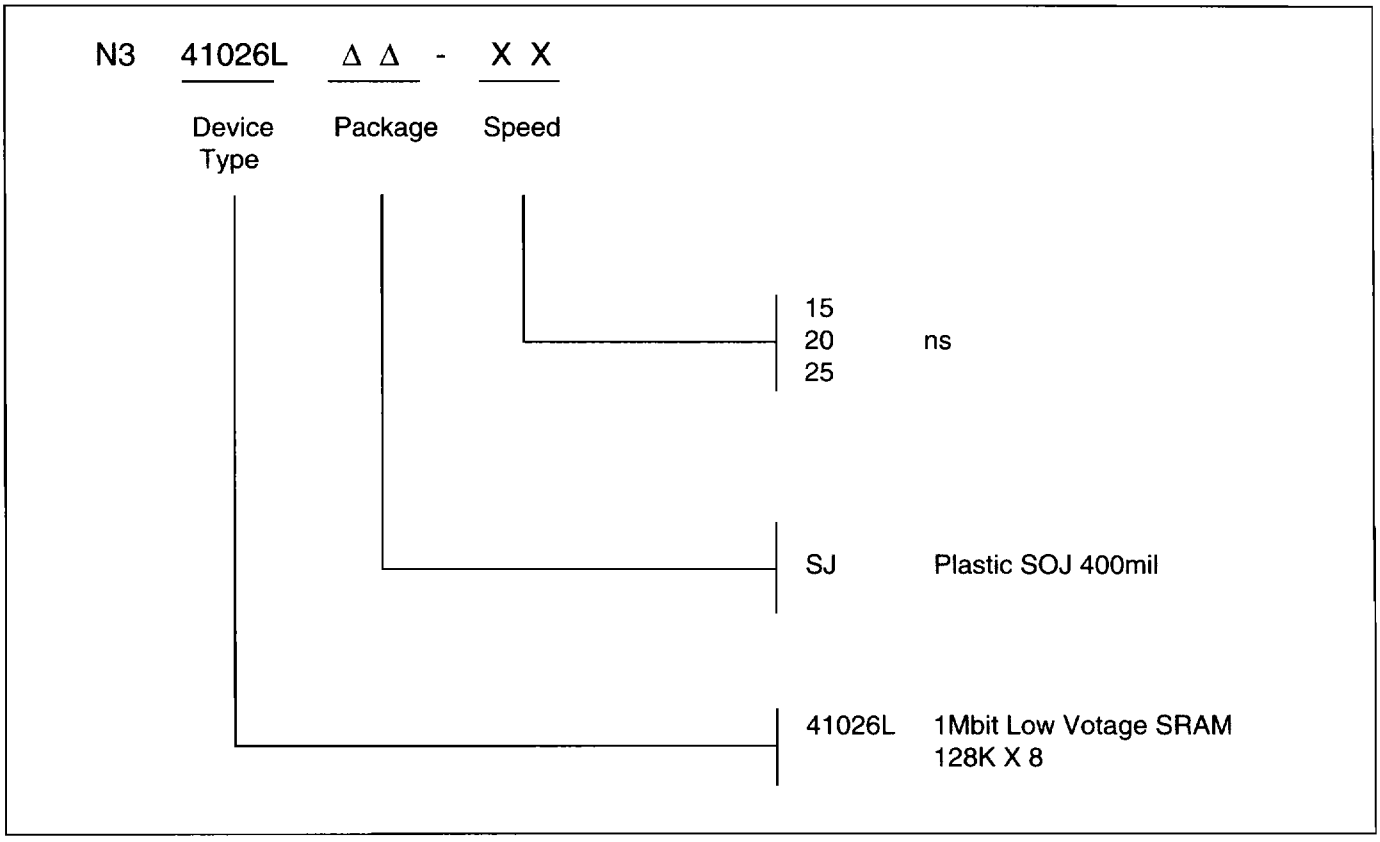
Write Cycle No.1(Write Enable Controlled)



Write Cycle No.2(Chip Enable Controlled)



■ Ordering Information



PART NO.	Access Time (ns)	Operating Current (mA)	Power down Standby Current (mA)	Package
N341026LSJ-15	15	120	30	32pin Plastic SOJ
N341026LSJ-20	20	110	30	32pin Plastic SOJ
N341026LSJ-25	25	100	30	32pin Plastic SOJ