National Semiconductor

74VHC245 • 74VHCT245
Octal Bidirectional Transceiver with TRI-STATE® Outputs

General Description

The VHC/VHCT245 is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The 'VHC245 is intended for bidirectional asynchronous communication between data busses. The direction of data transmission is determined by the level of the T/$\overline{R}$ input. The enable input can be used to disable the device so that the busses are effectively isolated. All inputs are equipped with protection circuits against static discharge.

Features

- High Noise Immunity:
  VHC $V_{NIH} = V_{NIL} = 28\%\ V_{CC}$ (Min)
  VHCT $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- Power Down Protection:
  VHC Inputs Only
  VHCT Inputs and Outputs
- Low Noise:
  VHC $V_{OLP} = 0.9V$ (typ)
  VHCT $V_{OLP} = 1.1V$ (typ)
- Low Power Dissipation:
  $I_{CC} = 4\ \mu A$ (Max) @ $T_a = 25°C$
- Balanced Propagation Delays: $t_{pLH} \cong t_{pHL}$
- Pin and Function Compatible with 74HC/HCT245

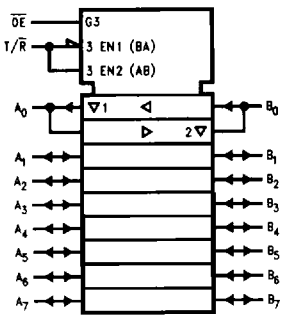
Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC245M	M20B	20 Lead Molded JEDEC SOIC
74VHC245SJ	M20D	20 Lead Molded EIAJ SOIC
74VHC245MSC	MSC20	20 Lead Molded EIAJ Type 1 SSOP
74VHC245MTC	MTC20	20 Lead Molded JEDEC Type 1 TSSOP
74VHC245N	N20A	20 Lead Molded DIP
74VHCT245M	M20B	20 Lead Molded JEDEC SOIC
74VHCT245SJ	M20D	20 Lead Molded EIAJ SOIC
74VHCT245MTC	MTC20	20 Lead Molded JEDEC Type 1 TSSOP
74VHCT245N	N20A	20 Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
EIAJ Type 1 SSOP available on Tape and Reel only, order MSCX.

Logic Symbol

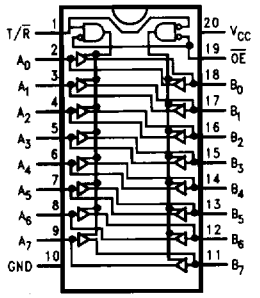
IEEE/IEC



TL/F/11520–2

Connection Diagram

Pin Assignment for DIP, SSOP, TSSOP and SOIC



TL/F/11520–3

Pin Description

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN}) ($T/\overline{R}$, $\overline{OE}$)	−0.5V to 7.0V
DC Output Voltage (V_{OUT})	
VHC	−0.5V to V_{CC} + 0.5V
VHCT*	−0.5V to 7.0V
Input Diode Current (I_{IK}) ($T/\overline{R}$, $\overline{OE}$)	−20 mA
Output Diode Current (I_{OK})	
(VHC)	±20 mA
(VHCT)	−20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

*V_{OUT} > V_{CC} only if output is in H or Z state.

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	
VHC	2.0V to 5.5V
VHCT*	4.5V to 5.5V
Input Voltage (V_{IN})($T/\overline{R}$, $\overline{OE}$)	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	
74 VHC/VHCT	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V (VHC only)	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C			74VHC T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0	1.50			1.50		V		
		3.0–5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	Low Level Input Voltage	2.0			0.50		0.50	V		
		3.0–5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		4.5	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{CC} or GND; V_{OUT} = V_{CC} or GND; V_{IN} $\overline{OE}$ = V_{IH} or V_{IL}	
I_{IN} ($T/\overline{R}$, $\overline{OE}$)	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V_{CC} (V)	74VHC $T_A = 25°C$ Typ	74VHC $T_A = 25°C$ Limits	Units	Conditions	Fig. No.
*V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.9	1.2	V	C_L = 50 pF	2-11, 12
*V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.9	−1.2	V	C_L = 50 pF	2-11, 12
*V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF	2-11, 12
*V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF	2-11, 12

*Parameter guaranteed by design.

DC Characteristics for 'VHCT Family Devices

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$ Min	Typ	Max	74VHCT $T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	
V_{IH}	High Level Input Voltage	4.5 5.5	2.0 2.0			2.0 2.0		V		
V_{IL}	Low Level Input Voltage	4.5 5.5			0.8 0.8		0.8 0.8	V		
V_{OH}	High Level Output Voltage	4.5	3.15	3.65		3.15		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		4.5	2.5			2.4		V		I_{OH} = −8 mA
V_{OL}	Low Level Output Voltage	4.5		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		4.5			0.36		0.44	V		I_{OL} = 8 mA
I_{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25		±2.5	μA	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC} or GND V_{IN} $\overline{OE}$ = V_{IH} or V_{IL}	
I_{IN} ($T/\overline{R}$, $\overline{OE}$)	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	V_{IN} = V_{CC} or GND	
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35		1.50	mA	V_{IN} = 3.4V Other Inputs = V_{CC} or GND	
I_{OPD}	Output Leakage Current (Power Down State)	0.0			+0.5		+5.0	μA	V_{OUT} = 5.5V	

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DC Characteristics for 'VHCT Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V_{CC} (V)	74VHCT T_A = 25°C Typ	74VHCT T_A = 25°C Limits	Units	Conditions	Fig. No.
V_{OLP}*	Quiet Output Maximum Dynamic V_{OL}		1.1	1.6	V	C_L = 50 pF	2-11, 12
V_{OLV}*	Quiet Output Minimum Dynamic V_{OL}		−1.1	−1.6	V	C_L = 50 pF	2-11, 12
V_{IHD}*	Minimum High Level Dynamic Input Voltage			2.0	V	C_L = 50 pF	2-11, 12
V_{ILD}*	Maximum Low Level Dynamic Input Voltage			0.8	V	C_L = 50 pF	2-11, 12

*Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHC T_A = 25°C Min	Typ	Max	74VHC T_A = −40°C to +85°C Min	Max	Units	Conditions		Fig. No.
t_{PLH} t_{PHL}	Propagation Delay Time	3.3 ± 0.3		5.8	8.4	1.0	10.0	ns		C_L = 15 pF	2-5
				8.3	11.9	1.0	13.5			C_L = 50 pF	
		5.0 ± 0.5		4.0	5.5	1.0	6.5	ns		C_L = 15 pF	2-5
				5.5	7.5	1.0	8.5			C_L = 50 pF	
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	3.3 ± 0.3		8.5	13.2	1.0	15.5	ns	R_L = 1 kΩ	C_L = 15 pF	2-7, 8
				11.0	16.7	1.0	19.0			C_L = 50 pF	
		5.0 ± 0.5		5.8	8.5	1.0	10.0	ns		C_L = 15 pF	2-7, 8
				7.3	10.6	1.0	12.0			C_L = 50 pF	
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	3.3 ± 0.3		11.5	15.8	1.0	18.0	ns	R_L = 1 kΩ	C_L = 50 pF	2-7, 8
		5.0 ± 0.5		7.0	9.7	1.0	11.0			C_L = 50 pF	
t_{OSLH} t_{OSHL}	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 1)	C_L = 50 pF	
		5.0 ± 0.5			1.0		1.0			C_L = 50 pF	
C_{IN} ($T/\overline{R}$, $\overline{OE}$)	Input Capacitance			4	10		10	pF	V_{CC} = Open		
$C_{I/O}$	Output Capacitance			8				pF	V_{CC} = 5.0V		
C_{PD}	Power Dissipation Capacitance			21				pF	(Note 2)		

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/8 (per Bit).

AC Electrical Characteristics for 'VHCT Family Devices: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74VHCT $T_A = 25°C$			74VHCT $T_A = -40°C$ to $+85°C$		Units	Conditions		Fig. No.
			Min	Typ	Max	Min	Max				
t_{PLH} t_{PHL}	Propagation Delay Time	5.0 ±0.5		4.5	7.7	1.0	8.5	ns		C_L = 15 pF	2-5
				5.3	8.7	1.0	9.5			C_L = 50 pF	
t_{PZL} t_{PZH}	TRI-STATE Output Enable Time	5.0 ±0.5		8.9	13.8	1.0	15.0	ns	R_L = 1 kΩ	C_L = 15 pF	2-7, 8
				9.7	14.8	1.0	16.0			C_L = 50 pF	
t_{PLZ} t_{PHZ}	TRI-STATE Output Disable Time	5.0 ±0.5		10.0	15.4	1.0	16.5	ns	R_L = 1 kΩ	C_L = 50 pF	2-7, 8
t_{OSLH} t_{OSHL}	Output to Output Skew	5.0 ±0.5			1.0		1.0	ns	(Note 1)	C_L = 50 pF	
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open		
$C_{I/O}$	Output Capacitance			9				pF	V_{CC} = 5.0V		
C_{PD}	Power Dissipation Capacitance			23				pF	(Note 2)		

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per Bit).