FEATURES:

- 128K x 8 Advanced High-Speed BiCMOS Static RAM
- Equal access and cycle times
  — Commercial: 15/17ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
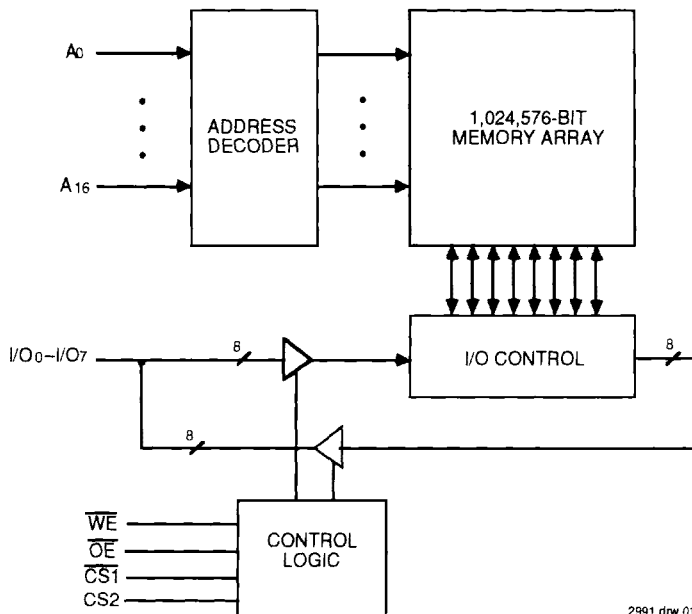- Available in 32-pin Plastic DIP and SOJ packages

DESCRIPTION:

The IDT71B024 is a 1,024,576-bit high-speed Static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71B024 has an output enable pin which operates as fast as 8ns, with address access times as fast as 15ns available. All bidirectional inputs and outputs of the IDT71B024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refresh are required for operation.

The IDT71B024 is packaged in a 32-pin 400 mil Plastic DIP and 32-pin 400 mil Plastic SOJ.
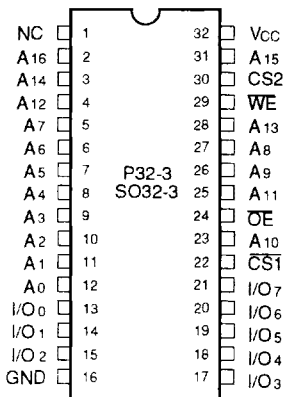
FUNCTIONAL BLOCK DIAGRAM

2991 drw 01

COMMERCIAL TEMPERATURE RANGE   **SEPTEMBER 1992**

PIN CONFIGURATION

NC	1		32	Vcc
A16	2		31	A15
A14	3		30	CS2
A12	4		29	$\overline{WE}$
A7	5		28	A13
A6	6		27	A8
A5	7	P32-3	26	A9
A4	8	SO32-3	25	A11
A3	9		24	$\overline{OE}$
A2	10		23	A10
A1	11		22	$\overline{CS1}$
A0	12		21	I/O7
I/O0	13		20	I/O6
I/O1	14		19	I/O5
I/O2	15		18	I/O4
GND	16		17	I/O3

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DIP/SOJ
TOP VIEW

TRUTH TABLE[1,2]

INPUTS				I/O	FUNCTION
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$		
X	H	X	X	High-Z	Deselected–Standby (ISB)
X	VHC[3]	X	X	High-Z	Deselected–Standby (ISB1)
X	X	L	X	High-Z	Deselected–Standby (ISB)
X	X	VLC[3]	X	High-Z	Deselected–Standby (ISB1)
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

2991 tbl 01

NOTES:
1. H = VIH, L = VIL, X = Don't care.
2. VLC = 0.2V, VHC = Vcc -0.2V.
3. Other inputs ≥VHC or ≤VLC

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Unit
VTERM[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	−55 to +125	°C
TSTG	Storage Temperature	−55 to +125	°C
PT	Power Dissipation	1.25	W
IOUT	DC Output Current	50	mA

NOTES: 2991 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
CI/O	I/O Capacitance	VOUT = 3dV	7	pF

NOTE: 2991 tbl 03
1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	Vcc+0.5	V
VIL	Input Low Voltage	−0.5[1]	—	0.8	V

NOTE: 2991 tbl 04
1. VIL (min.) = −1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B024 Min.	IDT71B024 Max.	Unit
|ILI|	Input Leakage Current	Vcc = Max., VIN = GND to Vcc	—	5	μA
|ILO|	Output Leakage Current	Vcc = Max., $\overline{CS1}$ = VIH, CS2 = VIL, VOUT = GND to Vcc	—	5	μA
VOL	Output Low Voltage	IOL = 8mA, Vcc = Min.	—	0.4	V
VOH	Output High Voltage	IOH = −4mA, Vcc = Min.	2.4	—	V

2991 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

($V_{CC} = 5.0V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$)

|		71B024S15		71B024S17		
Symbol	Parameter	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	200	—	195	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	55	—	50	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC} or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0[2], V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	40	—	40	—	mA

2991 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
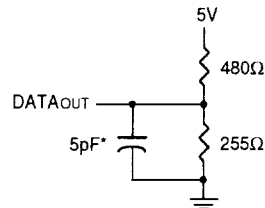
AC TEST CONDITIONS

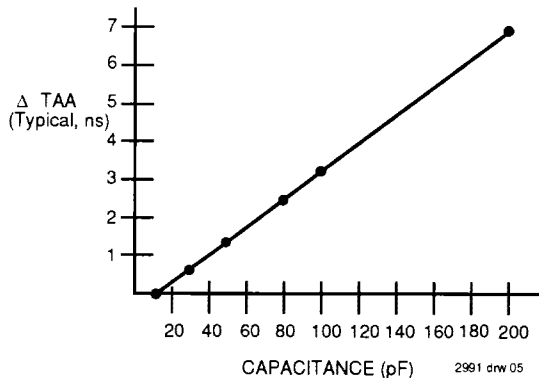| Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, & 3

2991 tbl 07
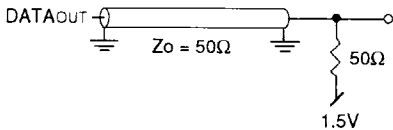
Figure 1. AC Test Load

*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

Symbol	Parameter	71B024S15		71B024S17		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
tRC	Read Cycle Time	15	—	17	—	ns
tAA	Address Access Time	—	15	—	17	ns
tACS	Chip Select Access Time	—	15	—	17	ns
tCLZ[1]	Chip Select to Output in Low-Z	3	—	3	—	ns
tCHZ[1]	Chip Deselect to Output in High-Z	0	8	0	8	ns
tOE	Output Enable to Output Valid	—	8	—	9	ns
tOLZ[1]	Output Enable to Output in Low-Z	0	—	0	—	ns
tOHZ[1]	Output Disable to Output in High-Z	0	7	0	7	ns
tOH	Output Hold from Address Change	4	—	4	—	ns
tPU[1]	Chip Select to Power-Up Time	0	—	0	—	ns
tPD[1]	Chip Deselect to Power-Down Time	—	15	—	17	ns
Write Cycle						
tWC	Write Cycle Time	15	—	17	—	ns
tAW	Address Valid to End-of-Write	12	—	12	—	ns
tCW	Chip Select to End-of-Write	12	—	12	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	8	—	9	—	ns
tDH	Data Hold Time	0	—	0	—	ns
tOW[1]	Output Active from End-of-Write	3	—	3	—	ns
tWHZ[1]	Write Enable to Output in High-Z	0	8	0	8	ns

NOTE:

2991 tbl 08
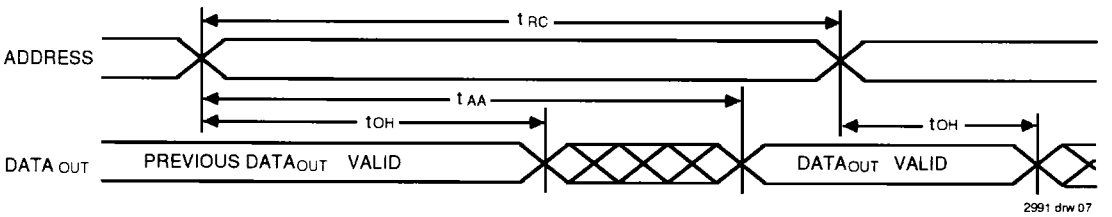
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
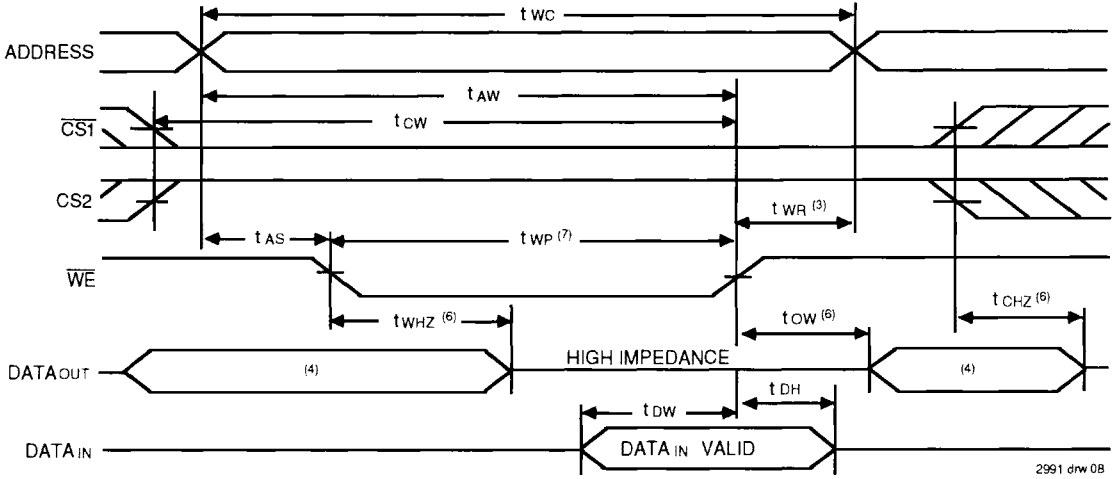
TIMING WAVEFORM OF READ CYCLE NO. 1[1]

2991 drw 06
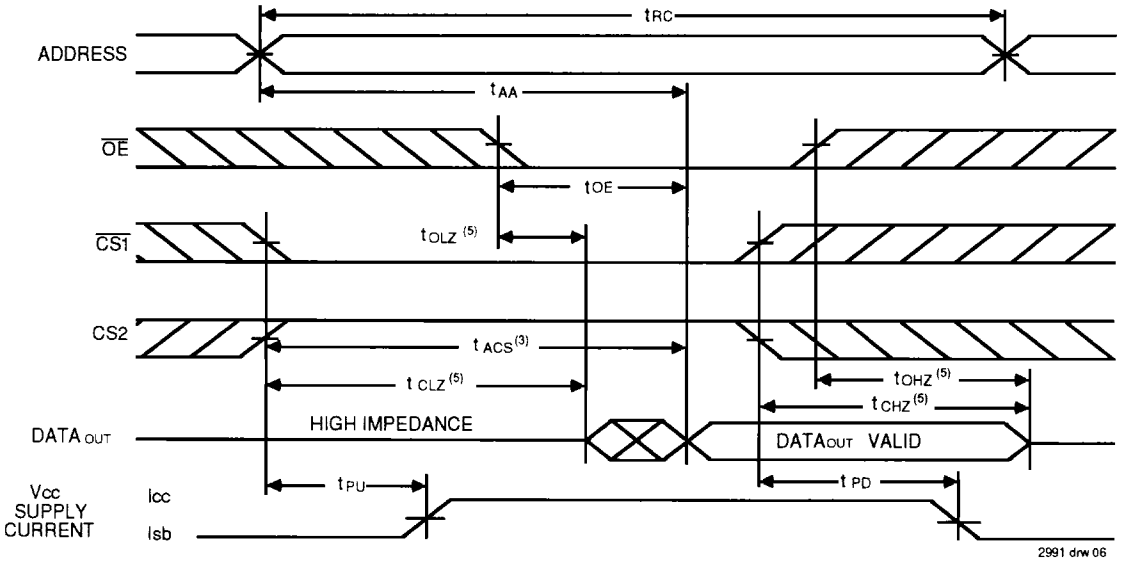
## TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]

2991 drw 07

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NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 5, 7]

2991 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)[1, 2, 5]
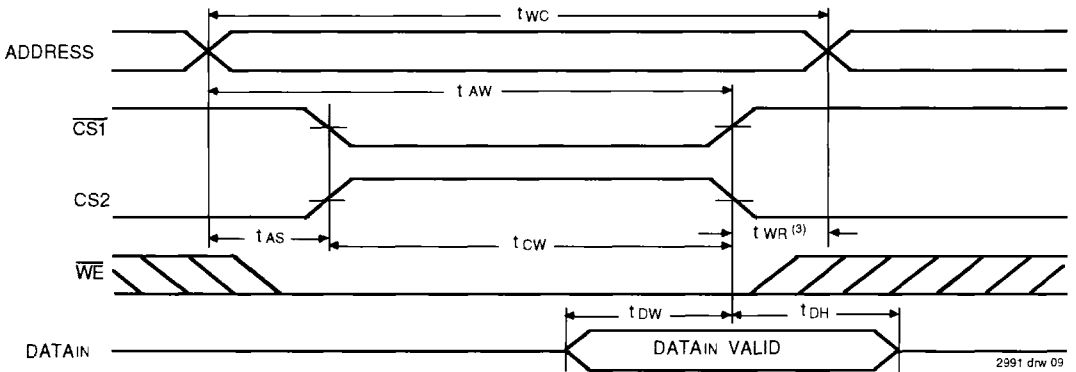
2991 drw 09

NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state. $\overline{CS1}$ and CS2 must both be active during the t_{CW} write period.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.

ORDERING INFORMATION

IDT   71B024   S   XX   X   X

Device Type   Power   Speed   Package   Process/ Temperature Range

Blank	Commercial (0°C to +70°C)
P	400-mil Plastic DIP (P32-3)
Y	400-mil SOJ (SO32-3)
15	Commercial Only ⎫ Speed in Nanoseconds
17	Commercial Only ⎭

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