Electrical Characteristics and Recommended AC Operating Conditions (Notes 6,7,8)

SYMBOL	PARAMETER	-60		-70		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	ns	9, 13, 14
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	ns	9, 13
t_{AA}	Access Time from Column Address	-	30	-	35	ns	9, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11

Electrical Characteristics and Recommended AC Operating Conditions (Cont)

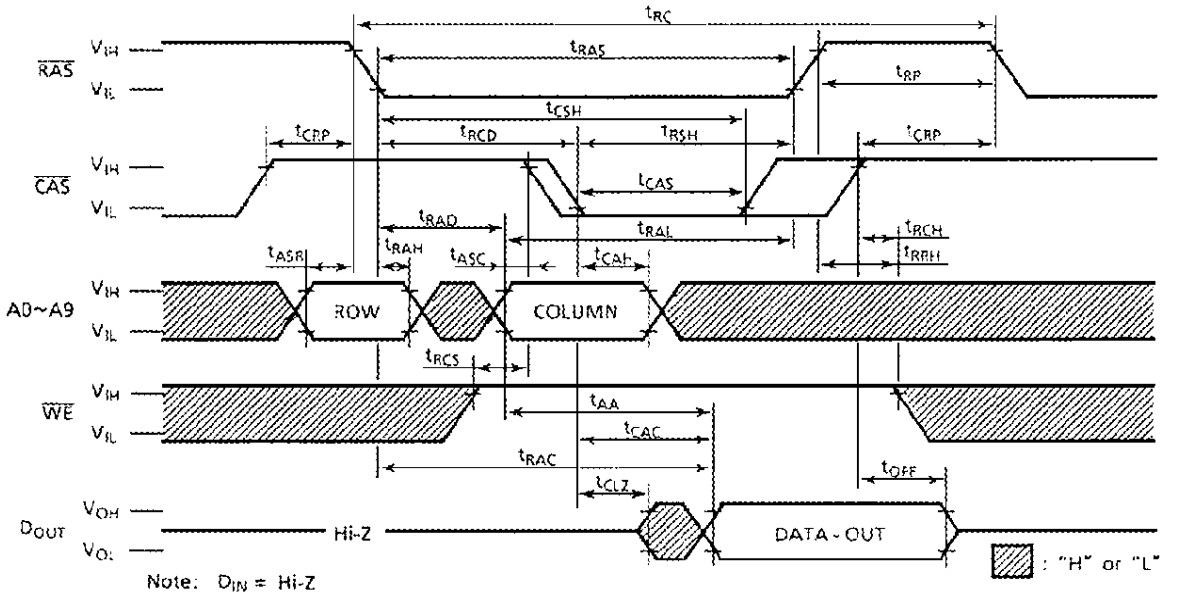
SYMBOL	PARAMETER	-60		-70		UNIT	NOTES
		MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	10	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	
t_{DH}	Data Hold Time	10	-	15	-	ns	
t_{REF}	Refresh Period	-	16	-	16	ms	
t_{REF}	Refresh Period (Self Refresh)	-	64	-	64	ms	
t_{REF}	Refresh Period (Self Refresh)	-	128	-	128	ms	15
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	-	30	-	ns	

Notes:

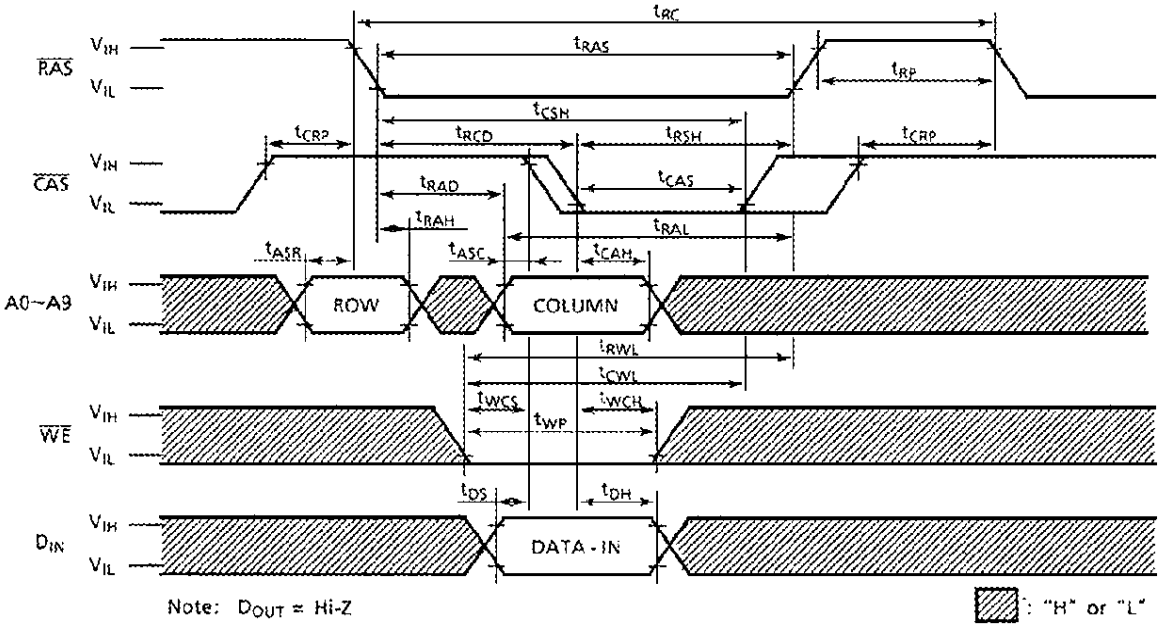
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS}$=V_{IL}. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs (3.3V type = 500μs) is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. When the internal refresh counter is used, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. 5V type: This parameter is measured with a load equivalent to 2 TTL loads and 100pF.
   3.3V type: This parameter is measured with a load equivalent to 1 LVTTL load and 100pF at V_{OH}=2.0V (I_{OUT}= -2mA), V_{OL}=0.8V (I_{OUT}=2mA).
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; if neither of the above sets of condition is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
15. This specification is insured under the condition of 0≤Ta≤60°C.

Timing Waveforms

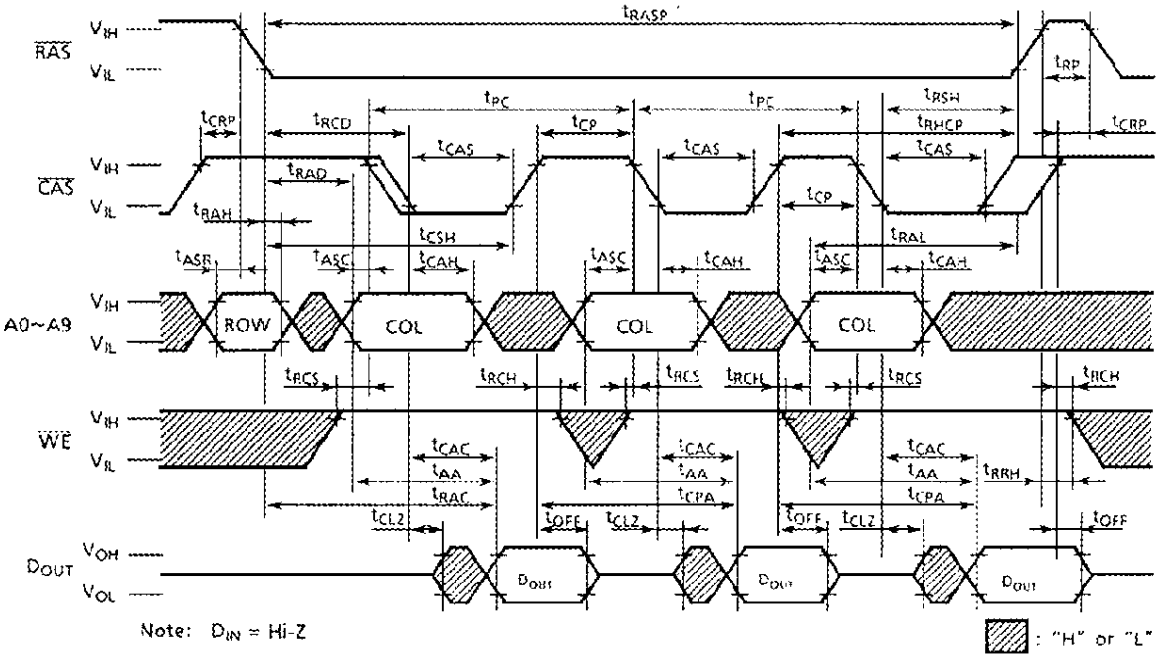
Read Cycle



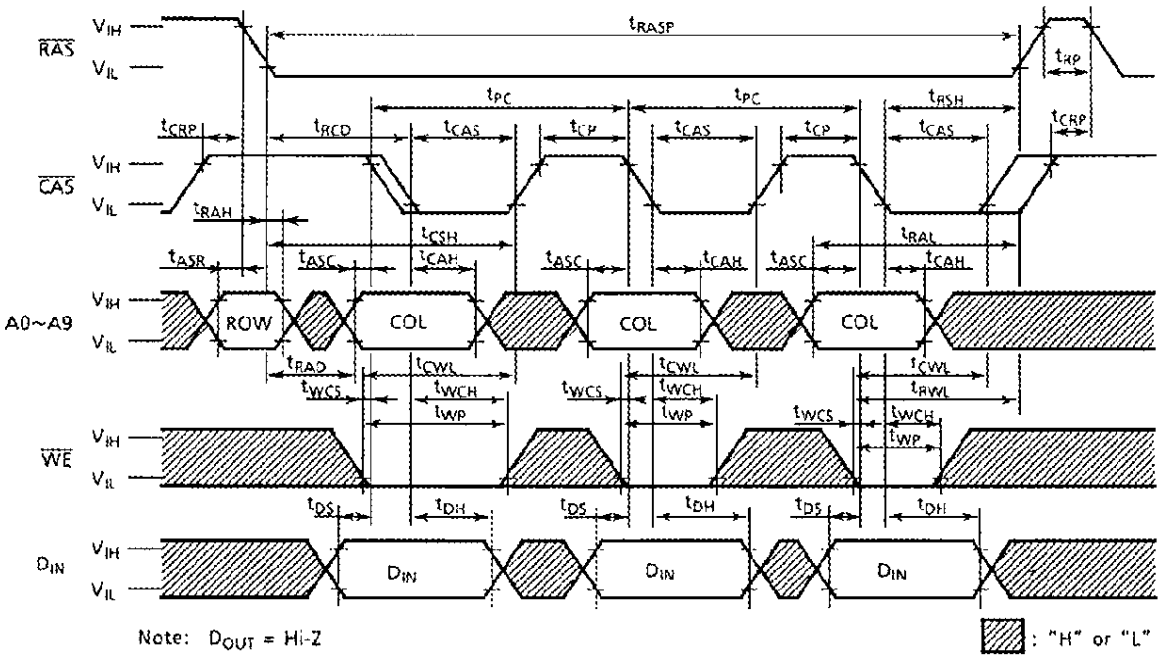
Write Cycle (Early Write)



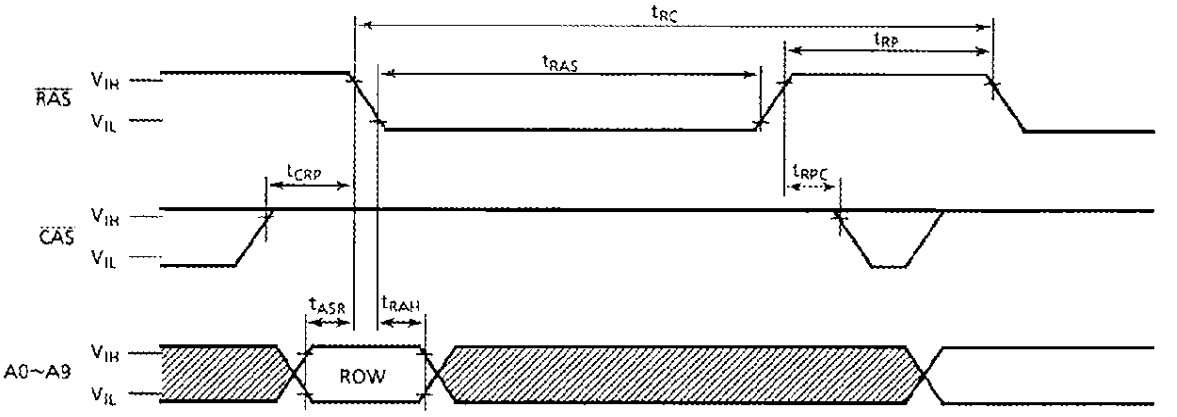
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)



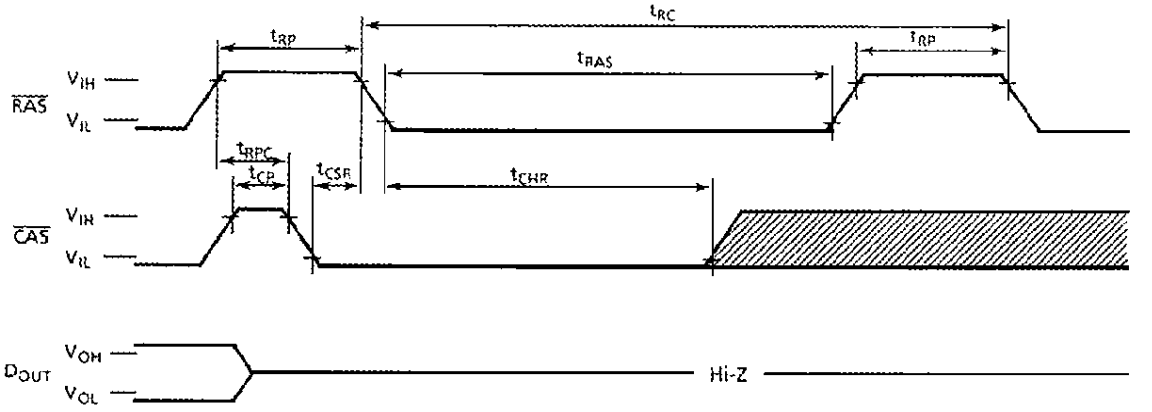
$\overline{RAS}$ Only Refresh Cycle



Note: $\overline{WE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = Hi-Z

▨ : "H" or "L"

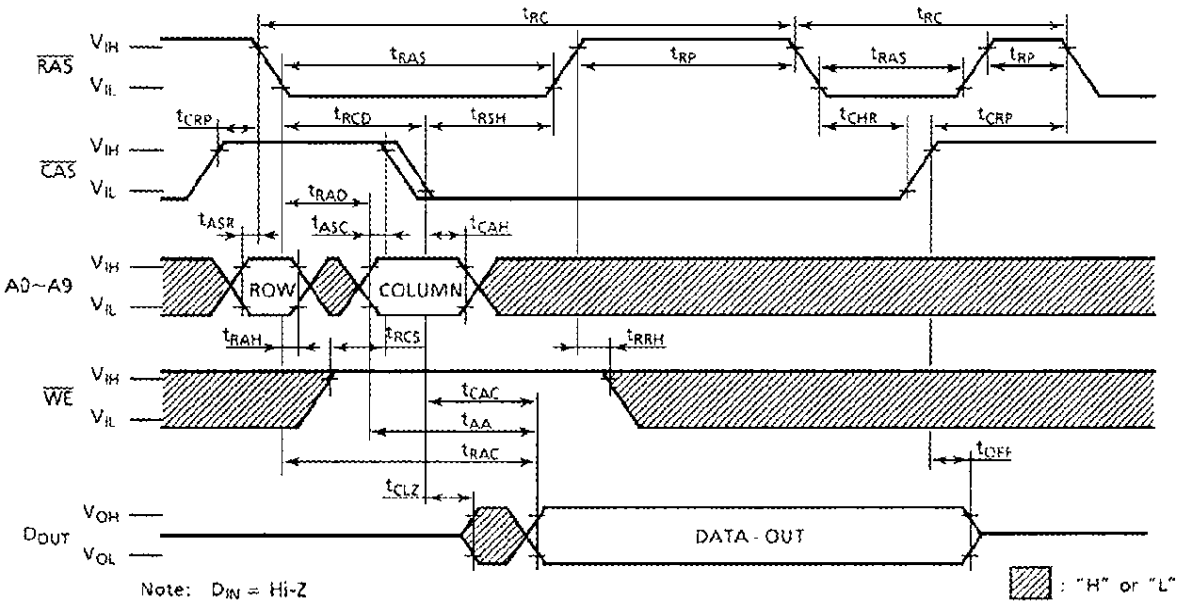
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



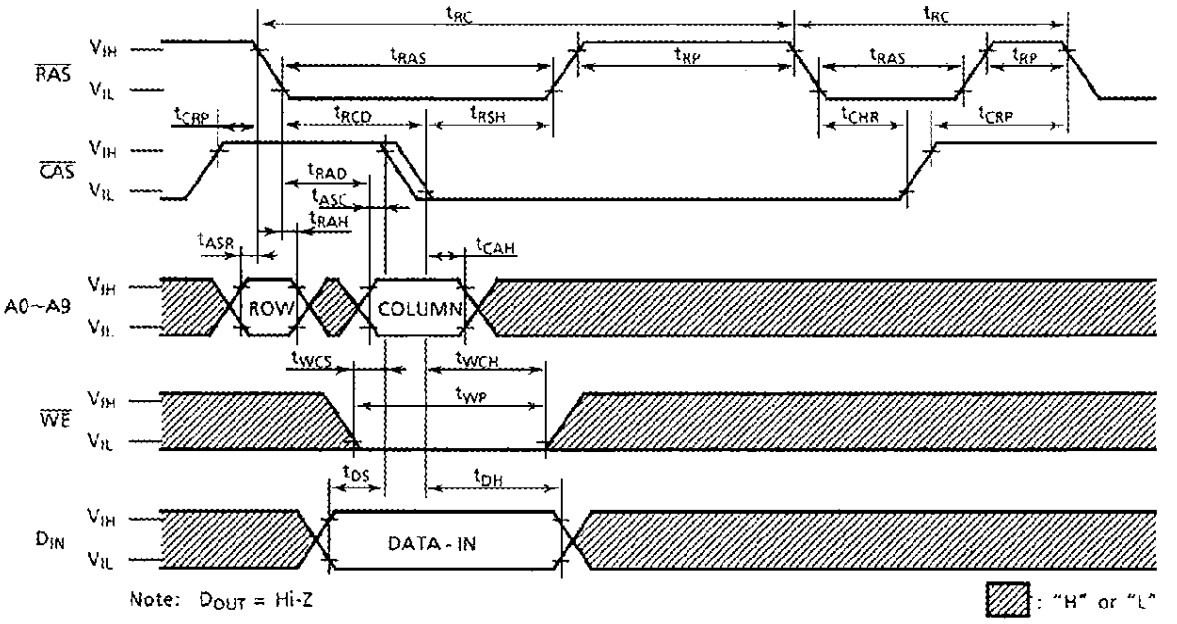
Note: $\overline{WE}$, A0~A9 = "H" or "L"
D_{IN} = Don't Care.

▨ : "H" or "L"

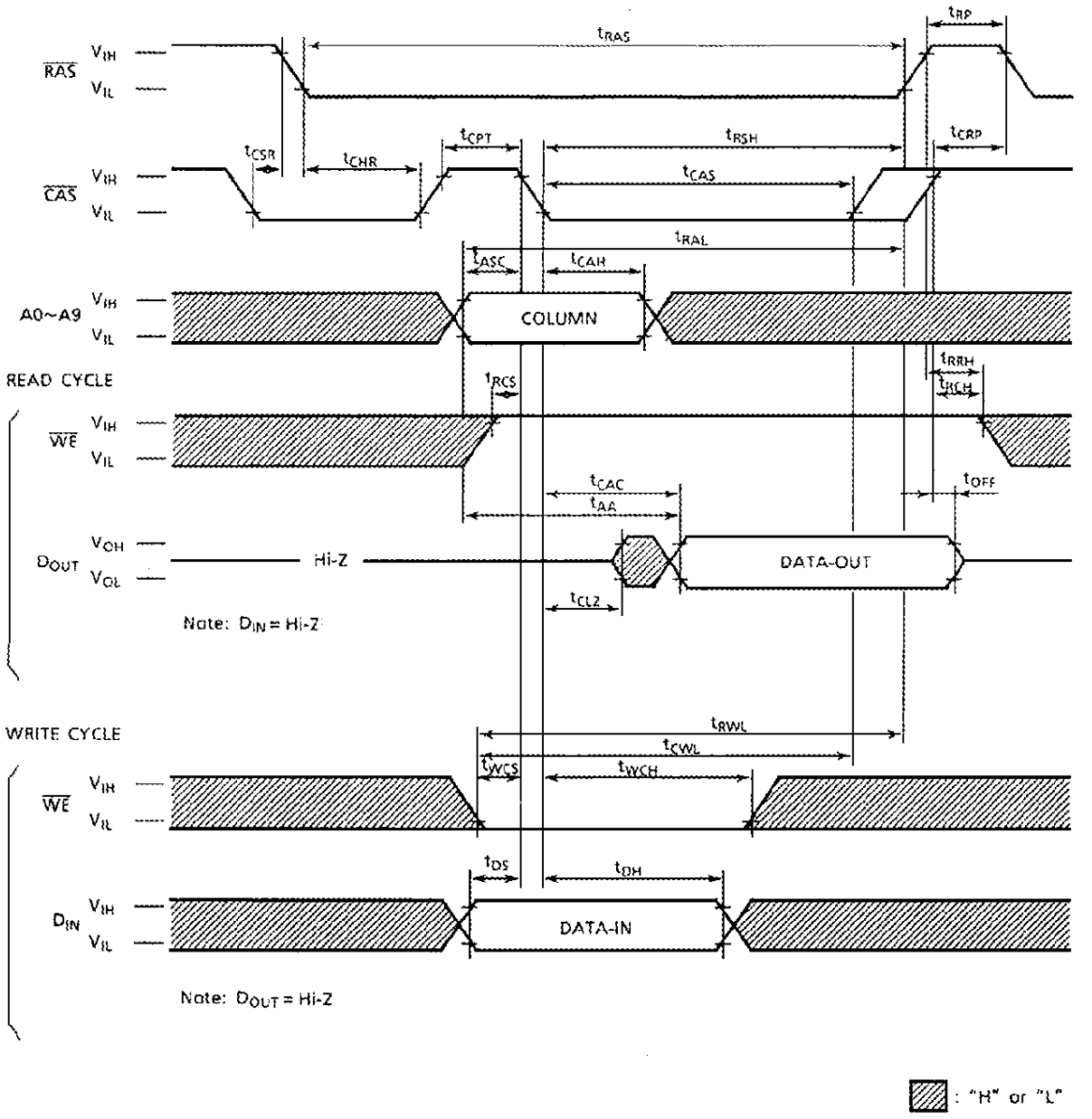
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle



Back to Memory