# HYBRID

## MEMORY PRODUCTS LIMITED

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**128K x 8 SRAM**

**MSM8128X-85/10/12**

Issue 2.2 : March 1992

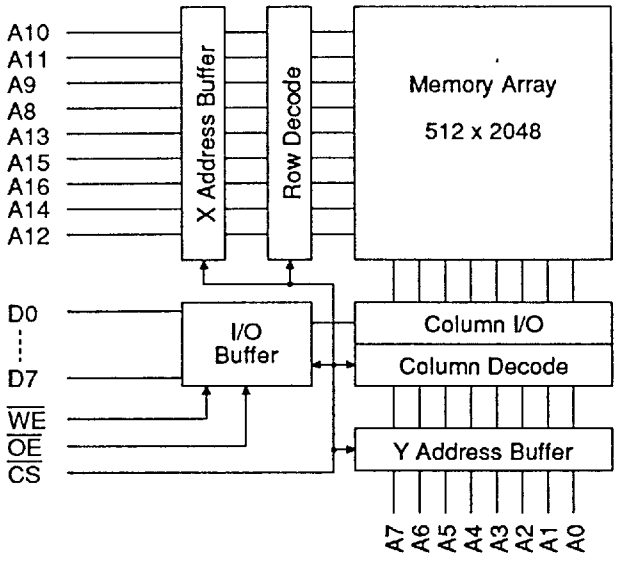
**PRELIMINARY**

131,072 x 8 CMOS High Speed Static RAM

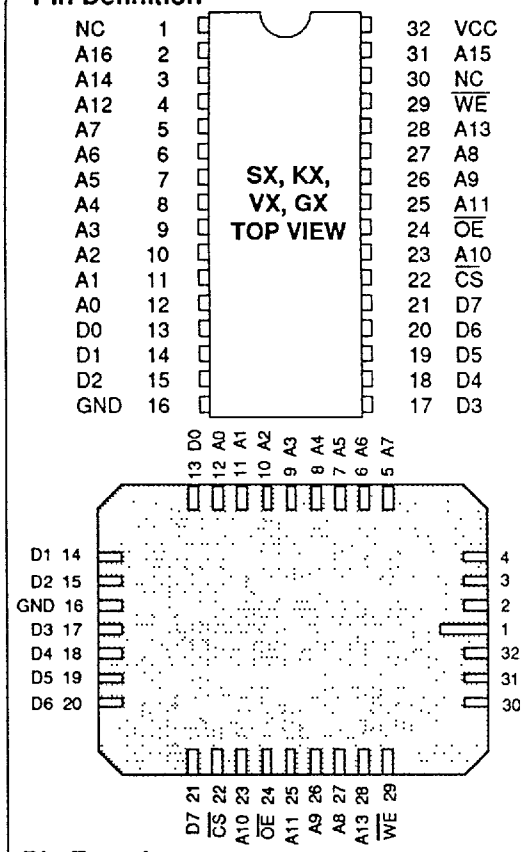
### Features

Fast Access Times of 85/100/120 ns
JEDEC ASIC 32 pin DIL footprint
VIL™ High Density Package Available
Low Power Standby 3mW (typ.)
10µW (typ.)(suffix - L)
Low Power Operation 75mW(typ.)
2.0V Data Retention Mode
Completely Static Operation
Equal Access and Cycle Times
Battery back-up capability
Directly TTL compatible
Common data inputs & outputs
May be processed in accordance with MIL-STD-883C

### Block Diagram




### Pin Definition




### Pin Functions

| | |
|---|---|
| **A0-A16** | Address Inputs |
| **D0-7** | Data Input/Output |
| **$\overline{CS}$** | Chip Select |
| **$\overline{OE}$** | Output Enable |
| **$\overline{WE}$** | Write Enable |
| **NC** | No Connect |
| **$V_{CC}$** | Power (+5V) |
| **GND** | Ground |

### Package Details

| Pin Count | Description | Package Type | Material | Pin Out |
|---|---|---|---|---|
| 32 | 0.6" Dual-in-Line (DIP) | S | Ceramic | JEDEC |
| 32 | 0.4" Dual-in-Line (DIP) | K | Ceramic | JEDEC |
| 32 | 0.1" Vertical-in-Line (VIL™) | V | Ceramic | JEDEC |
| 32 | Bottom Brazed Flat Pack | G | Ceramic | JEDEC |
| 32 | Extended Leadless Chip Carrier (LCC) | W | Ceramic | JEDEC PENDING |
| 32 | J-Leaded Chip Carrier (JLCC) | J | Ceramic | JEDEC PENDING |

Package details on pages 6&7.

VIL™ is a trademark of Mosaic Semiconductor Inc. (U.S. Patent Des. 316,251), which along with Hybrid Memory Products Ltd. is part of the Implex plc group.

## Absolute Maximum Ratings (1)

| | | | |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ (2) | $V_T$ | -0.5V to +7 | V |
| Power Dissipation | $P_T$ | 1 | W |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 3.0V for less than 30ns.

## Recommended Operating Conditions

| | | *min* | *typ* | *max* | |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | - | 5.8 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | - | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | - | 70 | °C |
| | $T_{AL}$ | -40 | - | 85 | °C (I suffix) |
| | $T_{AM}$ | -55 | - | 125 | °C (M, MB suffix) |

## DC Electrical Characteristics ($V_{CC}$ = 5.0V±10%, $T_A$=-55°C to +125°C)

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$=0V to $V_{CC}$ | - | - | 2 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$=$V_{IH}$, $V_{I/O}$=0V to $V_{CC}$, OE=$V_{IH}$ | - | - | 2 | µA |
| Operating Supply Current | $I_{CC}$ | $\overline{CS}$=$V_{IL}$, , $I_{I/O}$=0mA, I/P's Static | - | 15 | 30 | mA |
| Average Supply Current | $I_{CC1}$ | Min. Cycle, $\overline{CS}$=$V_{IL}$, $V_{IN}$=$V_{IL}$ or $V_{IH}$, $I_{I/O}$=0mA | - | 45 | 70 | mA |
| | $I_{CC2}$ | 1µs cycle, Duty=100%, $I_{I/O}$=0mA, $\overline{CS}$≤0.2V, 0.2V≥$V_{IN}$≥$V_{CC}$-0.2V | - | 15 | 30 | mA |
| Standby Supply Current | $I_{SB}$ | $\overline{CS}$=$V_{IH}$, I/P's static | - | 1 | 3 | mA |
| | $I_{SB1}$ | $\overline{CS}$≥$V_{CC}$-0.2V, 0.2V≥$V_{IN}$≥$V_{CC}$-0.2V | - | 0.02 | 2 | mA |
| -L Part | $I_{SB2}$ | $\overline{CS}$≥$V_{CC}$-0.2V, 0.2V≥$V_{IN}$≥$V_{CC}$-0.2V | - | 2 | 750 | µA |
| Output Voltage | $V_{OL}$ | $I_{OL}$=2.1mA | - | - | 0.4 | V |
| | $V_{OH}$ | $I_{OH}$=-1.0mA | 2.4 | - | - | V |

Typical values are at $V_{CC}$=5.0V, $T_A$=25°C and specified loading.

## Capacitance ($V_{CC}$=5V±10%, $T_A$=25°C)

| *Parameter* | *Symbol* | *Test Condition* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|
| Input Capacitance: | $C_{IN}$ | $V_{IN}$= 0V | - | 8 | pF |
| I/O Capacitance: | $C_{I/O}$ | $V_{I/O}$= 0V | - | 10 | pF |

Note: This parameter is sampled and not 100% tested.

## AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* $V_{cc}$=5V±10%



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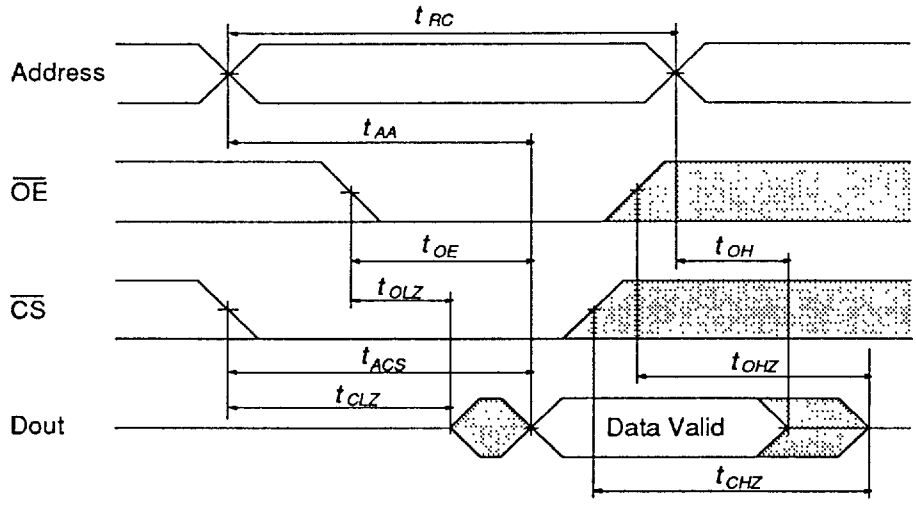
## Electrical Characteristics & Recommended AC Operating Conditions

### Read Cycle

| Parameter | Symbol | 85 min | 85 max | 10 min | 10 max | 12 min | 12 max | Unit |
|---|---|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 85 | - | 100 | - | 120 | - | ns |
| Address Access Time | $t_{AA}$ | - | 85 | - | 100 | - | 120 | ns |
| Chip Select Access Time | $t_{ACS}$ | - | 85 | - | 100 | - | 120 | ns |
| Output Enable to Output Valid | $t_{OE}$ | - | 45 | - | 50 | - | 60 | ns |
| Output Hold from Address Change | $t_{OH}$ | 10 | - | 15 | - | 15 | - | ns |
| Chip Selection to Output in Low Z(3) | $t_{CLZ}$ | 10 | - | 10 | - | 10 | - | ns |
| Output Enable to Output in Low Z(3) | $t_{OLZ}$ | 5 | - | 5 | - | 5 | - | ns |
| Chip Deselection to Output in High Z(3) | $t_{CHZ}$ | 0 | 30 | 0 | 35 | 0 | 45 | ns |
| Output Disable to Output in High Z(3) | $t_{OHZ}$ | 0 | 30 | 0 | 35 | 0 | 45 | ns |

### Read Cycle Timing Waveform (1,2)




Notes:
(1) WE is High for Read Cycle.
(2) Address valid prior to or coincident with CS transition Low.
(3) $t_{CHZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.



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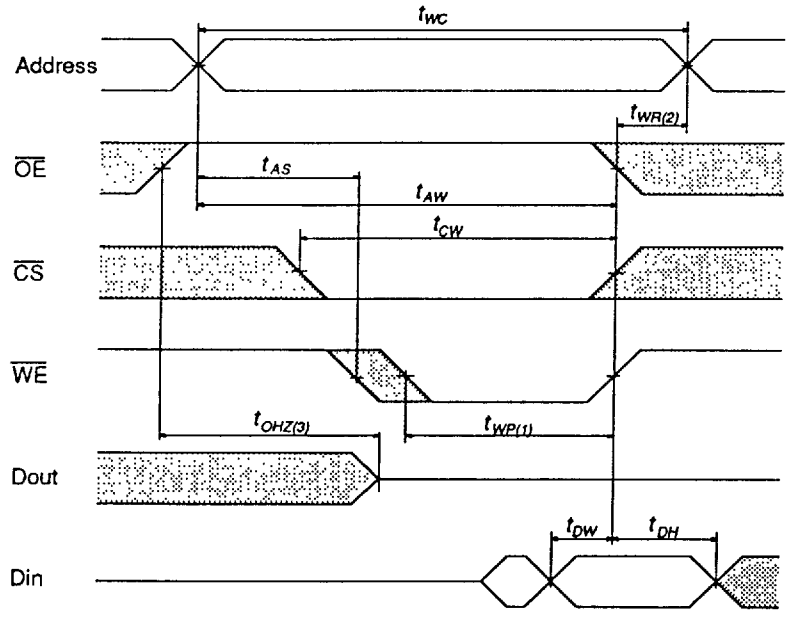
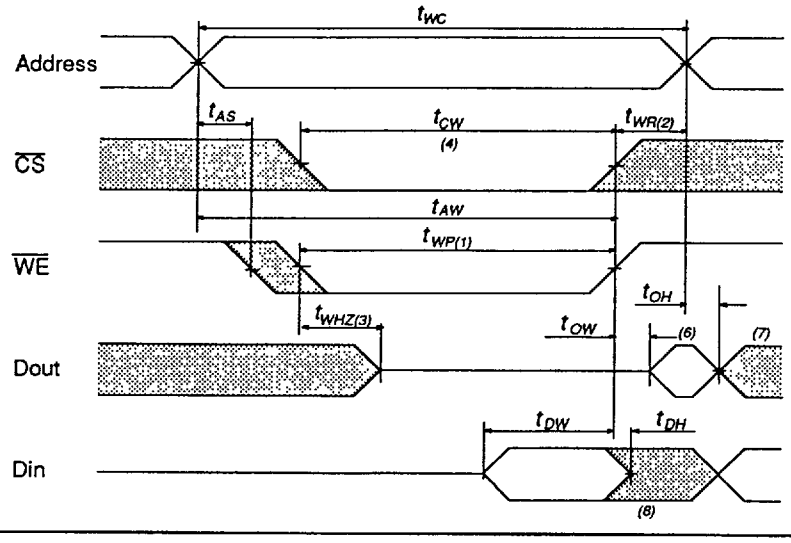
## Write Cycle

| Parameter | Symbol | 85 min | 85 max | 10 min | 10 max | 12 min | 12 max | Unit |
|---|---|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 85 | - | 100 | - | 120 | - | ns |
| Chip Selection to End of Write | $t_{CW}$ | 75 | - | 90 | - | 100 | - | ns |
| Address Valid to End of Write | $t_{AW}$ | 75 | - | 90 | - | 100 | - | ns |
| Address Setup Time | $t_{AS}$ | 0 | - | 0 | - | 0 | - | ns |
| Write Pulse Width | $t_{WP}$ | 65 | - | 75 | - | 90 | - | ns |
| Write Recovery Time | $t_{WR}$ | 5 | - | 5 | - | 10 | - | ns |
| Write to Output in High Z[9] | $t_{WHZ}$ | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 35 | - | 40 | - | 50 | - | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | - | 0 | - | 0 | - | ns |
| Output Disable to Output in High Z[9] | $t_{OHZ}$ | 0 | 30 | 0 | 35 | 0 | 40 | ns |
| Output Active from End of Write | $t_{OW}$ | 5 | - | 10 | - | 10 | - | ns |

## Write Cycle No.1 Timing Waveform




## Write Cycle No.2 Timing Waveform (5)



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## AC Characteristics Notes

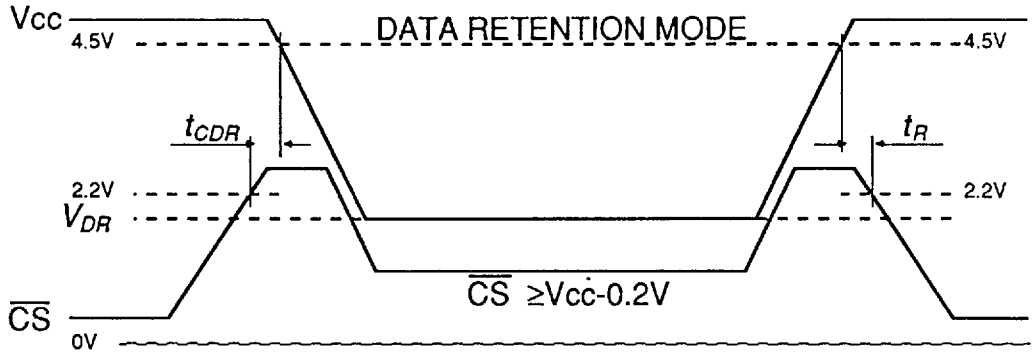
(1) A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}=V_{il}$)
(6) Dout is in the same phase as written data of this write cycle.
(7) Dout is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) $t_{WHZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

## Low $V_{cc}$ Data Retention Characteristics - L Version Only ($T_A$=-55°C to +125°C)

| *Parameter* | *Symbol* | *Test Condition* | *min* | *typ* | *max* | *Unit* |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CS}\geq V_{CC}$-0.2V | 2.0 | - | - | V |
| Data Retention Current | $I_{CCDR}$ | $V_{CC}$=3.0V, $\overline{CS}\geq V_{CC}$-0.2V, 0.2V≥$V_{IN}\geq V_{CC}$-0.2V | - | 1[1] | 350 | µA |
| Chip Deselect to Data Retention | $t_{CDR}$ | See Retention Waveform | 0 | - | - | ns |
| Operation Recovery Time | $t_R$ | See Retention Waveform | 5 | - | - | ms |

Notes 1. 20µA max at $T_A$=0 to 40°C.

## Low $V_{cc}$ Data Retention Timing Waveform



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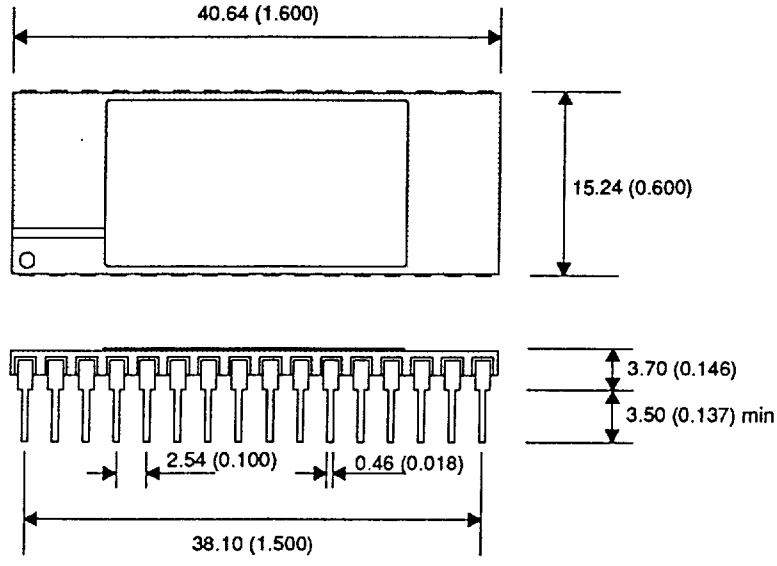
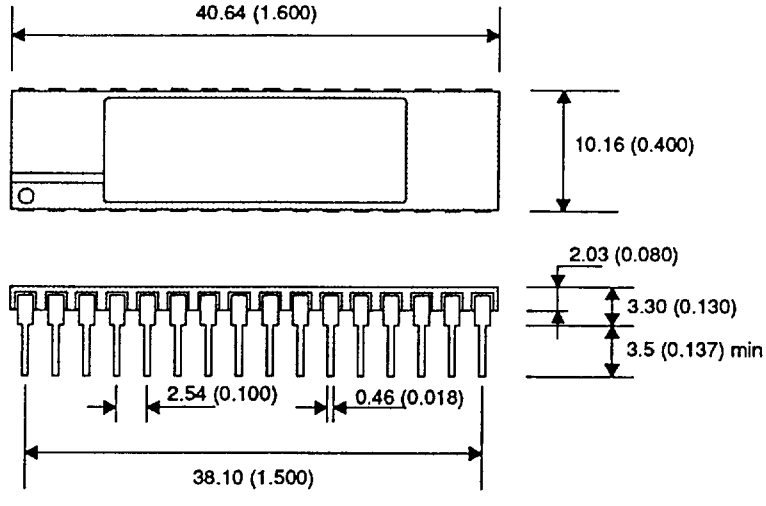
## Package Details

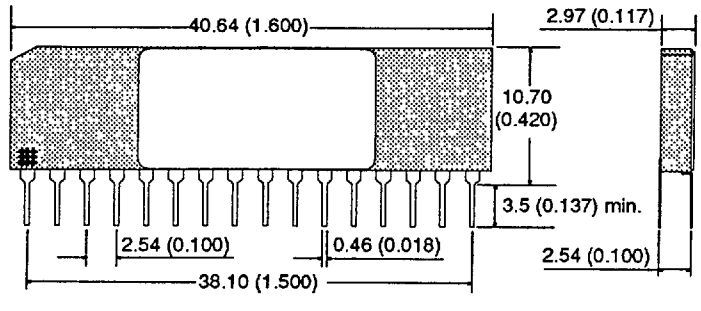
### 32 pin 0.6" Dual-in-Line (DIP) - 'SX' Package




### 32 pin 0.4" Dual-in-Line (DIP) - 'KX' Package




### 32 pin 0.1" Vertical-in-Line (VIL™) - 'VX' Package




All dimensions in mm (inches).



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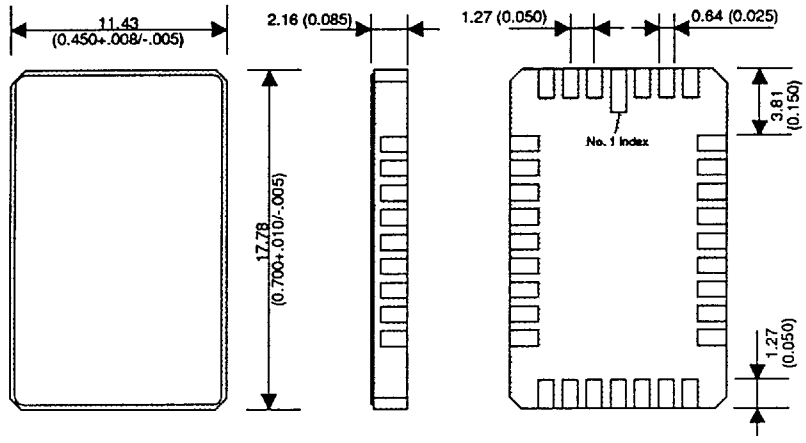
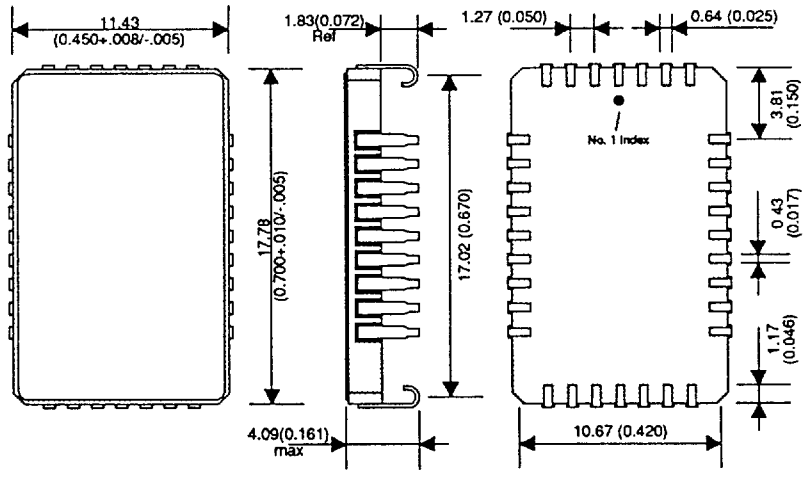
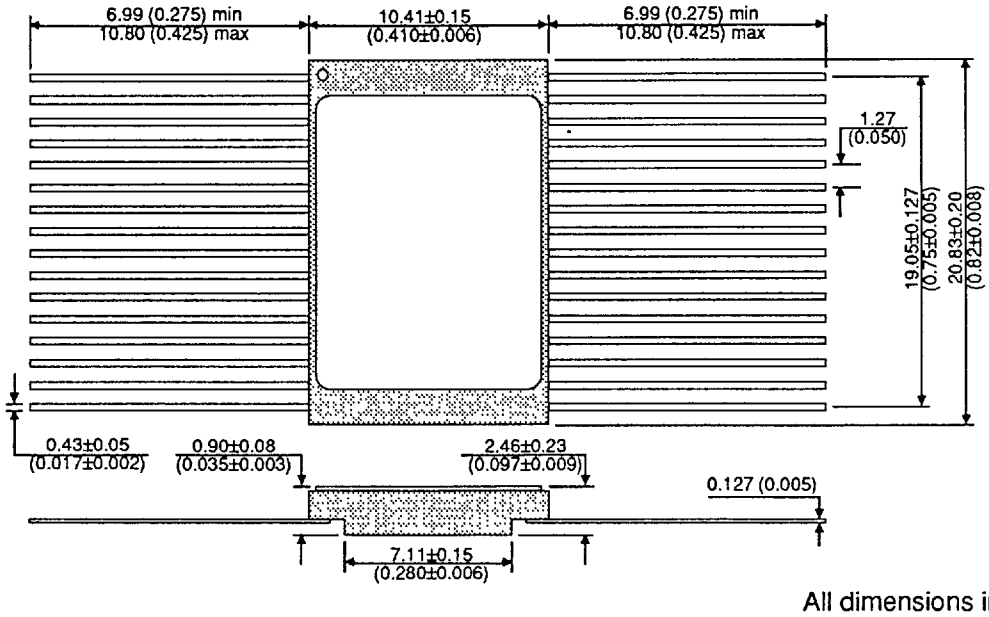
## 32 pin Extended Leadless Chip Carrier (LCC) - 'WX' Package




## 32 pin Extended 'JX' Leaded Chip Carrier (JLCC) - 'JX' Package




## 32 pin Ceramic Flatpack - 'GX' Package




All dimensions in mm (inches).



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## Military Screening Procedure

**Screening Flow** for high reliability product in accordance with MIL-STD-883C method 5004 is shown below.

| MB COMPONENT SCREENING FLOW | | |
|---|---|---|
| *SCREEN* | *TEST METHOD* | *LEVEL* |
| **Visual and Mechanical** | | |
| Internal visual | 2010 Condition B or manufacturers equivalent | 100% |
| Temperature cycle | 1010 Condition C (10 Cycles,-65°C to +150°C) | 100% |
| Constant acceleration | 2001 Condition E (Y, only) (30,000g) | 100% |
| Pre-Burn-in electrical | Per applicable device specifications at $T_A$=+25°C | 100% |
| Burn-in | $T_A$=+125°C,160hrs min | 100% |
| **Final Electrical Tests** | Per applicable Device Specification | |
| Static (dc) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Functional | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| Switching (ac) | a) @ $T_A$=+25°C and power supply extremes | 100% |
| | b) @ temperature and power supply extremes | 100% |
| **Percent Defective allowable (PDA)** | Calculated at post-burn-in at $T_A$=+25°C | 5% |
| **Hermeticity** | 1014 | |
| Fine | Condition A | 100% |
| Gross | Condition C | 100% |
| **External Visual** | 2009 Per vendor or customer specification | 100% |

## Ordering Information

**MSM8128SXLMB-10**

| | | |
|---|---|---|
| Speed | 85 | = 85 ns |
| | 10 | = 100 ns |
| | 12 | = 120 ns |
| Temp. range/screening | Blank | = Commercial |
| | I | = Industrial |
| | M | = Military |
| | MB | = High Reliability screening |
| Power Consumption | Blank | = Standard Power |
| | L | = Low Power |
| Package | SX | = 32 pin 0.6" DIP |
| | KX | = 32 pin 0.4" DIP |
| | VX | = 32 pin 0.1" VIL |
| | GX | = 32 lead FlatPack |
| | WX | = 32 pad LCC |
| | JX | = 32 pad JLCC |

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The policy of the company is one of continuous development and while the information present is believed to be accurate no liability is assumed for any data contained herewith, and the company reserves the right to make changes without notice at any time.

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