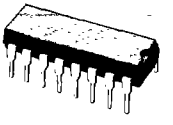
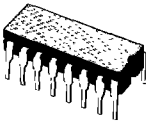
DUAL JK POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION

The T74LS109A consist of two high speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and K pins together.



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

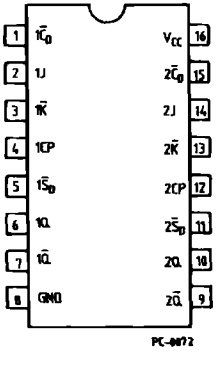
C1
(Plastic Chip Carrier)

ORDER CODES :

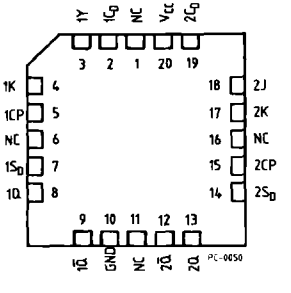
T74LS109A D1	T74LS109A C1
T74LS109A B1	T74LS109A M1

PIN CONNECTION (top view)

DUAL IN LINE

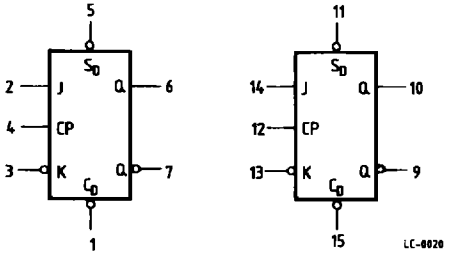


CHIP CARRIER

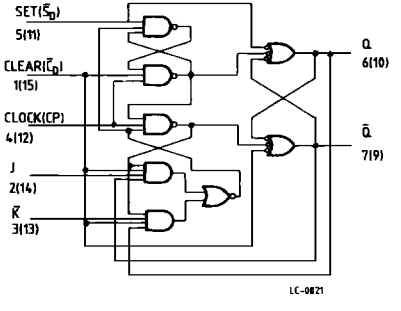


NC = No Internal Connection

LOGIC SYMBOL



LOGIC DIAGRAM AND TRUTH TABLE



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

Operating Mode	Input				Output	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (clear)	H	L	X	X	L	H
* Undetermined	L	L	X	X	H	H
Load "1" (set)	H	H	h	h	H	L
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (reset)	H	H	l	l	L	H

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously.
The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable ; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h, (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS109AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Condition (note 1)		Unit
			Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage		V
V_{IL}	Input LOW Voltage				0.8	Guaranteed Input LOW Voltage		V
V_{CD}	Input Clamp Diode Voltage			- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage		2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage			0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN V_{IN} = V_{IL} or V_{IH} per Truth Table	V
				0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current	J, K, Clock Set, Clear			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
		J, K, Clock Set, Clear			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current	J, K, Clock Set, Clear			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)		- 20		- 100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				8.0	V_{CC} = MAX		mA

Notes : 1. For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

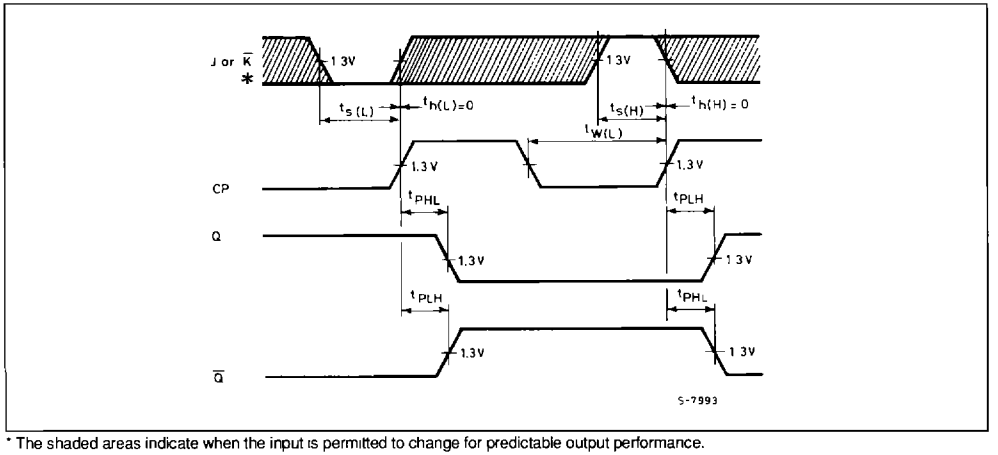
Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	25	33		V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Clock, Clear Set to Output		13 25	25 40		ns

AC SET-UP REQUIREMENTS : T_A = 25 °C

Symbol	Parameter		Limits			Test Conditions	Unit
			Min.	Typ.	Max.		
t_W	Clock, Clear, Set Pulse Width		25			V_{CC} = 5.0 V	ns
t_s	Data Set-up Time	HIGH	35				ns
		LOW	25				ns
t_h	Hold Time		5.0				ns

AC WAVEFORMS

Figure 1 :Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 2 :Set and Clear to Output Delays, Set and Clear Pulse Widths.

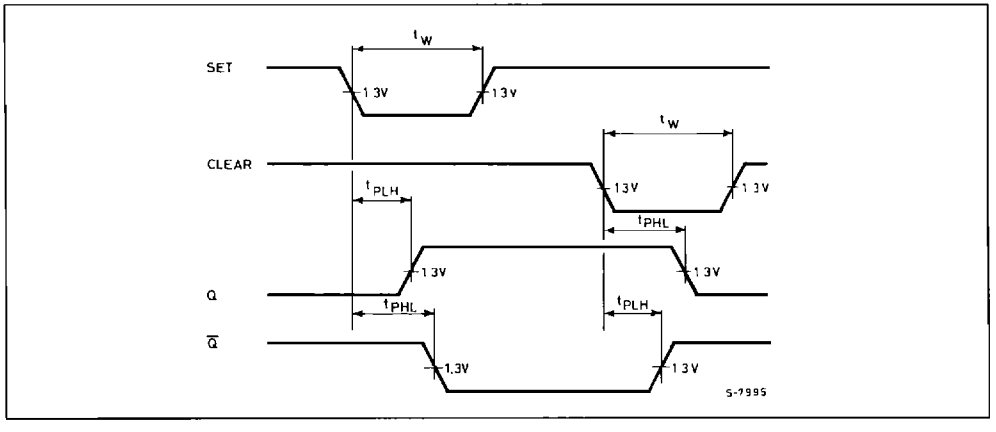
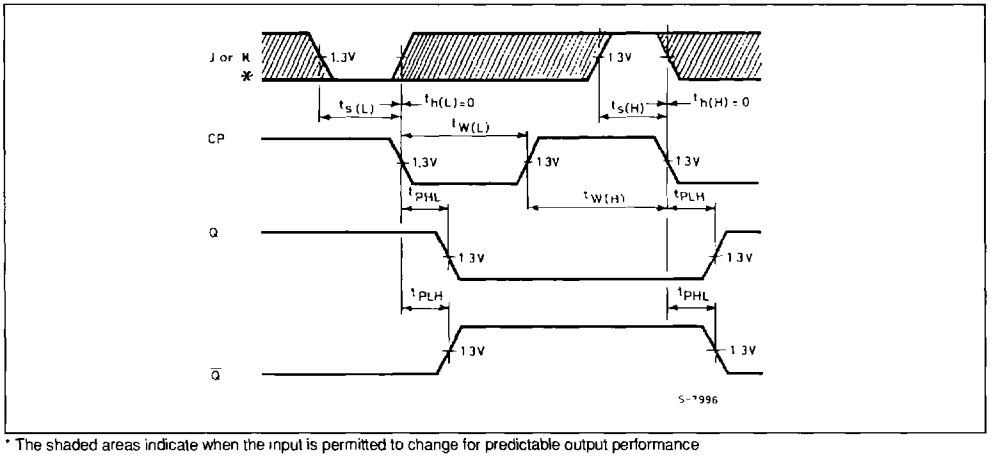


Figure 3 :Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width.



* The shaded areas indicate when the input is permitted to change for predictable output performance