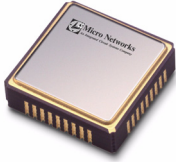




GENERAL DESCRIPTION

The M906-02 is a PLL (Phase Locked Loop) based clock generator that uses an internal VCSO (Voltage Controlled SAW Oscillator) to produce a very low jitter output clock. From the M906-02-155.5200, an output clock frequency of 155.52 or 77.76MHz is provided from six LVPECL clock output pairs. (Other frequencies are available; consult factory.) The accuracy of the output frequency is assured by the internal PLL that phase-locks the internal VCSO to the reference input frequency (19.44MHz for the M906-02-155.5200). The input reference can either be an external crystal, utilizing the internal crystal oscillator, or a stable external clock source such as a packaged crystal oscillator.



PIN ASSIGNMENT (9 x 9 mm SMT)

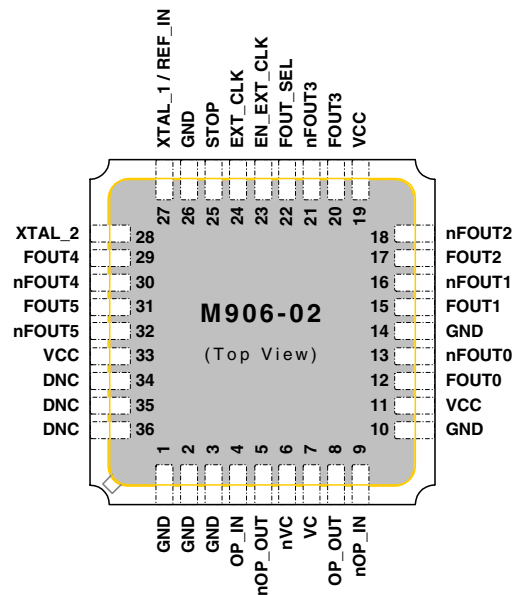


Figure 1: Pin Assignment

FEATURES

- ◆ Output clock frequency range 75MHz to 175MHz (Consult factory for frequency availability)
- ◆ Selectable divider chooses one of two frequencies
- ◆ Six identical LVPECL output pairs (same frequency)
- ◆ Jitter 0.7ps rms (at 155.52MHz, over 12kHz-20MHz), typ.
- ◆ Ideal for OC-48/STM-16 clock reference
- ◆ Output-to-output skew < 100ps
- ◆ External XTAL or LVCMOS reference input
- ◆ Selectable external feed-through clock input
- ◆ STOP clock control (Logic 1 stops output clocks)
- ◆ Integrated SAW (surface acoustic wave) delay line
- ◆ Single 3.3V power supply
- ◆ Small 9 x 9 mm SMT (surface mount) package

Example Output Frequency Configurations

(M906-02-155.5200)

Ref Clock Frequency (MHz)	VCSO Frequency (MHz)	P Divider Value	Output Frequency (MHz)
19.44	155.52	1	155.52
		2	77.76

Table 1: Example Output Frequency Configurations

SIMPLIFIED BLOCK DIAGRAM

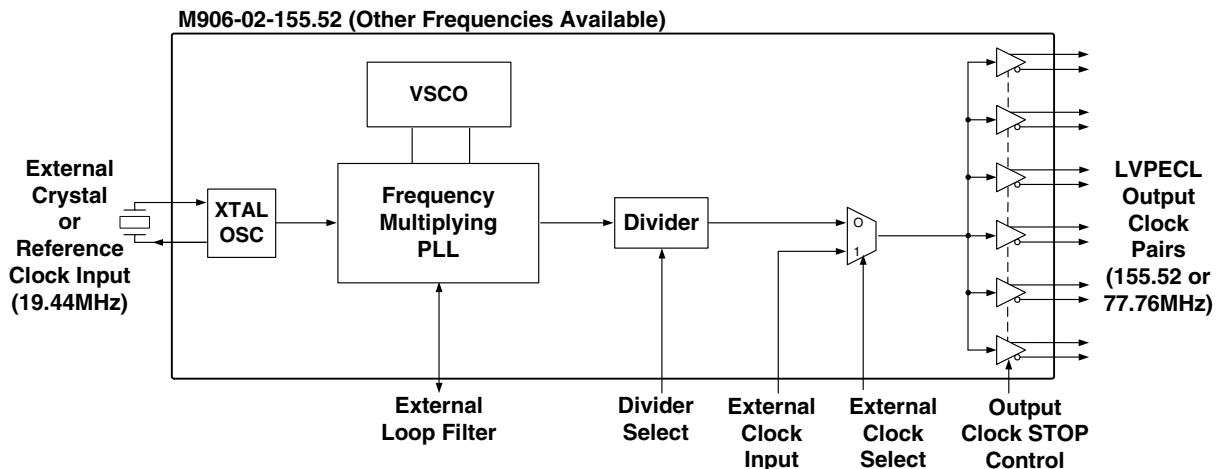


Figure 2: Simplified Block Diagram



DETAILED BLOCK DIAGRAM

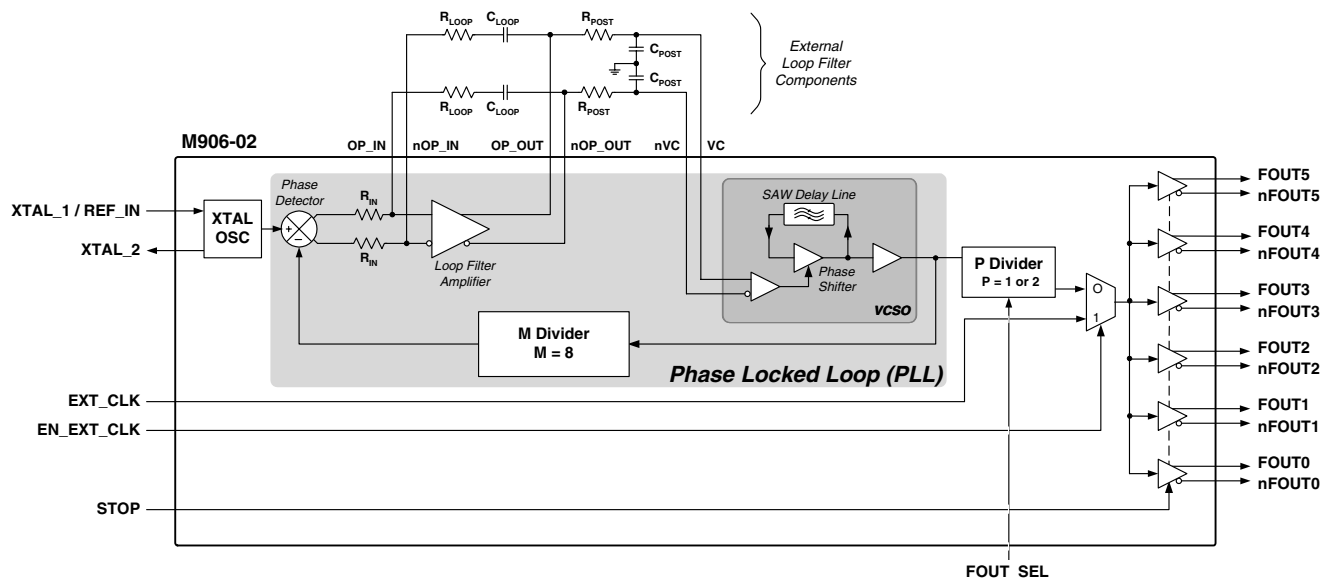


Figure 3: Detailed Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4	OP_IN	Input		
9	nOP_IN			
5	nOP_OUT	Output		External loop filter connections. See Figure 5.
8	OP_OUT			
6	nVC	Input		
7	VC			
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12, 13	FOUT0, nFOUT0	Output	No internal terminator	Clock output pairs, differential LVPECL output (155.52 or 77.76 MHz for the M906-02-155.5200)
15, 16	FOUT1, nFOUT1			
17, 18	FOUT2, nFOUT2			
20, 21	FOUT3, nFOUT3			
29, 30	FOUT4, nFOUT4			
31, 32	FOUT5, nFOUT5			
22	FOUT_SEL	Input		Determines post-PLL divider value: When FOUT_SEL = 1, P = 1 When FOUT_SEL = 0, P = 2
23	EN_EXT_CLK	Input	Internal pull-down resistor ¹	Logic 1 enables the EXT_CLK input. Use Logic 0 for normal operation.
24	EXT_CLK	Input		External clock feed-through: 0 to 200 MHz
25	STOP	Input	Internal pull-down resistor ¹	Logic 1 stops clock outputs. Use Logic 0 for normal operation.
27	XTAL_1 / REF_IN	Input		External crystal connection. Also accepts LVCMOS/LVTTL compatible clock source.
28	XTAL_2	Input		External crystal connection. Leave unconnected when driving pin 27 with external clock reference.
34, 35, 36	DNC		Do Not Connect.	Internal nodes. Connection to these pins can cause erratic device operation.

Table 2: Pin Descriptions

Note 1: For typical value of internal pull-down resistor, see **DC Characteristics, Pull-down** on pg. 6 for typical value.



FUNCTIONAL DESCRIPTION

The M906-02 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to an input reference clock.

The M906-02 combines the flexibility of a VCSO (Voltage Controlled SAW Oscillator) with the stability of a crystal oscillator.

Input Reference

The 19.44MHz input reference can either be an external, discrete crystal device or a stable external clock source such as a packaged crystal oscillator:

- If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should be a parallel-resonant, fundamental mode crystal. Apply it to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.
- If an external LVCMOS/LVTTL clock source is used, apply it to the XTAL_1 / REF_IN input pin.

In either case, the reference clock is supplied directly to the phase detector of the PLL.

The EX_CLK pin is available for a clock feed-through mode for testing. See "External Clock Feed-through" on pg. 3.

The PLL

The PLL (Phase Locked Loop) includes the phase detector, the VCSO, and a feedback divider (labeled "M Divider").

The feedback divider is a digital circuit that divides the VCSO output frequency by a numerical value "M" in order to match the input reference frequency.

By controlling the frequency and phase of the VCSO, the phase detector precisely locks the frequency and phase of the feedback divider output to that of the input reference. This creates an output frequency that is a multiple of the reference frequency (which is output from the VCSO).

The relationship between the VCSO output frequency, the M Divider, and the input reference frequency is defined as follows:

$$F_{vcs0} = M \times F_{xtal}$$

For the M906-02-155.5200 (see "Ordering Information" on pg. 8):

- VCSO output frequency = 155.52MHz
- M = 8
- Input reference frequency = 19.44MHz

Therefore, for the M906-02-155.5200:

$$155.52\text{MHz} = 8 \times 19.44\text{MHz}$$

The VCSO center output frequency of 155.52MHz enables the product of M × input crystal frequency to fall within the lock range of the VCSO.

Post-PLL Divider

The M906-02 also features a post-PLL divider (labeled "P Divider") for selecting one of two output frequencies (e.g., 155.52 or 77.76 MHz).

The FOUT_SEL pin determines the P Divider value:

- When FOUT_SEL = 1, P = 1.
- When FOUT_SEL = 0, P = 2.

External Clock Feed-through

The EXT_CLK pin provides an input for an external single-ended clock that directly drives the LVPECL clock outputs. This pin is intended for system debugging and performance evaluation..

- EN_EXT_CLK Logic 1 enables the EXT_CLK input. Use Logic 0 for normal operation.
- EXT_CLK Apply an external LVCMOS/LVTTL clock source for 0 to 200 MHz feed-through operation. Leave inactive for normal operation.¹

Note 1: In applications where EXT_CLK is active while the SAW PLL signal path is enabled, it is necessary to gate the EXT_CLK to minimize jitter in the LVPECL output pairs. See the *PCB Design Guidelines for ICS SAW PLLs* application note at www.icst.com/products/appnotes/M000-AN-001.PCBdesign.pdf

STOP Clock

The STOP pin puts the output clock into a static condition.

- Logic 1 Output clocks are static
- Logic 0 Output clocks enabled for normal operation



APPLICATION INFORMATION

This section includes information on the optional external crystal and on the external loop filter.

The subsections on the loop filter provide example component values and also briefly describe the SAW PLL simulator tool and additional application information available at www.icst.com.

External Crystal Specifications

If an external crystal is used with the on-chip crystal oscillator circuit (XTAL OSC), the external crystal should have the following general specifications:

Crystal Specifications

Parameter	Min	Typ	Max	Unit
Crystal Type	AT-cut quartz			
Mode of Oscillation	Fundamental			
f_0 Frequency Range	16	40		MHz
ESR Equivalent Series Resistance		50		Ω
Spurious Response (non-harmonic)		-40		dBc
C_L Load Capacitance, parallel load resonant	16	32		pF
P_0 Drive Level	0.1	1.0		mW

Table 3: Crystal Specifications

The external crystal will be applied to the XTAL_1 / REF_IN and XTAL_2 input pins. External crystal load capacitors are also required.

Recommended External Crystal Configuration

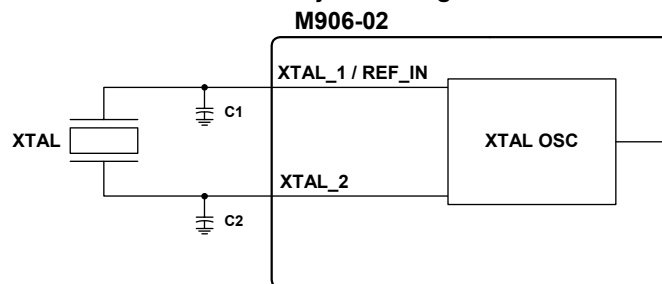


Figure 4: Recommended External Crystal Configuration

XTAL Load Capacitance Specification = 18 pF

C1 = 27 pF

C2 = 33 pF

External load capacitors C1 and C2 present a load of 15 pF to the crystal (they are seen in series by the crystal through the common ground connection). With the additional of PCB trace capacitance and M906-02 input capacitance, the total load to the crystal is about 18 pF.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M906-02 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 5).

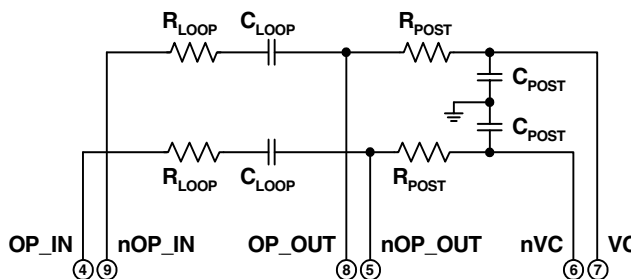


Figure 5: External Loop Filter

The loop filter is implemented as a differential circuit to minimize system noise interference. Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here. See Table 4, Example External Loop Filter Component Values, below.

Example External Loop Filter Component Values

PLL Bandwidth (kHz)	Damping Factor	R loop (k Ω)	C loop (μ F)	R post (k Ω)	C post (pF)
0.395	2.0	1.5	4.70	20	3300
1.2	2.9	4.7	1.00	20	1000
10^1	2.4	39.0	0.01	20	240

Table 4: Example External Loop Filter Component Values

Note 1: Recommended for minimum output jitter when using a crystal or crystal oscillator reference.

Refer to the M906-02 product web page at www.icst.com/products/summary/m906-02.htm for additional product information.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

Refer to the SAW PLL Simulator Software web page at www.icst.com/products/calculators/m2000filterSWdesc.htm for additional information.



SAW PLL Application Notes Available

The ICS web site (www.icst.com) also has application notes on:

- PCB layout guidelines (including special detailed instructions for preventing issues such as external reference crosstalk)
- Any new special device application details that may become available

- Instructions for using PLL simulator software
- Guidelines for PCB fabrication (including recommended PCB footprint, solder mask, and furnace profile)

Refer to the SAW PLL Application Notes web page at www.icst.com/products/appnotes/SawPLLAppNotes.htm for application notes and any additional product information that may become available.

ABSOLUTE MAXIMUM RATINGS¹

Symbol	Parameter	Rating	Unit
V _I	Inputs	-0.5 to V _{CC} +0.5	V
V _O	Outputs	-0.5 to V _{CC} +0.5	V
V _{CC}	Power Supply Voltage	4.6	V
T _S	Storage Temperature	-45 to +100	°C

Table 5: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Positive Supply Voltage	3.135	3.3	3.465	V
T _A	Ambient Operating Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	°C

Table 6: Recommended Conditions of Operation



ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ (commercial), $T_A = -40^\circ C$ to $+85^\circ C$ (industrial), $F_{VCSO} = 155.52MHz$,¹
LVPECL outputs terminated with 50Ω to $V_{CC} - 2V$

	Symbol	Parameter	Min	Typ	Max	Unit
Power Supply	V_{CC}	Positive Supply Voltage	3.135	3.3	3.465	V
	I_{CC}	Power Supply Current		350		mA
Logic Inputs	V_{IH}	Input High Voltage	2		$V_{CC} + 0.3$	V
	V_{IL}	Input Low Voltage	-0.3		0.8	V
	I_{IH}	Input High Current			150	μA
	I_{IL}	Input Low Current	-5.0			μA
Reference Clock Input	V_{IH}	Input High Voltage	$(V_{CC}/2) + 0.5$		$V_{CC} + 0.3$	V
	V_{IL}	Input Low Voltage	-0.3		$(V_{CC}/2) + 0.5$	V
	I_{IH}	Input High Current			150	μA
	I_{IL}	Input Low Current	-5.0			μA
All Inputs	C_{IN}	Input Capacitance, All Inputs	FOUT_SEL, EN_EXT_CLK, EXT_CLK, STOP, XTAL_1 / REF_IN		4	pF
Pull-down	$R_{pulldown}$	Internal Pull-down Resistor	EN_EXT_CLK, STOP		51	k Ω
Differential Output	V_{OH}	Output High Voltage	$V_{CC} - 1.4$		$V_{CC} - 1.0$	V
	V_{OL}	Output Low Voltage	$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
	V_{P-P}	Peak to Peak Output Voltage	0.6		0.85	V

Note 1: For other VCSO center frequencies, contact ICS

Table 7: DC Characteristics

AC Characteristics

Unless implied otherwise, $V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ (commercial), $T_A = -40^\circ C$ to $+85^\circ C$ (industrial), $F_{VCSO} = 155.52MHz$,¹
LVPECL outputs terminated with 50Ω to $V_{CC} - 2V$

	Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
	F_{OUT}	Output Frequency Range	75		175	MHz	FOUT_SEL=1 ¹
	F_{IN}	Nominal Input Frequency, XTAL_1 / REF_IN		19.44		MHz	
	APR	VCSO Pull-Range	± 100	± 150		ppm	
Φ_n	Single Side Band Phase Noise @ 155.52MHz	1kHz Offset		-100		dBc/Hz	
		10kHz Offset		-110		dBc/Hz	
		100kHz Offset		-134		dBc/Hz	
J(t)	Jitter (rms)		0.7	1.0	ps	12kHz to 20MHz	
t_{DC}	Output Duty Cycle, High Time		45	50	55	%	
t_R	Output Rise Time	FOUT, nFOUT (0-5)	350	450	550	ps	20% to 80%
t_F	Output Fall Time	FOUT, nFOUT (0-5)	350	450	550	ps	20% to 80%
t_S	Output Skew	Between Any Pair			100	ps	
		EXT_CLK Frequency	EXT_CLK	0		200	MHz

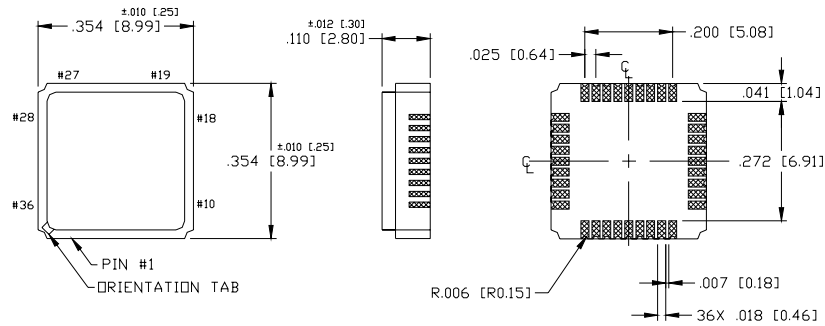
Note 1: For other VCSO center frequencies, contact ICS

Table 8: AC Characteristics



DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:



Refer to the SAW PLL application notes web page at www.icst.com/products/appnotes/SawPllAppNotes.htm for application notes, including recommended PCB footprint, solder mask, and furnace profile.

NOTES:

1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ± 0.005 [0.13]

Figure 6: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier



ORDERING INFORMATION

Part Numbering Scheme

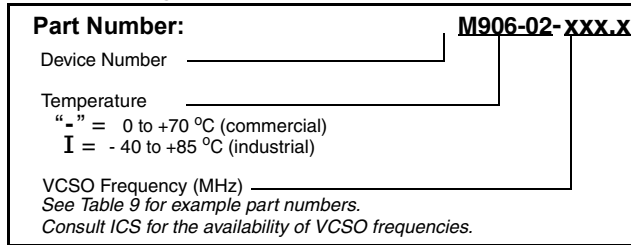


Figure 7: Part Numbering Scheme

Example Part Numbers

For Output Frequencies (MHz)	Temperature	Order Part Number
155.52 (and 77.76)	commercial	M906-02-155.5200
	industrial	M906-02I155.5200
150 to 175 (and 75 to 87.5)	commercial	M906-02-xxx.xxxx
	industrial	M906-02Ixxx.xxxx

Table 9: Example Part Numbers

Consult ICS for the availability of VCSO frequencies

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