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128K x 32 SRAM Module

PUMA67S4000/A-45/55/70

Issue 4.0 : March 1996

Description

The PUMA67S4000/A is a 4Mbit CMOS High Speed Static RAM organised as 128k x 32 in a JEDEC J-leaded Ceramic Surface Mount Substrate. The output width is user configurable to 8, 16 or 32 bits and is available with two pinouts, a single $\overline{WE}$ or version A with $\overline{WE1}$-4. Access times available are 45ns, 55ns and 70ns. It has a low power standby of 44mW And is 3.0V battery back-up compatible. All inputs and outputs are TTL compatible.

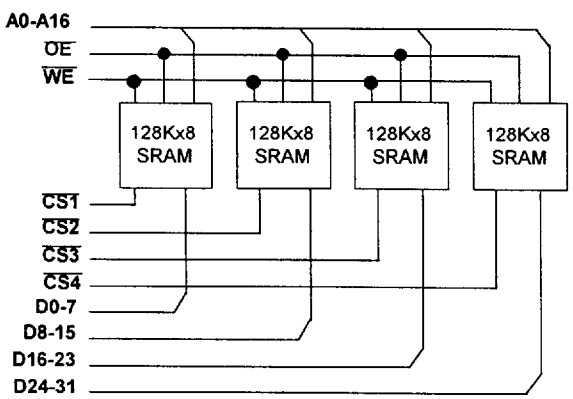
All versions can be screened in accordance with MIL-STD-883 or with BS9400 requirements.

4,194,304 bit CMOS High Speed Static RAM

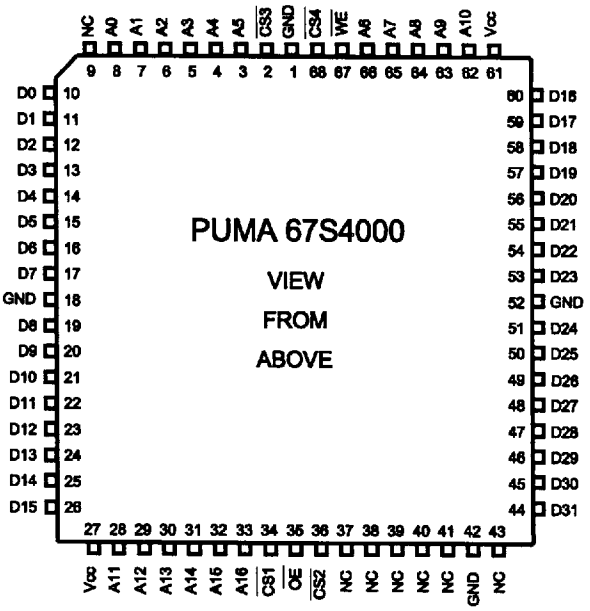
Features

- Fast Access Times of 45/55/70 ns.
- JEDEC 68 'J' Ceramic Surface Mount Substrate, available in two pinouts : Single $\overline{WE}$ is standard version, $\overline{WE1}$~4 is A version.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power 688 / 1045 / 1760 mW (Max)
- Low Power Standby 44 mW (Max). - L Version
- 3.0V Battery Back-up Capability.
- TTL Compatible Inputs and Outputs.
- Equal Access and Cycle Times.

Block Diagram (see page 7 for A Block Diagram)



Pin Definition (see page 7 for A pinout)



Pin Functions

A0~A16	Address Inputs	**$\overline{D0~D31}$**	Data Inputs/Outputs
$\overline{CS1~4}$	Chip Selects	**$\overline{OE}$**	Output Enable
$\overline{WE}$	Write Enable (**$\overline{WE1~4}$** for A version)	**NC**	No Connect
V_{CC}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{ss} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	4	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width: -3.0V for less than 20ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (Suffix **I**)
	T_{AM}	-55	-	125	°C (Suffix **M**, **MB**)

DC Electrical Characteristics (V_{CC}=5V±10%, T_A=-55°C to +125°C)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
Input Leakage Current	Address, $\overline{OE}$, $\overline{WE}$	I_{LI1}	V_{IN} = 0V to V_{CC}	-8	-	8	µA
	$\overline{CS1}$~4, $\overline{WE1}$~4	I_{LI2}	V_{IN} = 0V to V_{CC}	-2	-	2	µA
Output Leakage Current	8bit	I_{LO}	$\overline{CS}$(2)=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=0V to V_{CC}	-8	-	8	µA
Operating Supply Current	32bit	I_{CC32}	$\overline{CS}$(2)=V_{IL}, $I_{I/O}$=0mA, I/P's static	-	-	320	mA
	16bit	I_{CC16}	As above	-	-	190	mA
	8bit	I_{CC8}	As above	-	-	125	mA
Average Supply Current	32bit	I_{CC32}	Min. cycle, $I_{I/O}$=0mA, 100% Duty	-	-	480	mA
	16bit	I_{CC16}	As above	-	-	270	mA
	8bit	I_{CC8}	As above	-	-	165	mA
Standby Supply Current	TTL levels	I_{SB}	$\overline{CS}$(2) = V_{IH}	-	-	60	mA
	-L Version	I_{SB1}	$\overline{CS}$(2) ≥ V_{CC}-0.2V, V_{IN} = V_{IH} or V_{IL}, Min. cycle	-	0.04	8	mA
Output Voltage Low		V_{OL}	I_{OL} = 8.0 mA	-	-	0.4	V
Output Voltage High		V_{OH}	I_{OH} = -4.0 mA	2.4	-	-	V

Notes: (1) Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

(2) $\overline{CS}$ above is accessed through $\overline{CS1}$~4 (and $\overline{WE}$ is accessed by $\overline{WE1}$~4 on the PUMA 67S4000A), and these inputs must be controlled as required by the user.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*	
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	38	pF	
	$\overline{WE1}$~4(1), $\overline{CS1}$~4	C_{IN2}	V_{IN}=0V	-	17	pF	
I/O Capacitance	D0~D31	$C_{I/O}$	$V_{I/O}$=0V	-	38	pF	These parameters are calculated, not measured.

Note: (1) On the standard module $\overline{WE}$ = 38pF max.

Operating Modes

The Table below shows the logic inputs required to control the operating modes of each of the SRAMs on the PUMA 67S4000 or PUMA 67S4000A modules.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*V_{CC} Current*	*I/O Pin*	*Reference Cycle*
Not Selected	1	X	X	I_{SB}, I_{SB1}	High Z	Power Down
Output Disable	0	1	1	I_{CC}	High Z	
Read	0	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	X	0	I_{CC}	D_{IN}	Write Cycle

1 = V_{IH},
0 = V_{IL},
X = Don't Care

Note: $\overline{CS}$ above is accessed through $\overline{CS1\sim4}$ (and $\overline{WE}$ by $\overline{WE1\sim4}$ on the PUMA 67S4000A). For correct operation, $\overline{CS1\sim4}$ (and $\overline{WE1\sim4}$) must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation.

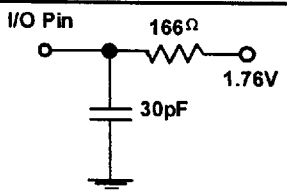
Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS1\sim4} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS1\sim4} \geq V_{CC}$-0.2V, V_{IN}>0V	-	-	3.0	mA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ns

AC Test Conditions

*Input pulse levels: 0.0V to 3.0V
*Input rise and fall times: 5 ns
*Input and Output timing reference levels: 1.5V
*V_{cc}=5V±10%
*PUMA module is tested in 32 bit mode.

Output Load



AC OPERATING CONDITIONS

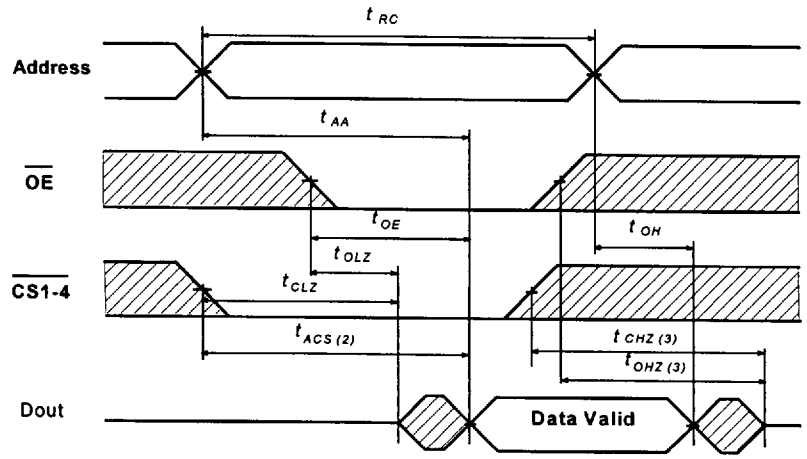
Read Cycle

Parameter	Symbol	45 min	45 max	55 min	55 max	70 min	70 max	Units
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	45	-	55	-	70	ns
Chip Select Access Time(2)	t_{ACS}	-	45	-	55	-	70	ns
Output Enable to Output Valid	t_{OE}	-	25	-	30	-	40	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z(3)	t_{CHZ}	0	20	0	25	0	30	ns
Output Disable to Output in High Z(3)	t_{OHZ}	0	25	0	30	0	35	ns

Write Cycle

Parameter	Symbol	45 min	45 max	55 min	55 max	70 min	70 max	Unit
Write Cycle Time	t_{WC}	45	-	55	-	70	-	ns
Chip Selection to End of Write	t_{CW}	40	-	45	-	55	-	ns
Address Valid to End of Write	t_{AW}	40	-	45	-	55	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	40	-	50	-	ns
Write Recovery Time	t_{WR}	3	-	3	-	3	-	ns
Write to Output in High Z	t_{WHZ}	0	20	0	25	0	30	ns
Data to Write Time Overlap	t_{DW}	20	-	25	-	30	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Read Cycle Timing Waveform (1-3)



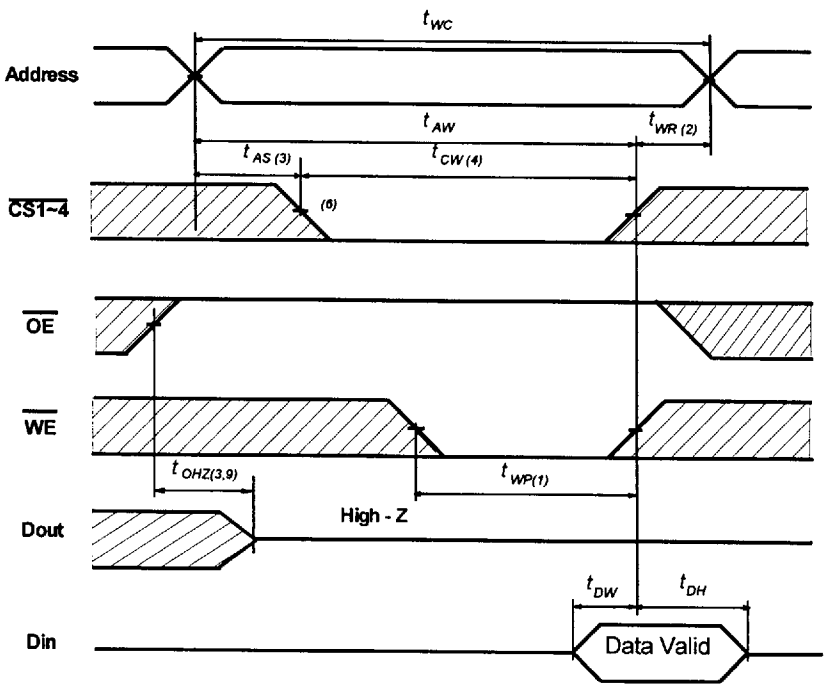
Notes:

(1) During the Read Cycle, $\overline{WE}$ is high for the PUMA 67S4000 module and $\overline{WE1\sim4}$ are high for the PUMA 67S4000A module.

(2) Address valid prior to or coincident with $\overline{CS1\sim4}$ transition Low.

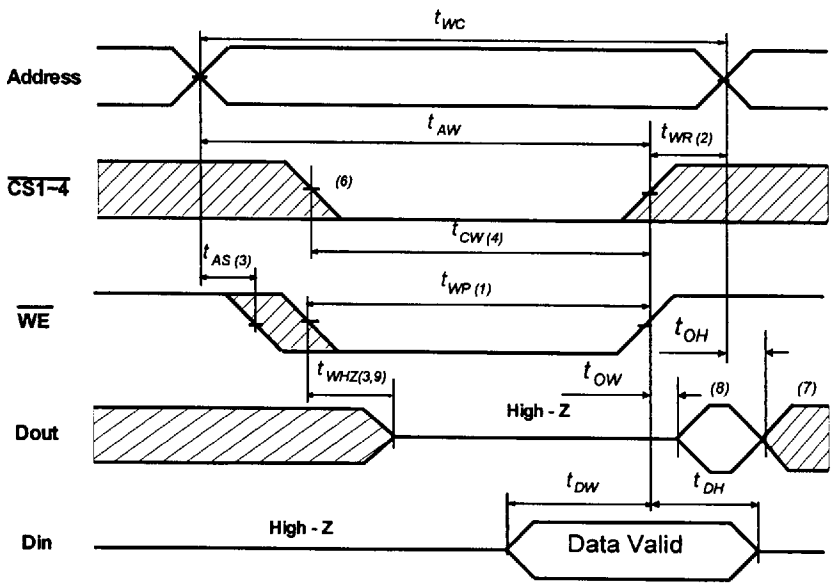
(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform



Note: On the PUMA 67S4000A, $\overline{WE}$ refers to $\overline{WE1\sim4}$.

Write Cycle No.2 Timing Waveform



Note: On the PUMA 67S4000A, $\overline{WE}$ refers to $\overline{WE1\sim4}$.

AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})

(6) D_{OUT} is in the same phase as written data of this write cycle.

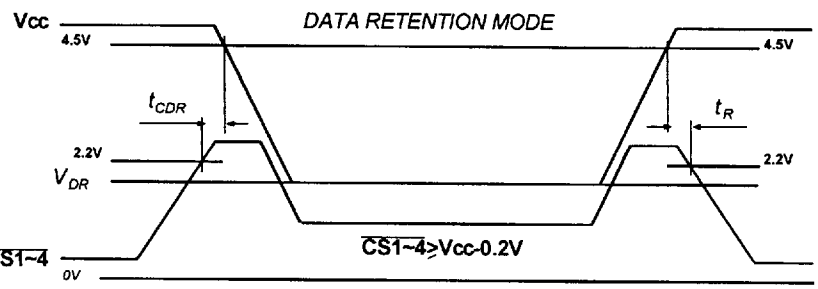
(7) D_{OUT} is the read data of next address.

(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied.

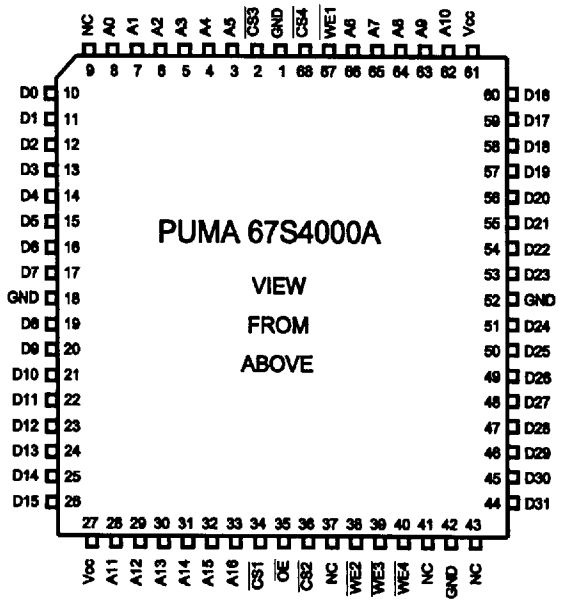
(9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

$\overline{CS}$ refers to $\overline{CS1\sim4}$. $\overline{WE}$ above refers to $\overline{WE}$ on the PUMA 67S4000 and $\overline{WE1\sim4}$ on the PUMA 67S4000A

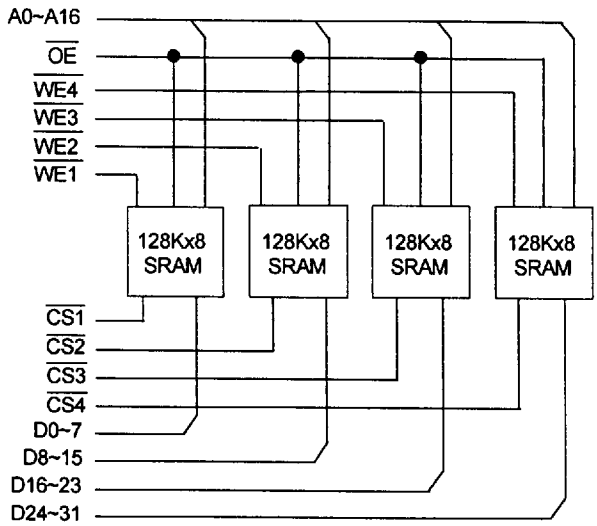
Low V_{cc} Data Retention Timing Waveform



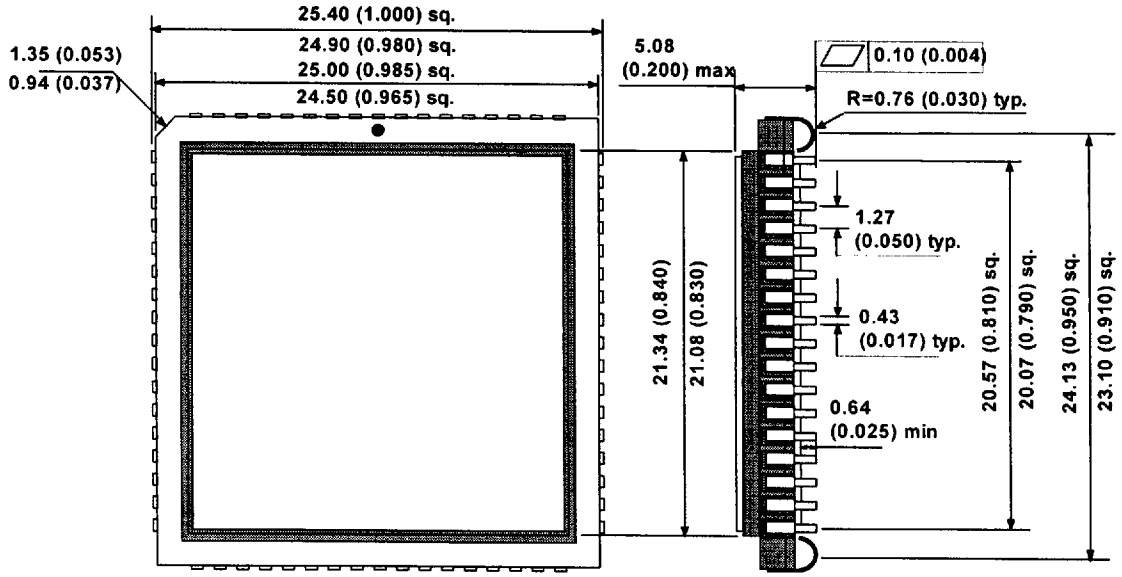
Pin Definition version "A"



Block Diagram version "A"



Package Details Dimensions in mm(inches)



SCREENING

Military Screening Procedure

MultiChip Screening Flow for high reliability product is in accordance with Mil-883 method 5004.

MB MULTICHIP MODULE SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Constant acceleration	2001 Condition B (Y1 & Y2) (10,000g)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C, 160hrs minimum.	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	10%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 67S4000ALMB-45