DESCRIPTION

The HY628100A/HY628100A-I is a high speed, low power and 1M bit CMOS Static Random Access Memory organized as 131,072 words by 8bit. The HY628100A/HY628100A-I uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particulary well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

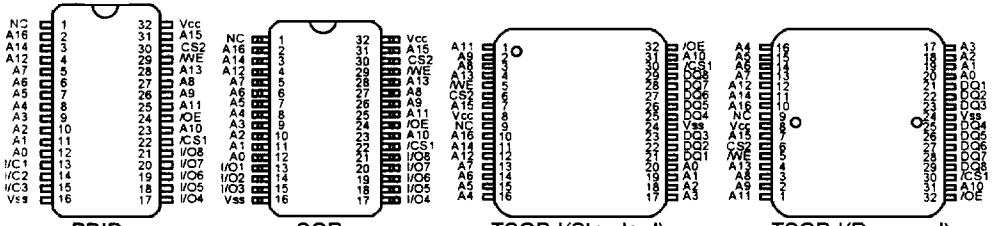
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(L/LL-part)
  - 2.0V(min) data retention
- Standard pin configuration
  - 32pin 600mil PDIP
  - 32pin 525mil SOP
  - 32pin 8x20mm/ 8x13.4mm TSOP-I (Standard and Reversed)

Product No	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)			Temperature (℃)
					L	LL	
HY628100A	5.0	55/70/85	10	1mA	100	20	0~70(Normal)
HY628100A-I	5.0	55/70/85	10	-	100	30	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

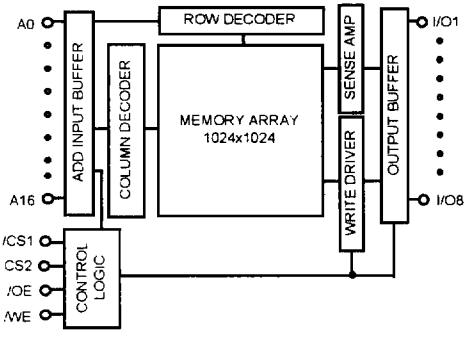
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A16	Address Input
I/O1 ~ I/O16	Data Input/Output
Vcc	Power(5.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
HY628100AP	55/70/85			PDIP
HY628100ALP	55/70/85	L-part		PDIP
HY628100ALLP	55/70/85	LL-part		PDIP
HY628100AG	55/70/85			SOP
HY628100ALG	55/70/85	L-part		SOP
HY628100ALLG	55/70/85	LL-part		SOP
HY628100AT1	55/70/85			TSOP-I(Standard)
HY628100ALT1	55/70/85	L-part		TSOP-I(Standard)
HY628100ALLT1	55/70/85	LL-part		TSOP-I(Standard)
HY628100AR1	55/70/85			TSOP-I(Reversed)
HY628100ALR1	55/70/85	L-part		TSOP-I(Reversed)
HY628100ALLR1	55/70/85	LL-part		TSOP-I(Reversed)
HY628100ALP-I	55/70/85	L-part	E.T.	PDIP
HY628100ALLP-I	55/70/85	LL-part	E.T.	PDIP
HY628100ALG-I	55/70/85	L-part	E.T.	SOP
HY628100ALLG-I	55/70/85	LL-part	E.T.	SOP
HY628100ALT1-I	55/70/85	L-part	E.T.	TSOP-I(Standard)
HY628100ALLT1-I	55/70/85	LL-part	E.T.	TSOP-I(Standard)
HY628100ALR1-I	55/70/85	L-part	E.T.	TSOP-I(Reversed)
HY628100ALLR1-I	55/70/85	LL-part	E.T.	TSOP-I(Reversed)

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.5 to 7.0	V	
T_A	Operating Temperature	0 to 70	℃	HY628100A
		-40 to 85	℃	HY628100A-I
T_{STG}	Storage Temperature	-65 to 125	℃	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Data Output Current	50	mA	
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	℃•sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliablity.

RECOMMENDED DC OPERATING CONDITION

T_A=0℃ to 70℃/-40℃ to 85℃

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.5	V
V_{IL}	Input Low Voltage	-0.5(1)	-	0.8	V

Note :
1. V_{IL} = -3.0V for pulse width less than 30ns

TRUTH TABLE

/CS1	CS2	/WE	/OE	MODE	I/O OPERATION
H	X	X	X	Standby	High-Z
X	L	X	X		High-Z
L	H	H	H	Output Disabled	High-Z
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In

Note :
1. H=V_{IH}, L=V_{IL}, X=don't care

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

Symbol	Parameter		Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current		Vss ≤ V_{IN} ≤ Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current		Vss < V_{OUT} < Vcc, /CS1 = V_{IH} or CS2 = V_{IL} or /OE = V_{IH} or /WE = V_{IL}		-1	-	1	uA
I_{CC}	Operating Power Supply Current		/CS1 = V_{IL}, CS2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	5	10	mA
I_{CC1}	Average Operating Current		/CS1 = V_{IL} CS2 = V_{IH}, Min Duty Cycle = 100%, $I_{I/O}$ = 0mA		-	30	50	mA
I_{SB}	TTL Standby Current (TTL Input)		/CS1 = V_{IH} or CS2 = V_{IL}		-	1	2	mA
I_{SB1}	Standby Current (CMOS Input)	HY628100A	/CS1 ≥ Vcc - 0.2V		-	-	1	mA
			CS2 ≥ 0.2V or CS2 ≥ Vcc - 0.2V	L	-	2	100	uA
				LL	-	1	20	uA
		HY628100A-I		L	-	2	100	uA
				LL	-	1	30	uA
V_{OL}	Output Low Voltage		I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage		I_{OH} = -1mA		2.4	-	-	V

Note : Typical values are at Vcc = 5.0V, T_A = 25℃

AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

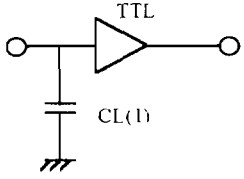
#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	55	-	70	-	85	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	25	-	35	-	45	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	20	0	25	0	30	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	25	0	30	ns
9	tOH	Output Hold from Address Change	10	-	10	-	10	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	55	-	70	-	85	-	ns
11	tCW	Chip Selection to End of Write	45	-	60	-	70	-	ns
12	tAW	Address Valid to End of Write	45	-	60	-	70	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	40	-	50	-	55	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	25	0	30	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	35	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC TEST CONDITIONS

T_A = 0℃ to 70℃(Normal) / -40℃ to 85℃(E.T.), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

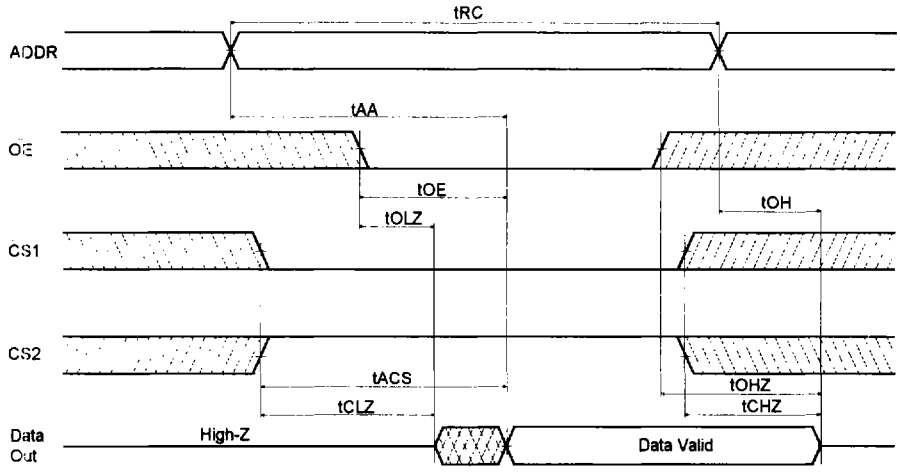
Temp = 25℃, f= 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

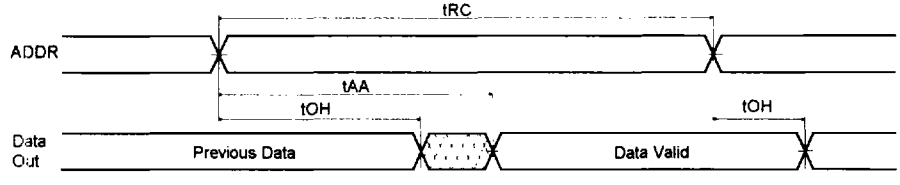
TIMING DIAGRAM

READ CYCLE 1



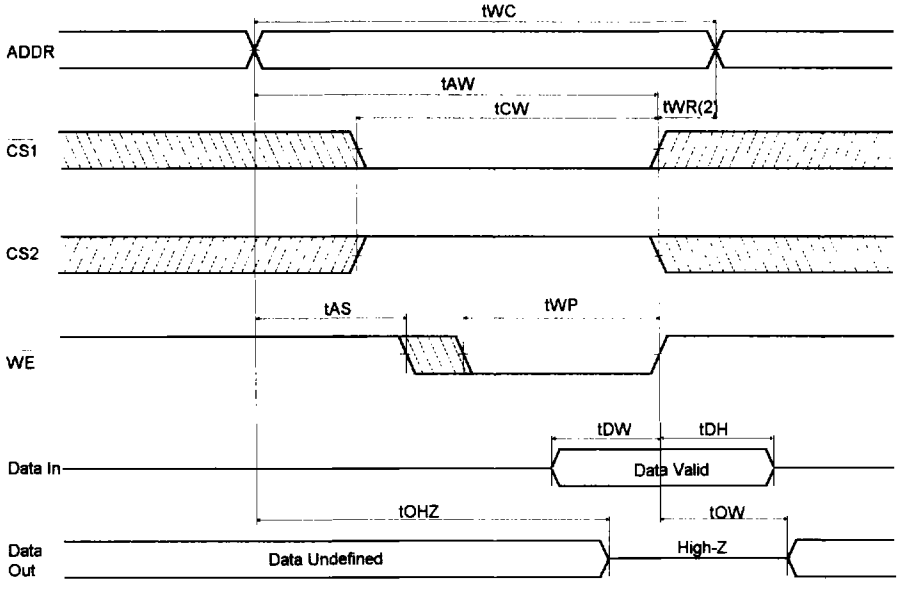
Note(READ CYCLE):
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

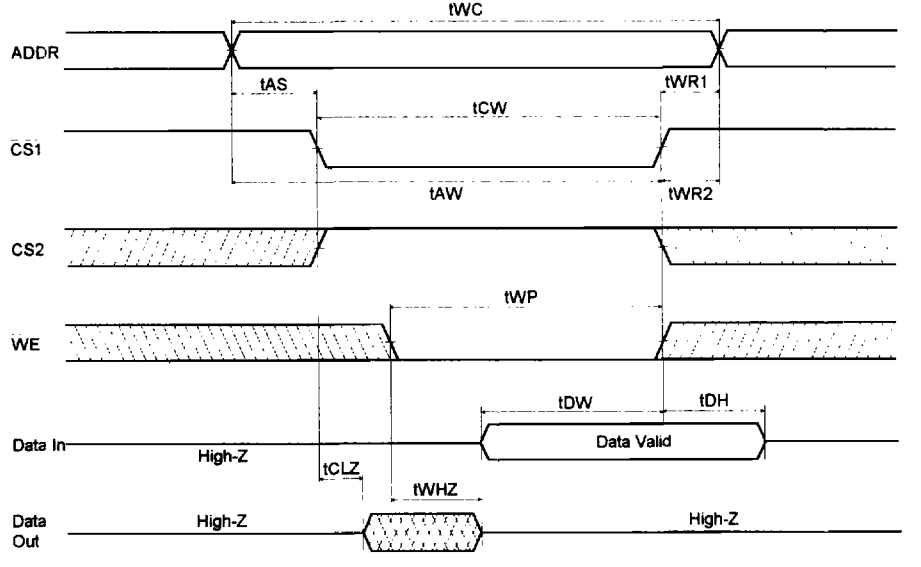


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS1 = V_{IL}, CS2 = V_{IH}
3. /OE =V_{IL}.

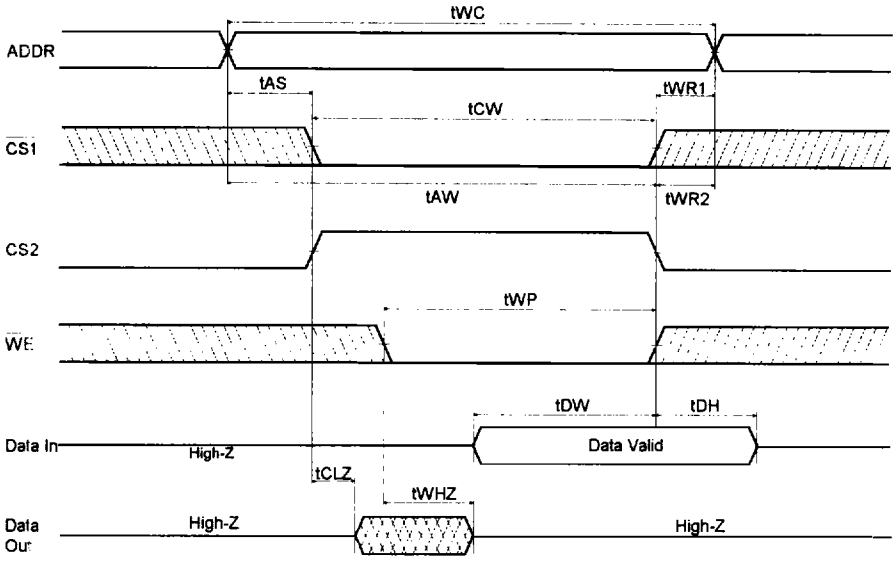
WRITE CYCLE 1(/WE Controlled)



WRITE CYCLE 2 (/CS1 Controlled)



WRITE CYCLE 3 (CS2 Controlled)



Notes(WRITE CYCLE):

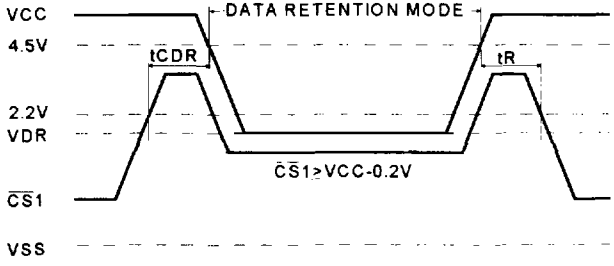
1. A write occurs during the overlap of a low /CS1, CS2 and low /WE. A write begines at the latest transition among /CS1 going low, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tRW is applied in case a write ends as /CS1, or /WE going high, and tWR2 is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When /CS1 is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

DATA RETENTION ELECTRIC CHARACTERISTIC

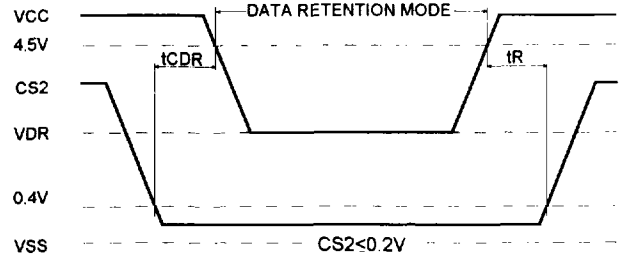
SYM	Parameter		Test Condition		Min	Typ	Max	Unit
VDR	Vcc for Data Retention		/CS1 ≥ Vcc - 0.2V CS2≤ 0.2V or ≥ Vcc - 0.2V, Vss≤VIN≤Vcc		2.0	-	-	V
ICCDR	Data Retention Current	HY628100A	Vcc = 3.0V, /CS1 ≥Vcc - 0.2V CS2≤ 0.2V or ≥ Vcc - 0.2V, Vss≤VIN≤Vcc	L	-	2	50	uA
				LL	-	1	10	uA
		HY628100A-I		L	-	1	50	uA
				LL	-	0.5	15	uA
tCDR	Chip Deselect to Data Retention Time				0	-	-	ns
tR	Operating Recovery Time				tRC(2)	-	-	ns

Notes:
1. Typical values are under the condition of TA = 25℃.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM 1



DATA RETENTION TIMING DIAGRAM 2

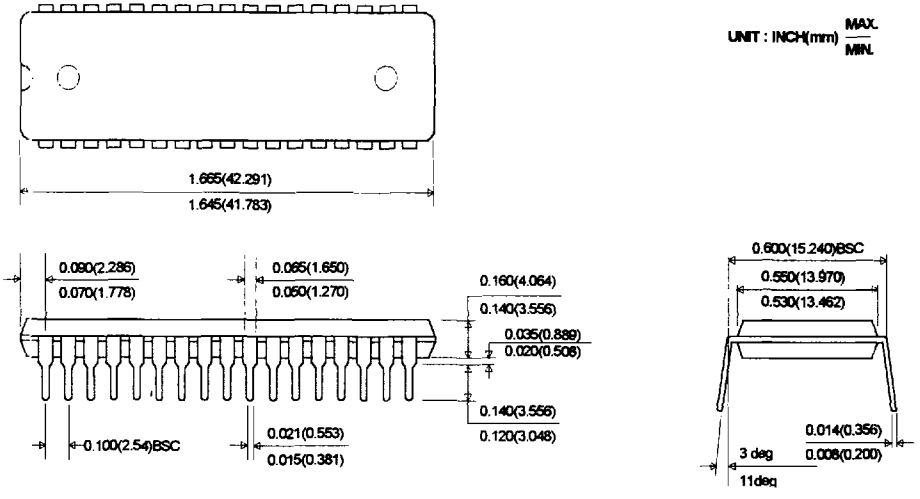


RELIABILITY SPEC.

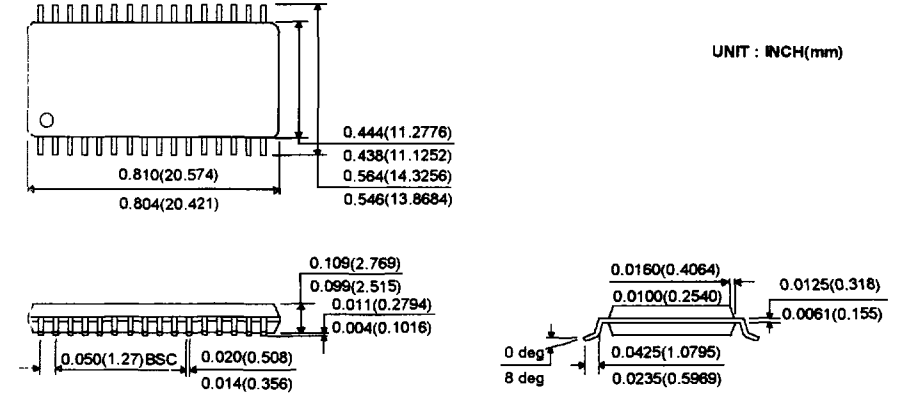
TEST MODE		TEST SPEC.
ESD	HBM	≥ 2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥ 100mA

PACKAGE INFORMATION

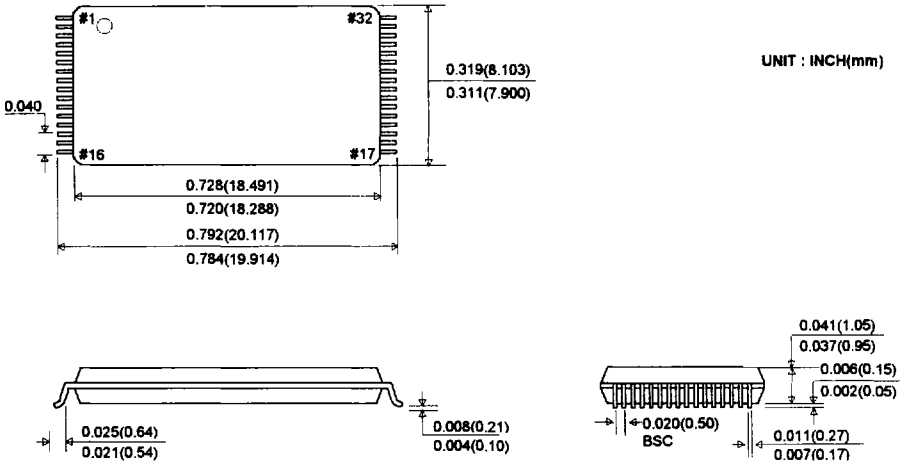
32pin 600mil Plastic Dual In Line Package(P)



32pin 525mil Small Outline Package(G)

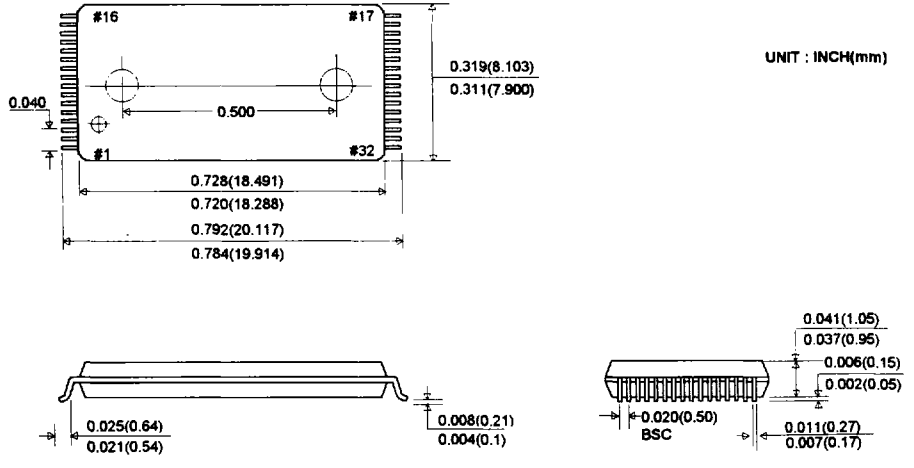


32pin 8x20mm Thin Small Outline Package Standard(T1)



UNIT : INCH(mm)

32pin 8x20mm Thin Small Outline Package Reversed(R1)



UNIT : INCH(mm)